USB2.0 Video Class

Tablet/PC Camera Controller

SN9C5258

Datasheet

Document No.- 5258 doc no.

Version 0.90

Revision	Date	Description
0.10	13-06-16	Draft of SN9C5258
0.20	13-09-03	Revise audio spec (sec2.9 & sec.3). Revise parallel sensor interface data
0.90	14-06-30	revise frame rate table revise pin diagram

Table of Contents

1 General Description

SN9C5258 is a USB 2.0 High-Speed compatible camera controller. The advanced power design provides low power consumption whenever device is under suspend, standby or operation mode. The low thermal design makes the module operating temperature inside platform under reasonable range. The SN9C5258 is fully compliant with USB Video Class. The supported OS includes Microsoft (Windows XP, Vista, 7 and 8/8.1.), Mac OS and Linux (Ubuntu. Android...etc.)

SN9C5258 support dual sensor interface(MIPI-CSI2 2 lane & Parallel 10bits) for application that need both BACK & FRONT cameras like Tablet/PC. Resolution of one is up to 5MP@30fps while another is up to FHD@30fps. It's able to extend the audio capability via D-Mic interface. The new generation image signal processor brings better visual experience. The high performance Motion-JPEG engine provides variant compression ratio to meet bandwidth requirement. With the integrated sensor interface and color processing engine, it can supports most available CMOS sensors. It is controlled by the embedded micro-controller and the statistics for 3A (AE / AWB / AF) are built-in. The flexible architecture is constituted by mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to fulfill customized features.

2 Features

2.1 System

- 3.3V single power supply
- Extreme low power consumption
  - standby: < 30mA (sensor is excluded)
  - suspend: <500uA (sensor is excluded)
- Built-in Clock Synthesizer for performance and power saving
- Built-in PLL for internal clock generation
- Using external serial flash to store customized code and data(default 128KBytes)
- High speed serial flash controller (60MHz) with phase detection
- External RAM is not needed
- 46-pins QFN 4.5x6.5mm package
- With 4 GPIO

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 compliant
- USB2.0 HS/FS auto sense and switch

- USB FS mode and USB disconnection are programmable
- Support device power state - Runtime D3 of ACPI
- 5 endpoints: CONTROL pipe, Bulk pipe, UVC Interrupt IN and Isochronous-IN (video, 24MB/s max), UAC Isochronous-IN
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Able to switch between 2 physical sensor interface: MIPI-CSI2(2 lane) & Parallel(10bits) which are exclusively active. MIPI-CSI2 (2 lane max.): support 5MP(2560x1920), 3MP(2048x1536) CMOS sensor. Parallel(10bits): support FHD(1920X1080), 2MP(1600x1200), 1.3MP(1280x1024), HD(1280x720), VGA(640x480) CMOS sensor
- Support both YUY2 and Bayer RAW image data format from sensor interface
- Support industrial standard 2-wire serial interface for sensor control

2.4 Color Processing

- AE histogram statistics
- AWB window statistics
- AF edge window statistics
- On-the fly defect-pixel cancellation
- Lens shading compensation for R/G/B channel
- Low pass filter
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels
- Programmable color conversion matrix for R/G/B input
- Configurable noise reduction
- De-color aliasing in Edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation
- Auto Gamma for backlight preview
- Auto Frequency for MSOC

2.5 Scaling Engine

- Fine scaling engine apply to both YUY2 and Bayer RAW input from sensor interface
- Fine scaling engine apply to both YUV and MJPG payload of UVC

- Fo supported sensors, combined scaling and windowing functions can provide similar field of view when output format range from QXGA~QQVGA
- With LPF to eliminate artifact

2.6 JPEG Encoder

- Built-in JPEG encoder to support USB Video Class MJPEG payload
- JPEG format is YUV422 baseline
- Programmable 128 bytes quantization table for Y and C to adjust compression ratio
- Encoding engine processing power is 150MP/sec (8MP@15fps, 5MP@30fps)

2.7 Video / Still Image

- Support UVC1.5 - Uncompressed YUY2 payload (YUV422, 16bits/pixel)
- Support UVC1.5 - Uncompressed M420 payload (YUV420, 12bits/pixel, for Lync F/G)
- Support UVC1.5 - MJPG payload
- Still image capture size is up to 5MP
- Support UVC still image capture method1 & method2

2.8 Frame rate

Mode		5M	3M	FHD	2M	1.3M	HD	VGA
BACK cam (MJPG)	BULK	30	30	60	60	60	60	60
	ISO	30	30	60	60	60	60	60
FRONT Cam (MJPG)	BULK	n/a	n/a	30	30	60	60	60
	ISO	n/a	n/a	30	30	60	60	60

2.9 Audio

- Support D-Mic(stereo) input interface with UAC1.0
- Programmable audio sampling frequency(8, 11.025, 16, 22.05, 24, 44.1, 48 kHz) and resolution (8/16 bits with mono/stereo)Programmable audio sampling frequency(8, 11.025, 16, 22.05, 24, 44.1, 48 kHz) and resolution (8/16 bits with mono/stereo)

2.10 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory
- Maximum CPU clock rate is 60MHz
- Auto load extended F/W from external serial flash
- Auto load VID/PID, manufacturer, product and serial number string from external serial flash
- Auto load UVC parameter definition from external serial flash
- Firmware is upgradeable from PC
- Able to force USB at FS mode & USB disconnect

- Watch dog to auto recovery
- With interrupt when sensor image transferring is finished of each frame

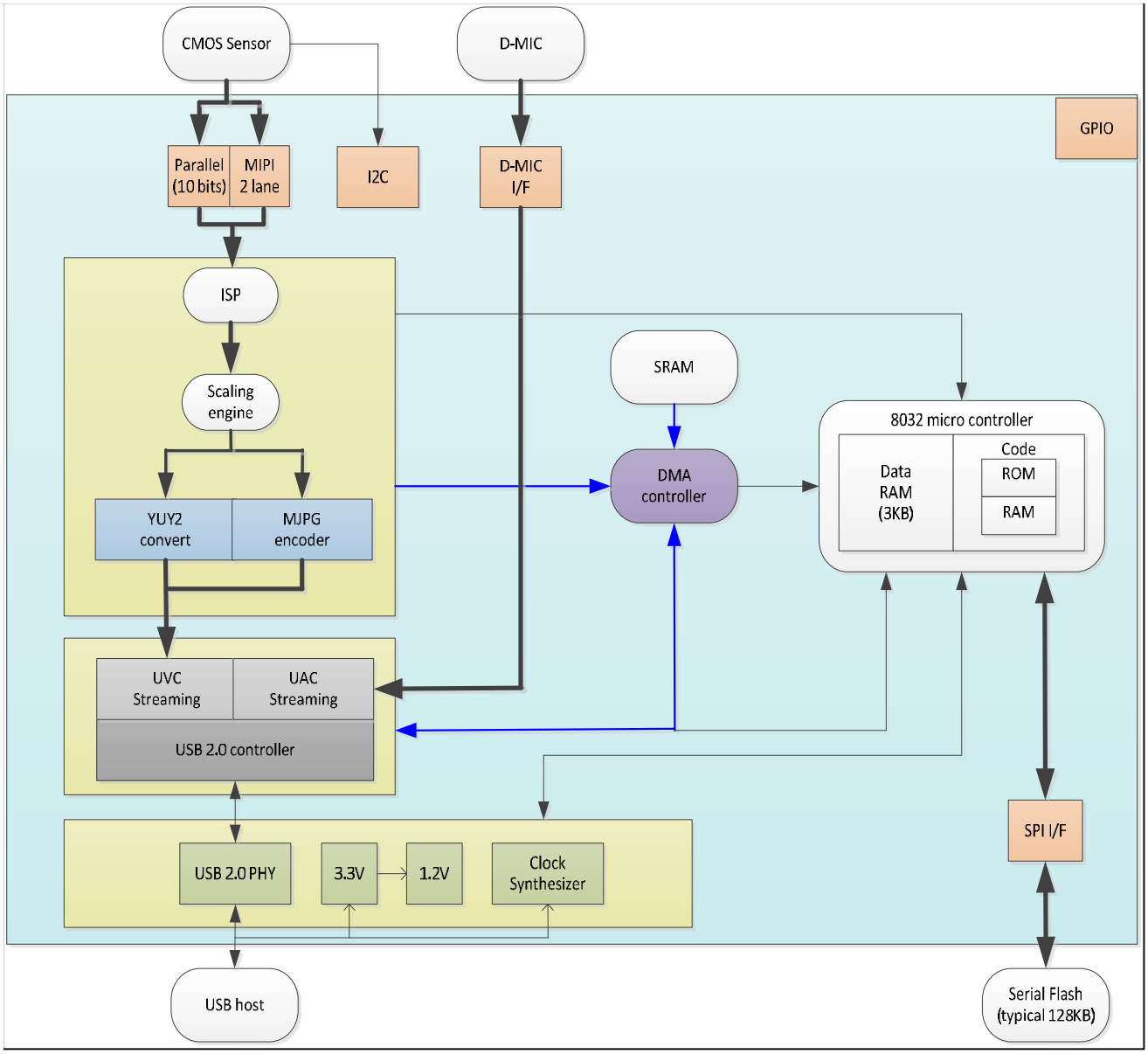
2.11 Pre-Defined for USB Video Class

- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)
- LED indicator on video streaming
- UVC Extension unit support

2.12 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit, Microsoft Window 7 32bit, Microsoft Window 7 64bit, Microsoft Window 8
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

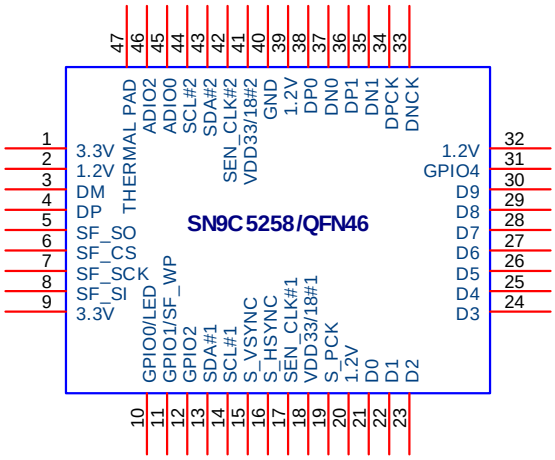
3 Function Block Diagram



4 Pin Assignment

4.1 SN9C5258 - QFN46

4.1.1 Pin-Out Diagram



4.1.2 Pin-Out Description

Pin No.	Pin Name	Description
1	3.3V	DSP system power.
2	1.2V	DSP core power.
3	DM	USB D-.
4	DP	USB D+.
5	SF_SO	SPI data out to serial flash.
6	SF_CS	SPI chip select to serial flash.
7	SF_SCK	SPI clock to serial flash.
8	SF_SI	SPI data in from serial flash.
9	3.3V	DSP system power.
10	GPIO[0]	General purpose I/O. Default for LED control.
11	GPIO[1]	General purpose I/O. Default for SPI serial flash write protect contro
12	GPIO[2]	General purpose I/O.
13	SDA#1	I2C data for parallel sensor.
14	SCL#1	I2C clock for parallel sensor.
15	S_VSYNC	Parallel sensor vsync.
16	S_HSYNC	Parallel sensor hsync.
17	SEN_CLK#1	Parallel sensor clock.
18	VDD33/18#1	I/O voltage level setting for parallel sensor.
19	S_PCK	Parallel sensor pixel clock.
20	1.2V	DSP core power.
21	D0	Parallel sensor image data.
22	D1	Parallel sensor image data.
23	D2	Parallel sensor image data.
24	D3	Parallel sensor image data.
25	D4	Parallel sensor image data.
26	D5	Parallel sensor image data.
27	D6	Parallel sensor image data.
28	D7	Parallel sensor image data.
29	D8	Parallel sensor image data.
30	D9	Parallel sensor image data.
31	GPIO4	General purpose I/O.
32	1.2V	DSP core power.
33	DNCK	MIPI sensor clock lane negative signal.
34	DPCK	MIPI sensor clock lane positive signal.
35	DN1	MIPI sensor data lane 1 negative signal.
36	DP1	MIPI sensor data lane 1 positive signal.
37	DN0	MIPI sensor data lane 0 negative signal.
38	DP0	MIPI sensor data lane 0 positive signal.
39	1.2V	MIPI power.
40	GND	Ground.
41	VDD33/18#2	I/O voltage level setting for MIPI sensor.
42	SEN_CLK#2	MIPI sensor clock.
43	SDA#2	I2C data for MIPI sensor.
44	SCL#2	I2C clock for MIPI sensor.
45	ADIO0	General purpose I/O or DMIC data in.
46	ADIO2	General purpose I/O or DMIC clock.

5 Electrical Characteristicsa

5.1 DC Operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD33_18	Power Supply	-0.3 ~ 3.6	V
DVDD	Power Supply	-0.12 ~ 1.32	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Typ	Units
VDD33	Power Supply	3.3	V
VDD33_18	Power Supply	3.3/1.8	V
DVDD	Power Supply	1.2	V
Vin	Input voltage	3.3	V

5.1.3 DC Electrical Characteristics

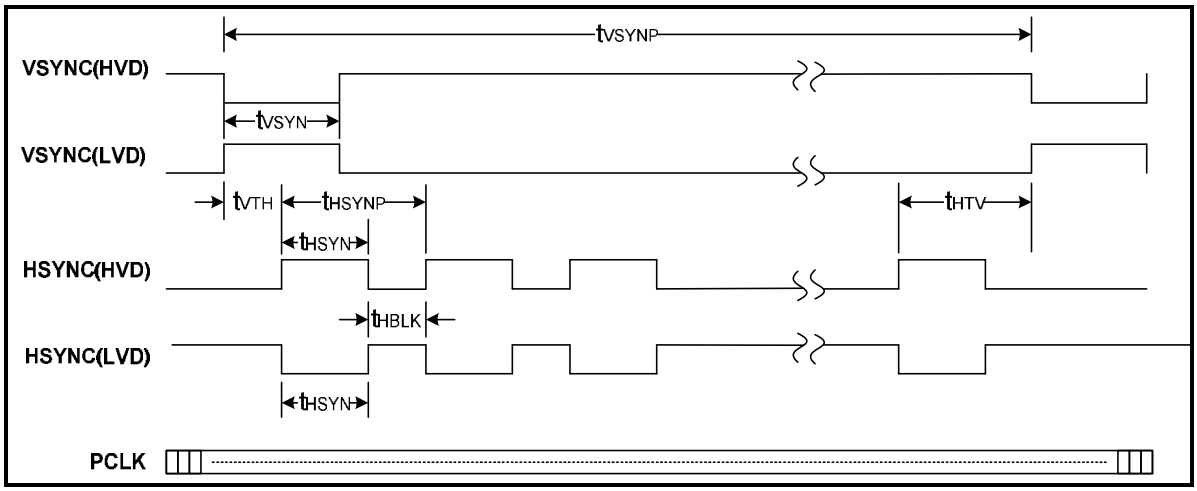
(Under Recommended Operating Conditions and
VDD33=3.0 ~ 3.6V, VDD33_18=1.62 ~ 3.6V, Ta=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDD33_18)	Input low voltage	CMOS	-0.3		0.2*VDD33_18	V
Vih(VDD33_18)	Input high voltage	CMOS	0.8*VDD33_18		VDD33_18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF

Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.2 AC Operating Condition

5.2.1 Parallel Sensor Interface

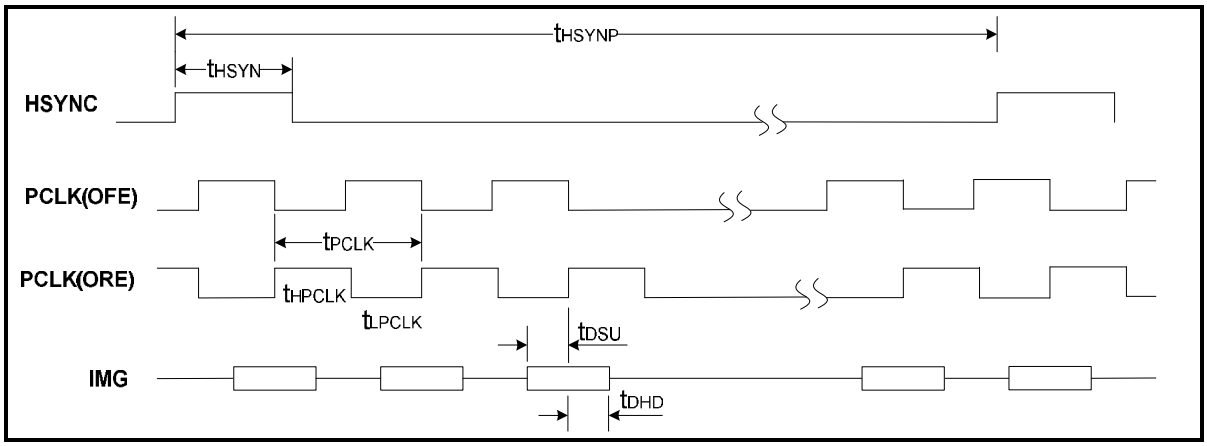


Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	tVSYNC	tPCLK	-	-	ns
VSYNC to HSYNC	tVTH	tPCLK	-	-	ns
HSYNC pulse width	tHSYN	tPCLK	-	-	ns
Blank time between two HSYNC	tHBLK	tPCLK	-	-	ns
HSYNC to VSYNC	tHTV	tHSYNP			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

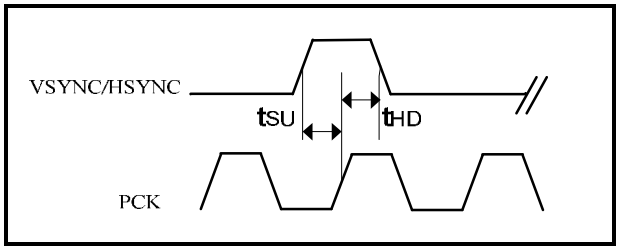
SYNC_MODE = 1 : (PCLK is free run)



Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

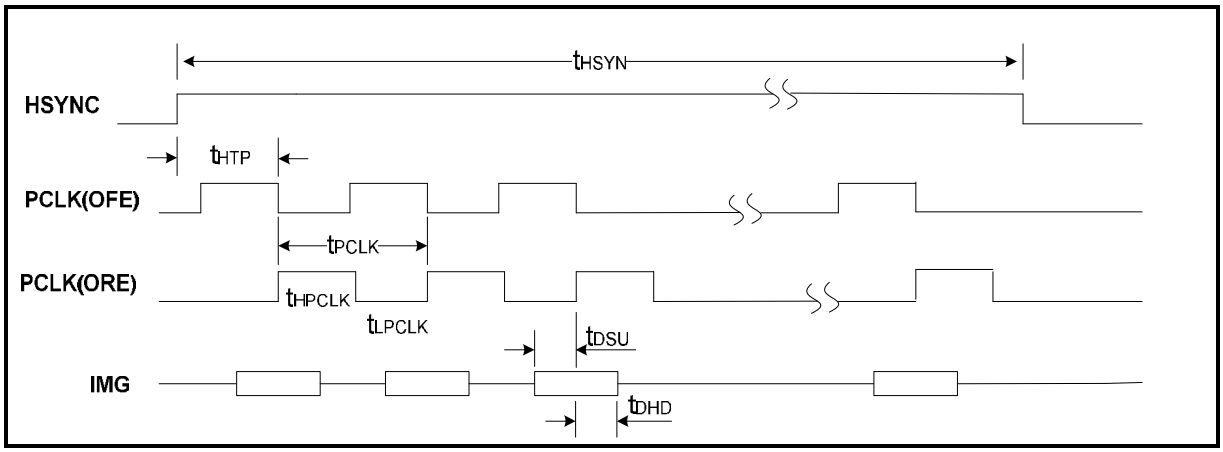
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	tSU	2	-	-	ns
VSYNC / HSYNC hold time	tHD	2	-	-	ns

SYNC_MODE = 0 : (PCLK is output only when hsync active)



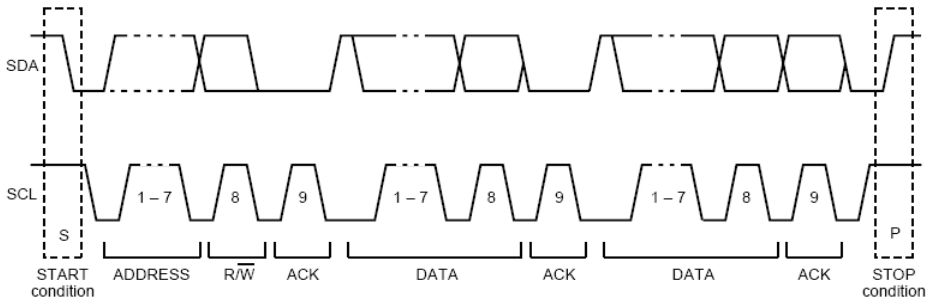
Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	HSIZE * tPCLK	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}	-	-	
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

Note:

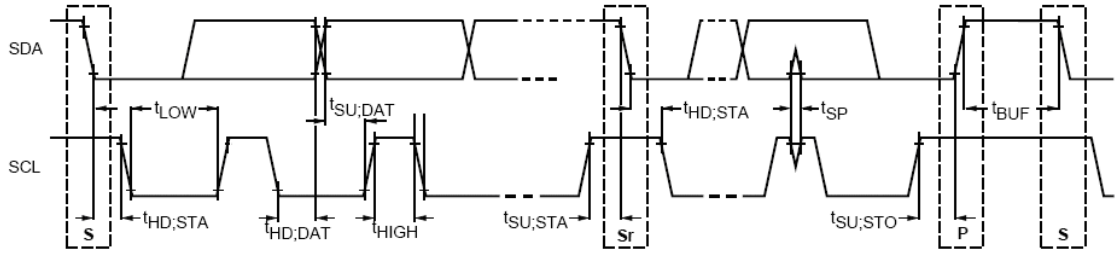
1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge
4. HSIZE represents total valid PCLK number per horizontal line

5.2.2 MIPI Sensor Interface(TBD)

5.2.3 I2C Control Interface



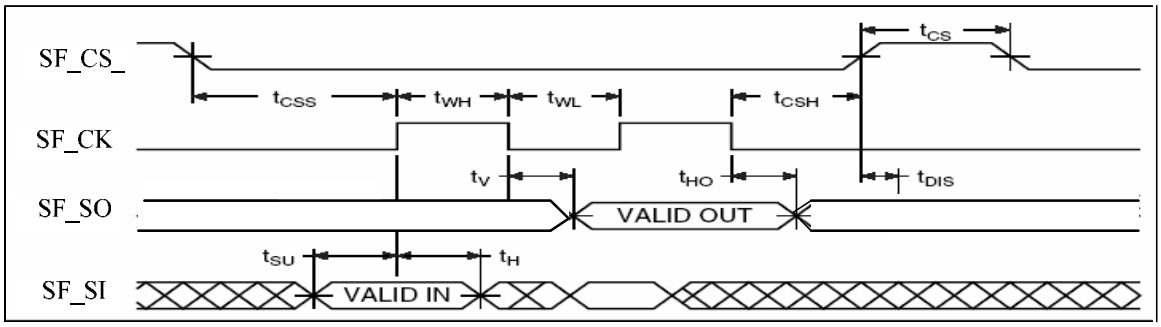
A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.4 Serial Flash Interface



When fSCK = 24 Mhz (SPEED=1)

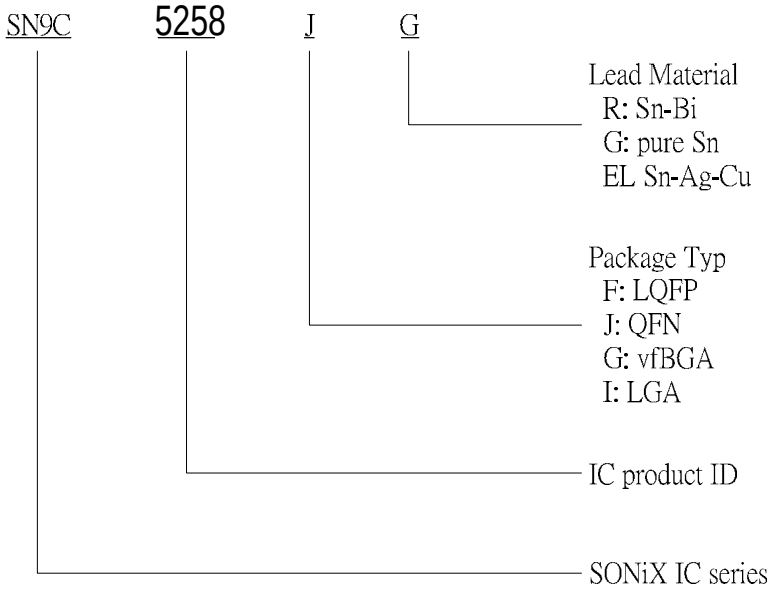
Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

When fSCK = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

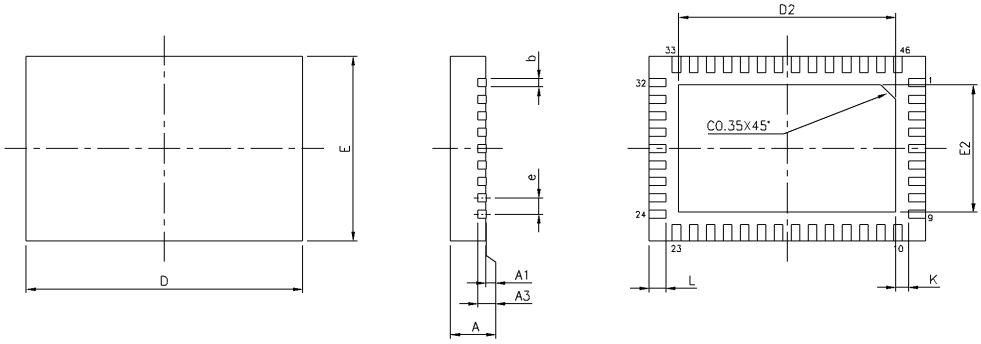
6 Package

6.1 Nomenclature



6.2 QFN46 - SN9C5258

6.2.1 Drawing



6.2.2 Dimension

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D	6.40	6.50	6.60
E	4.40	4.50	4.60
e		0.40 BSC.	
D2	5.00	5.10	5.20
E2	3.00	3.10	3.20
L	0.35	0.40	0.45
K	0.20	-	-

NOTES:

1. JEDEC OUTLINE : N/A

2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SUOULD NOT BE MEASURED IN THAT RADIUS AREA.

3. THE MINIUM "K" VALUE OF 0.20mm APPLIES.

4. BILATERAL COPLANARITY ZONE APPLIES TO THE

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