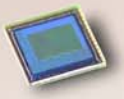
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/5" CMOS UXGA (2 Megapixel) CameraChip™ sensor
with OmniPixel3-HS™ technology

OV2655

color CMOS UXGA (2 Megapixel) CameraChip™ sensor with OmniPixel3-HS™ technology

datasheet (CSP2)
PRELIMINARY SPECIFICATION

version 1.2
august 2008

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still camera

ordering information

- **OV02655-V38A** (color, lead-free)
  38-pin CSP2

features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, scaling, cropping and windowing
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555, YUV422/420 and YCbCr422
- support for images sizes: UXGA, and any arbitrary size scaling down from SXGA
- support for video or snapshot operations
- support for horizontal and vertical sub-sampling
- embedded anti-shake
- support for internal and external frame synchronization
- support for LED and flash strobe mode
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI serial output interface
- support for second camera sharing ISP and MIPI interface
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- support for black sun cancellation
- suitable for module size of 6.5mm x 6.5mm
- High Dynamic Range (HDR) mode for SVGA (800x600) or lower resolutions providing a dynamic range of ~ 85dB

key specifications

- **active array size:** 1600 x 1200
- **power supply:**
  core: 1.5VDC ± 5%
  analog: 2.45 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 250 mW
  standby: 75 µA
- **temperature range:**
  operating: -20°C to 70°C
  stable image: 0°C to 50°C
- **output formats (8-bit):** YUV(422/420) / YCbCr422, RGB565/555, 8-/10-bit raw RGB data
- **lens size:** 1/5"
- **lens chief ray angle:** 25° non-linear (see **table 10-1**)
- **input clock frequency:** 6 ~ 27 and 54 MHz
- **S/N ratio:** 37 dB
- **dynamic range:** 66 dB
- **maximum image transfer rate:**
  UXGA (1600x1200): 15 fps for UXGA and any size scaling down from SXGA
  SVGA (800x600): 30 fps for SVGA and any size scaling down from SVGA
- **sensitivity:** 1030 mV/(Lux • sec)
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1235 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** 7 Ke^-
- **dark current:** 4 mV/sec @ 60°C
- **fixed pattern noise (FPN):** 1% of $V_{PEAK\ to\ PEAK}$
- **image area:** 2842 µm x 2121 µm
- **package dimensions:** 4835 µm x 4895 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV2655 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 2)

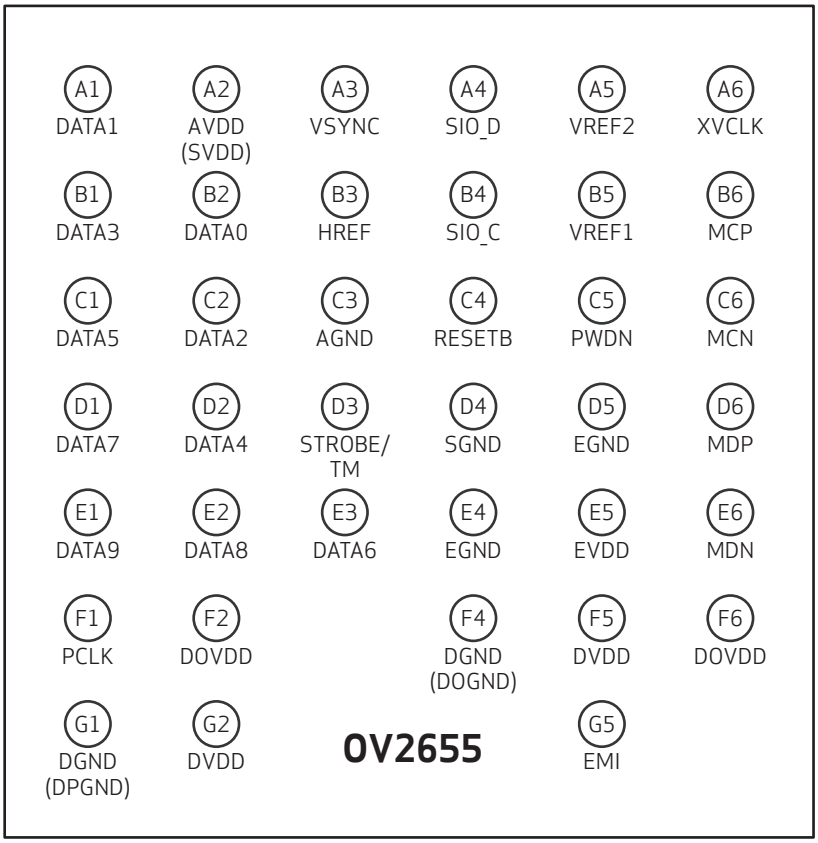
pin number	signal name	pin type	description	default I/O status
A1	DATA1[a]	I/O	digital video port (DVP) bit[1]	input
A2	AVDD	power	power for analog circuit/sensor array	
A3	VSYNC	I/O	vertical sync output	input
A4	SIO_D	I/O	SCCB data	
A5	VREF2	reference	internal anolog reference	
A6	XVCLK	input	system input clock	
B1	DATA3[a]	I/O	digital video port (DVP) bit[3]	input
B2	DATA0[a]	I/O	digital video port (DVP) bit[0]	input
B3	HREF	I/O	horizontal reference output	input
B4	SIO_C	input	SCCB input clock	
B5	VREF1	reference	internal analog reference	
B6	MCP	output	MIPI clock lane positive output	
C1	DATA5[a]	I/O	digital video port (DVP) bit[5]	input
C2	DATA2[a]	I/O	digital video port (DVP) bit[2]	input
C3	AGND	ground	ground for analog circuit	input
C4	RESETB	input	reset (active low with internal pull-up resistor)	
C5	PWDN	input	power down (active high with internal pull-down resistor)	
C6	MCN	output	MIPI clock lane negative output	
D1	DATA7[a]	I/O	digital video port (DVP) bit[7]	input
D2	DATA4[a]	I/O	digital video port (DVP) bit[4]	input
D3	STROBE	I/O	strobe output or scan chain test mode	input
D4	SGND	ground	ground for sensor analog	
D5	EGND	ground	ground for MIPI core	
D6	MDP	output	MIPI data lane positive output	

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
E1	DATA9[a]	I/O	digital video port (DVP) bit[9]	input
E2	DATA8[a]	I/O	digital video port (DVP) bit[8]	input
E3	DATA6[a]	I/O	digital video port (DVP) bit[6]	input
E4	EGND	ground	ground for MIPI core	
E5	EVDD	reference	power for MIPI core	
E6	MDN	output	MIPI data lane negative output	
F1	PCLK	I/O	pixel clock output	input
F2	DOVDD	power	power for I/O circuit	
F3	NC	–	no connect	
F4	DGND	ground	ground for digital core	
F5	DVDD	reference	power for digital core	
F6	DOVDD	power	power for I/O circuit	
G1	DGND	ground	ground for digital core	
G2	DVDD	reference	power for digital core	
G3	NC	–	no connect	
G4	NC	–	no connect	
G5	EMI	ground	ground	
G6	NC	–	no connect	

a. 10-bit output (RAW): DATA9 ~ DATA0; 8-bit output: DATA9 ~ DATA2

figure 1-1 pin diagram



2 system level description

2.1 overview

The OV2655 (color) CameraChip™ sensor is a low voltage, high-performance 1/5-inch 2.0 megapixel CMOS image sensor that provides the full functionality of a single chip UXGA (1600x1200) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV2655 has an image array capable of operating at up to 15 frames per second (fps) in UXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, Omnivision CameraChip sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For storage purposes, the OV2655 includes a one-time programmable (OTP) memory.

The OV2650 has a one lane MIPI interface and a traditional parallel digital video port. The sensor's advanced integrated Image Signal Processor (ISP) can also be used by to communicate to an external secondary camera (digital video port) while providing continued output through the MIPI interface.

OmniVision's OV2650 sensor has a High Dynamic Range mode which can be used in SVGA or lower resolutions for either still image or video capturing.

2.2 architecture

The OV2655 sensor core generates stream pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV2650 image sensor. **figure 2-2** shows an example application using an OV2650 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV2655 block diagram

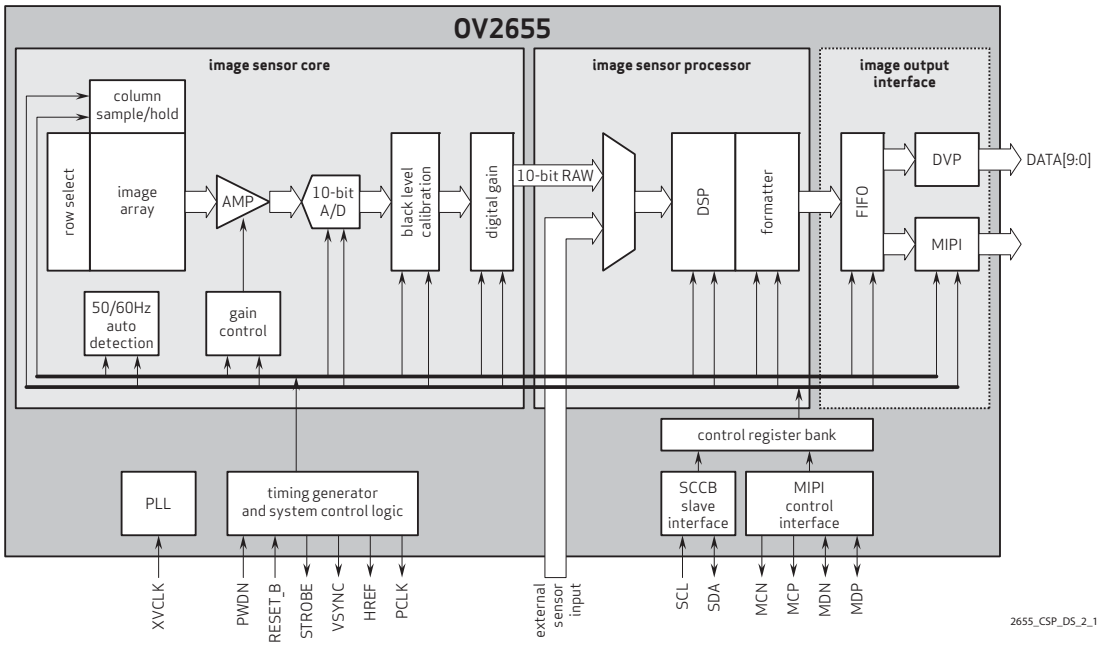
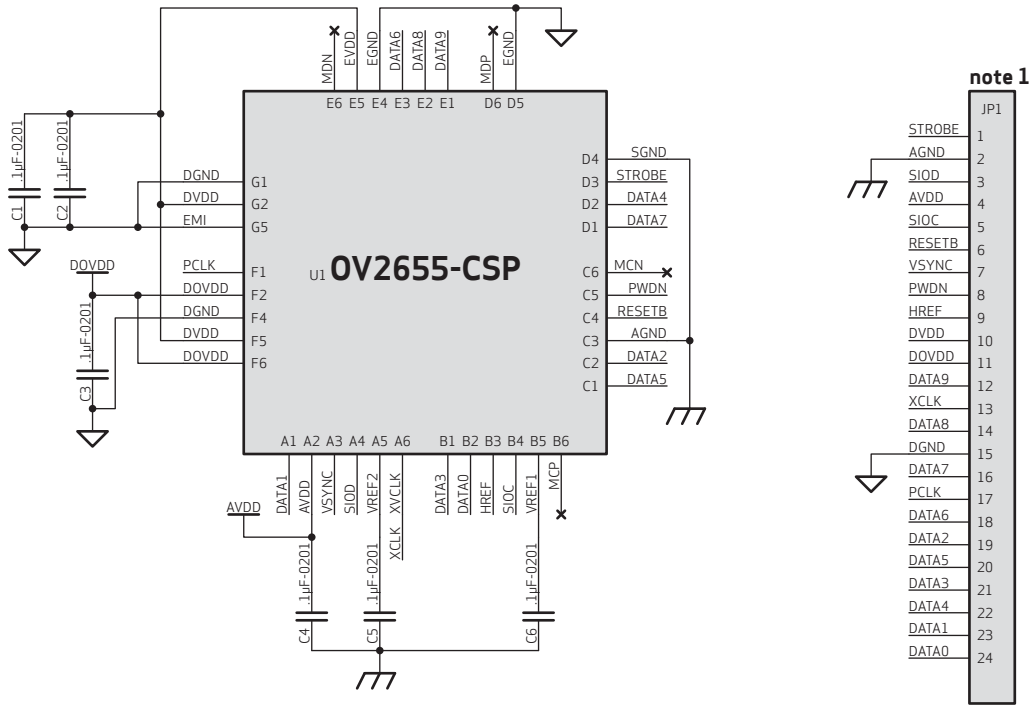


figure 2-2 reference design schematic



note 1 flex cable to Molex 52437-2491

note 2 PWDN should be connected to ground outside of module if unused.
RESETB should be connected to DOVDD outside of module if unused.
AVDD is 2.45 - 3.0V of sensor analog power (clean).
DVDD is 1.5V ±10% of sensor digital power (clean).
sensor pins AGND and DGND should be separate and connect to a single point outside PCB (DO NOT connect inside module).
decoupling capacitors should be close to the related sensor pins.
DATA9:0 is sensor RGB 10-bit output (DATA9: MSB, DATA0: LSB).

2655_CSP_DS_2_2

2.3 I/O control

The OV2655 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output drive capability control	0x30B2[1:0]	output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] I/O control	{0x30B1[1:0], 0x30B0[7:0]}	input/output selection for the DATA[9:0] pins 0: input 1: output
VSYNC I/O control	0x30B1[5]	input/output selection for the VSYNC pin 0: input 1: output
HREF I/O control	0x30B1[2]	input/output selection for the HREF pin 0: input 1: output
PCLK I/O control	0x30B1[3]	input/output selection for the PCLK pin 0: input 1: output
STROBE I/O control	0x30B1[4]	input/output selection for the STROBE pin 0: input 1: output

2.4 format and frame rate

table 2-2 format and frame rate

format	resolution	frame rate	scaling method	parallel port data rate (RAW/YUV)	MIPI data rate (RAW/YUV)
UXGA	1600x1200	15 fps	full	36/72 MHz	360/576 MHz
SXGA	1280x1024	15 fps	scaling	36/72 MHz	360/576 MHz
SVGA	800x600	15~30 fps	scaling from full at 15 fps	18/36 MHz	180/288 MHz
			vertical scaling from full at 30 fps	18/36 MHz	180/288 MHz
VGA	640x480	15~30 fps	scaling from full at 15 fps	18/36 MHz	180/288 MHz
			scaling from SVGA (VarioPixel) at 30 fps	18/36 MHz	180/288 MHz
CIF	352x288	15~30 fps	scaling from full at 15 fps	9/18 MHz	90/144 MHz
			scaling from SVGA (VarioPixel) at 30 fps	9/18 MHz	90/144 MHz
below SXGA	<SXGA	15~30 fps		SXGA ~SVGA 36/72 MHz	360/576 MHz
			scaling from full at 15 fps	SVGA~400x300 18/36 MHz	180/288 MHz
				400x300 and below 9/18 MHz	90/144 MHz
			scaling from SVGA (VarioPixel) at 30 fps	SVGA~400x300 18/36 MHz	180/288 MHz
				400x300 and below 9/18 MHz	180/288 MHz

2.5 system clock control

The OV2655 PLL allows for an input clock frequency ranging from 6~27 Mhz and 54 Mhz.

The PLL can be bypassed by setting register 0x300F[3] to 1.

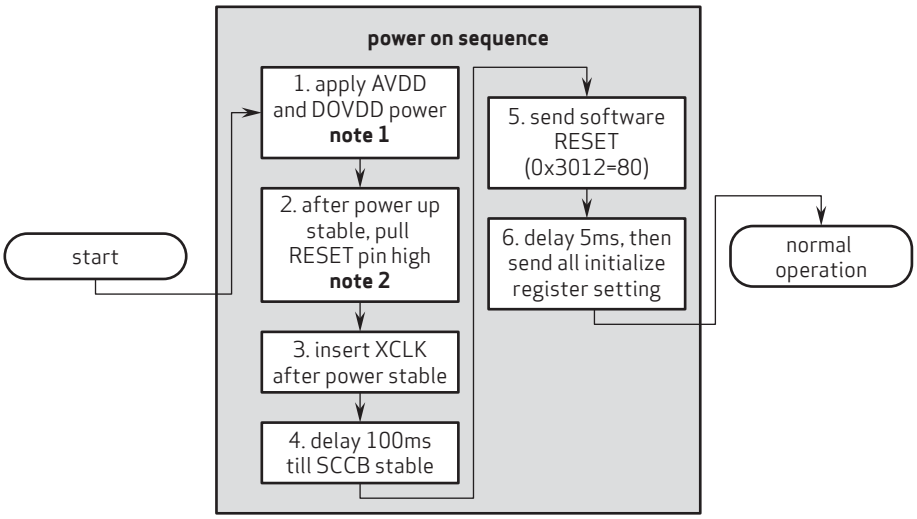
2.6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the CameraChip sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.7 power on sequence

Powering up the OV2655 sensor requires an analog power (AVDD) and digital power (DOVDD) to connect simultaneously. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power-up reset is included.

figure 2-3 power on sequence diagram

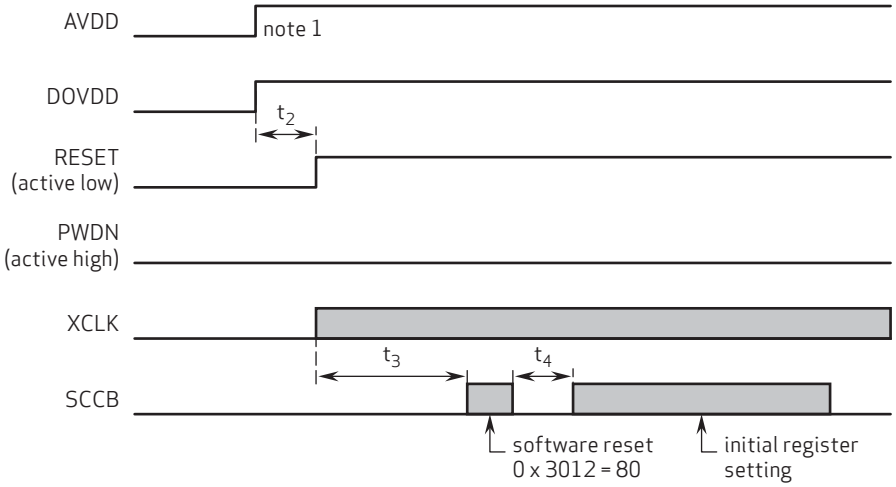


note 1 if AVDD and DOVDD are applied separately, the power on sequence should be DOVDD first then AVDD. The delay between AVDD and DOVDD should be as short as possible.

note 2 the delay between power stable and insert RESET signal should more than 3ms

2655_DS_2_3

figure 2-4 power on timing diagram



note 1: OmniVision strongly suggest to provide analog power and IO power at same time. If they are not provide at same time, digital power shuold come first and delay should be as short as possible.
t_2: after power stable, reset signal should be more than 3 ms
t_3: after more than 100ms, send SCCB command
t_4: delay 5ms

2655_DS_2_4

2.8 reset

The OV2655 sensor includes a RESET_B pin that forces a complete hardware reset when it is pulled low (GND). The OV2655 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3012[7] to high.

2.9 standby and sleep

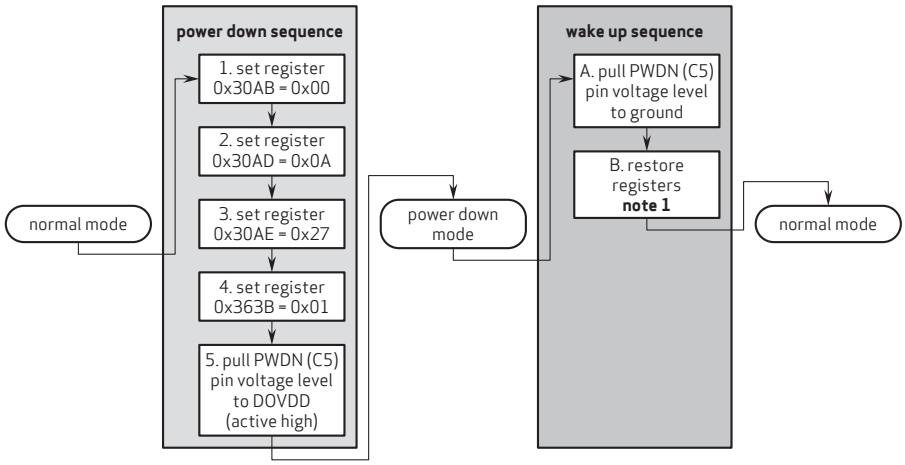
Two suspend modes are available for the OV2655:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode (see **figure 2-5**):

1. Set 0x30AB=00 and 0x30AD=0A
2. Set 0x30AE = 27 and 0x363B = 01
3. The PWDN pin must be tied to high

figure 2-5 power down/ wake up sequence



note 1 after the wake up sequence, if the MIPI connection detection function is needed, then register 0x363B must be restored to its original value.

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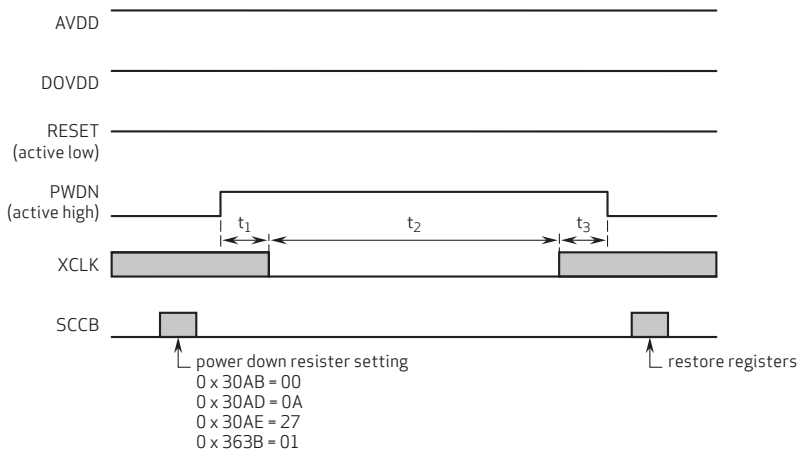
figure 2-6 power down timing diagram



note t_1: XCLK should keep more than 0.1ms after PWDN pull high
t_2: power down period should last more than 1 VSYNC period
t_3: XCLK should come more than 0.1ms before PWDN pull low

2655_DS_2.6

When this occurs, the OV2655 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

The OV2655 also supports MIPI ultra low power state (ULPS). After receiving ULPS command from host, the OV2655 will enter into ULPS mode. Except for the low speed part of the MIPI PHY and SCCB, all other blocks are enter into power down mode in ULPS mode.

2.10 power off sequence

Powering off the OV2655 sensor is described in **figure 2-7**.

figure 2-7 power off sequence diagram

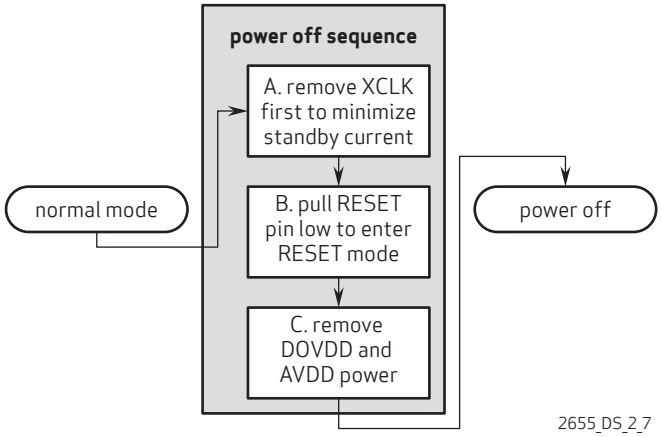
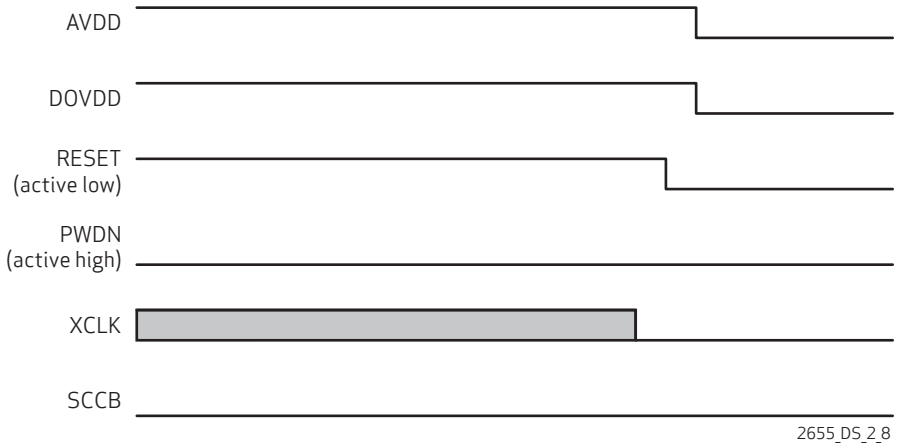


figure 2-8 power off timing diagram



3 block level description

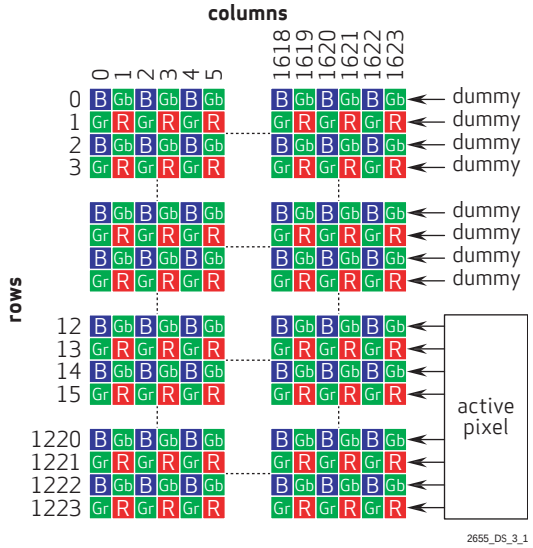
3.1 pixel array structure

The OV2655 sensor has an image array of 1624 columns by 1224 rows (1,987,776 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 1,987,776 pixels, 1,920,000 (1600x1200) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV2655 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV2655 usually delays the read-out sequence by one pixel by setting register **0x307C[1]** to 1. In flip, the OV2655 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make necessary adjustments.

figure 4-1 mirror and flip samples

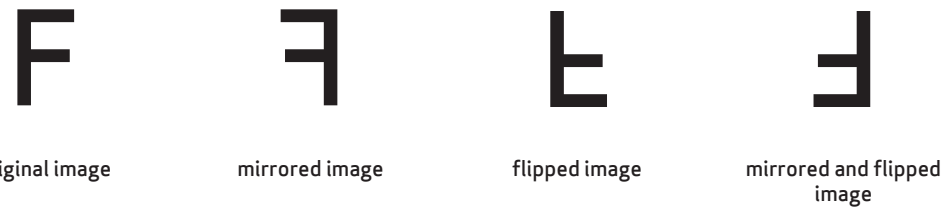


table 4-1 mirror and flip function control

function	register	description
mirror	0x307C[1]	mirror ON/OFF select 0: mirror OFF 1: mirror ON
	0x3090[3]	array mirror ON/OFF select 0: array mirror OFF 1: array mirror ON
flip	0x307C[0]	flip ON/OFF select 0: flip OFF 1: flip ON
	0x3023	B/R row adjustment

4.2 image windowing

An image windowing area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), and VH (vertical height). By properly setting the parameters, any portion within the sensor array size can be cropped as a visible area. This windowing is achieved by simply masking the pixels outside the window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image windowing

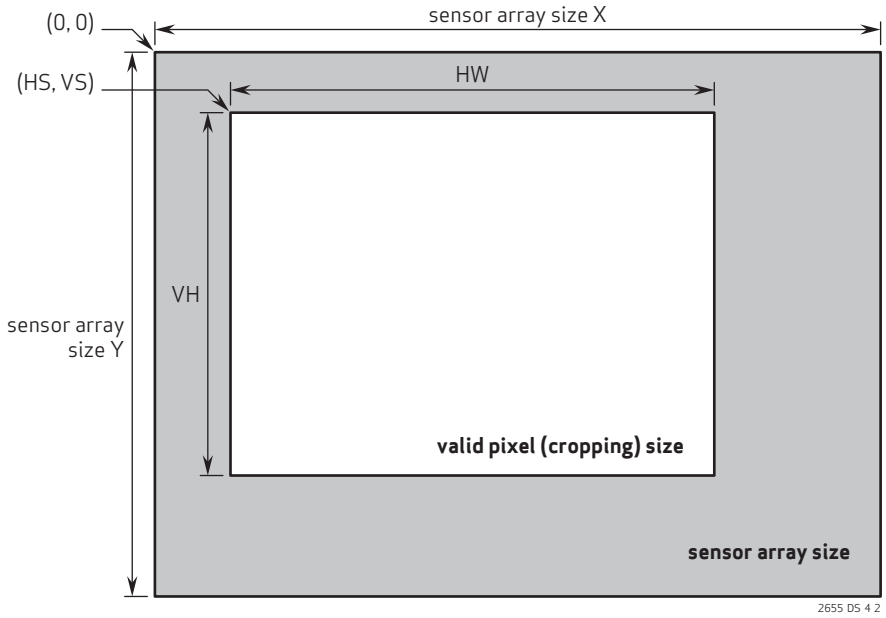


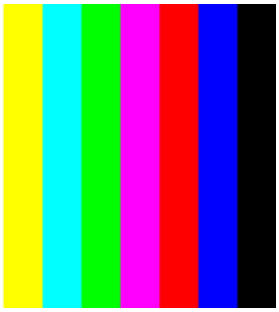
table 4-2 image cropping control functions

function	register	description
horizontal start	[0x3020, 0x3021]	HS[15:8] = 0x3020 HS[7:0] = 0x3021
vertical start	[0x3022, 0x3023]	VS[15:8] = 0x3022 VS[7:0] = 0x3023
horizontal width	[0x3024, 0x3025]	HW[15:8] = 0x3024 HW[7:0] = 0x3025
vertical height	[0x3026, 0x3027]	VH[15:8] = 0x3026 VH[7:0] = 0x3027

4.3 test pattern

For testing purposes, the OV2655 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-3 test pattern selection control

function	register	description
color bar	0x3308[0]	color bar enable 0: color bar OFF 1: color bar enable

4.4 50/60hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50hz or 60hz light source so that the basic step of integration time can be determined.

4.5 AEC/AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the CameraChip sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control.

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

4.7 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

4.8 strobe flash control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV2655 provides a programmable strobe signal function.

4.8.1 sensor-controlled strobe flash

The OV2655 can generate a programmable strobe signal from Strobe (pin D4). **table 4-4** lists the strobe pulse control registers.

table 4-4 strobe control functions

function	register	description
strobe function enable	0x307A[7]	strobe function enable 0: strobe disable 1: start strobe enable
strobe output pulse polarity control	0x307A[6] (TMC4[6])	strobe output polarity control 0: positive pulse 1: negative pulse
xenon mode strobe pulse width	0x307A[3:2] (TMC4[3:2])	xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
strobe mode	0x307A[1:0] (TMC4[1:0])	strobe mode select 00: xenon mode 01: LED 1 & 2 mode 10: LED 1 & 2 mode 11: LED 3 mode

4.8.1.1 strobe pulse

The strobe signal is programmable. It supports both LED and Xenon mode. The polarity of the pulse can be changed. The strobe signal is enabled (turned high / low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered to the rising edge (falling edge, if signal polarity is changed). It supports the flashlight modes shown in **table 4-5**.

table 4-5 flashlight modes

function	register	description
xenon	one pulse	no
LED 1	pulse	no
LED 2	pulse	no
LED 3	continuous	yes

4.9 one time programmable (OTP) memory

The OV2655 supports 96 bits maximum one-time programmable (OTP) memory to store chip identification and manufacturing information. Contact your local OmniVision FAE for more details.

5 image sensor processor digital functions

5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down and cen control, top level control signals as well as ISP modules that require control bytes (WBC, VarioPixel, UV_AVG, and YUV444to422).

- WBC: White Black pixel Canceling is used to detect and remove defect pixels.
- VarioPixel: This module is used to do pixel 2:1 sub sample in horizontal view. There are various ways to use VarioPixel function such as give out the average of 2 pixels, give out the first pixel and drop the second, or give out the second and drop the first.
- UV_AVG: The U and V average module is used to smooth chrominance to let color image looks better around edge. It has 2 options to do that: average with 5 consecutive U or V and get median value from 5 consecutive U or V.
- YUV444to422: This module is used to convert YUV444 to YUV422. This module has two options: average mode and drop mode.

5.2 ISP DCW, border cutting

This part includes the size registers for ISP input windowing, ISP output windowing, and Scaling input windowing. The ISP input windowing is designed to support digital zoom. It can get any size window in any position. The ISP output windowing and Scaling input windowing are both for cutting some border pixels or border lines which are not good enough due to algorithm limitation.

5.3 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. There are two main functions AWB: AWB_Stat and AWB_Gain.

- AWB_Stat is used to automatically generate digital gains for different light sources
- AWB_Gain is used to apply the AWB_Stat information gains on RAW data to remove unrealistic color

5.4 gamma

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

5.5 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

5.6 black level correction (BLC) and black level follower (BLF)

Black Level Correction (BLC) and Black Level Follower (BLF) are used to adjust black level situations. The ISP is an offset for BLC; ISP has to reduce this offset before applying any kind of digital gain, such as AWB, LENC, Gamma, and CMX, then add the offset back after multiplying gain. BLF is used to calculate the offset, truncate all levels below offset to 0 and stretch other levels to full range. If the BLF is enabled, modules after BLF do not need to consider BLC offset.

5.7 color interpolation (CIP), DNS and sharpen

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge ehancement. CIP functions work in both manual and auto modes.

5.8 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain. For different color temperatures, the parameters in the transmitting function will be changed.

5.9 UV adjust (UV_ADJ)

UV adjust (UV_ADJ) is used to reduce chrominance values in low light conditions to improve image quality. The higher AGC gain is, the lower the chrominance values. UV_ADJ has an automatic and manual mode.

5.10 special digital effect (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v registers. Calculate Y using Y offset, Y gain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

5.11 HDR

The HDR module has long and short exposure data which can be combined into one form of exposure data. This module includes two blocks (Combine and Stretch). Combine adds long and short exposure data together and Stretch receives data from Combine, removes the top and bottom levels in the image histogram, while stretching the image histogram to full range for enhanced image quality.

5.12 ANTI_Shake

The main purpose of ANTI_Shake is to prevent image motion during capture.

5.13 ISP system control

System control registers include clock and reset gated control. Individual modules can be reset or clock gated by setting registers 0x3104, 0x3105, 0x3107 and 0x3108.

5.14 format description

Format control converts internal data format into the desirable output format including YUV, RGB and raw.

table 5-1 format control register list (sheet 1 of 2)

register address	register name	function
0x3400	FMT_CTRL00	FMT_CTRL00 0x00: YUV422 yuyvyuyv.../yuyvyuyv..... (data order can be adjusted by FMT_CTRL[3:0]) 0x10: YUV420 yyyyyyyy..../yuyvyuyv.... (data order can be adjusted by FMT_CTRL[3:0]) 0x20: Y8 yyyyyyy...../yyyyyyyyy.... 0x30: YUV444(RGB888): yuvyuv...../yuvyuv....(gbrgbr..../gbrgbr....) (based on rgb_sel, SC_CTRL0[1]) (data order can be adjusted by FMT_CTRL[3:0]) 0x40: RGB565 {b[4:0],g[5:3]}, {g[2:0],r[4:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x50: RGB555: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x60: RGB444 {bFMT_CTRL[3:0],1'b0,g[3:1]},{g[0],2'h0, rFMT_CTRL[3:0],1'b0} (data order can be adjusted by FMT_CTRL[3:0]) 0x70: RGB444 {bFMT_CTRL[3:0],gFMT_CTRL[3:0]},{rFMT_CTRL[3:0], bFMT_CTRL[3:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x80: RGB444 {4'b0,bFMT_CTRL[3:0]},{gFMT_CTRL[3:0], rFMT_CTRL[3:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x90: Raw bgbgbg..../grgrgr..... (pixel order can be adjusted by FMT_CTRL[3:0]) 0xA0: YUV420 uyyuyyu..../vyyvyyvyy..... 0xB0: RGB555 {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} (data order can be adjusted by FMT_CTRL[3:0])

table 5-1 format control register list (sheet 2 of 2)

register address	register name	function
0x3401	FMT_CTRL1	FMT_CTRL1 Bit[7:6]: VMAX[1:0] (used for clipping) Bit[5:4]: VMIN[1:0] (used for clipping) Bit[3]: UV_SEL, for yuv422 or yuv420 0: Y0U_AVG,Y1,V_AVG 1: Y0U0,Y1V0 Bit[2:0]: Reserved
0x3402	FMT_CTRL2	FMT_CTRL2 Bit[7:6]: Ymax[1:0] Bit[5:4]: Ymin[1:0] Bit[3:2]: Umax[1:0] Bit[1:0]: Umin[1:0]
0x3403	FMT_CTRL3	Bit[7:0]: Vmin[9:2] (used for clipping)
0x3404	FMT_CTRL4	Bit[7:0]: Vmax[9:2] (used for clipping)
0x3405	FMT_CTRL5	Bit[7:0]: Umin[9:2] (used for clipping)
0x3406	FMT_CTRL6	Bit[7:0]: Umax[9:2] (used for clipping)
0x3407	FMT_CTRL7	Bit[7:0]: Ymin[9:2] (used for clipping)
0x3408	FMT_CTRL8	Bit[7:0]: Ymax[9:2] (used for clipping)
0x3409	FMT_CTRL9	Bit[7]: Reserved Bit[6]: dither_sel 0: Use register setting 1: Follow with FMT_CONTROL Bit[5:4]: r_dithering 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit Bit[3:2]: g_dithering 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit Bit[1:0]: b_dithering 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported, and extended features including HSYNC mode and test pattern output.

6.1.2 HSYNC mode

In this mode, the line blanking time and VSYNC to the first image line are fixed, and blank vertical dummy lines will appear. Only full size Raw/YUV format is supported.

table 6-1 DVP-related registers (sheet 1 of 2)

register address	register name	function
0x3600	DVP_CTRL00	DVP Control 00 Bit[7]: VSYNC_SEL2, DVP_VSYNC is high when frame end and low when SOF_IN Bit[6]: VSYNC_SEL 0: VSYNC is high when vertical blanking 1: VSYNC is high when image data Bit[5]: PCLK_GATE_EN 1: Gate DVP_PCLK when no data transfer Bit[4]: VSYNC_GATE, GATE DVP_PCLK when VSYNC && PCLK_GATE_EN Bit[3]: Reserved Bit[2]: PCLK_POL 1: PCLK will be reversed Bit[1]: HREF_POL 1: HREF will be reversed Bit[0]: VSYNC_POL 1: VSYNC will be reversed
0x3601	DVP_CTRL01	DVP Control 01 Bit[7:4]: Reserved Bit[3]: DATA_ORDER 0: DVP output DVP_DATA[9:0] 1: DVP output DVP_DATA[0:9] Bit[2]: DVP_H 0: Output DVP_DATA[9:0] 1: Output DVP_DATA{7:0,9:8} Bit[1]: DVP_L 0: Select DVP_DATA[9:2], when DVP 8 bit mode 1: Select DVP_DATA[7:0] Bit[0]: Reserved
0x3606	DVP_CTRL06	Bit[6]: HSYNC_NEW Bit[5]: DVP_EN Bit[4]: HSYNC_DVP_EN

table 6-1 DVP-related registers (sheet 2 of 2)

register address	register name	function
0x3607	DVP_CTRL07	User can use this register to set VSYNC width when VSYNC_SEL = 0 and VSYNC_SEL2 = 0 Bit[7:0]: VSYNC_WIDTH, VSYNC_WIDTH_REAL = VSYNC_WIDTH × 16
0x3609	DVP_CTRL09	Bit[3]: WIDTH_MAN_EN 1: Select WIDTH_MAN as output width
0x360B	DVP_CTRL0B	Bit[3]: PTN_EN, test patten enable BIt[2]: TST_BIT8 0: 10-bit mode 1: Test mode 8 bit mode Bit[1]: TST_MODE 0: Test pattern mode1 1: Test pattern mode2
0x360D ~ 0x360F	RSVD	Reserved

6.1.3 DVP timing

figure 6-1 DVP timing diagram

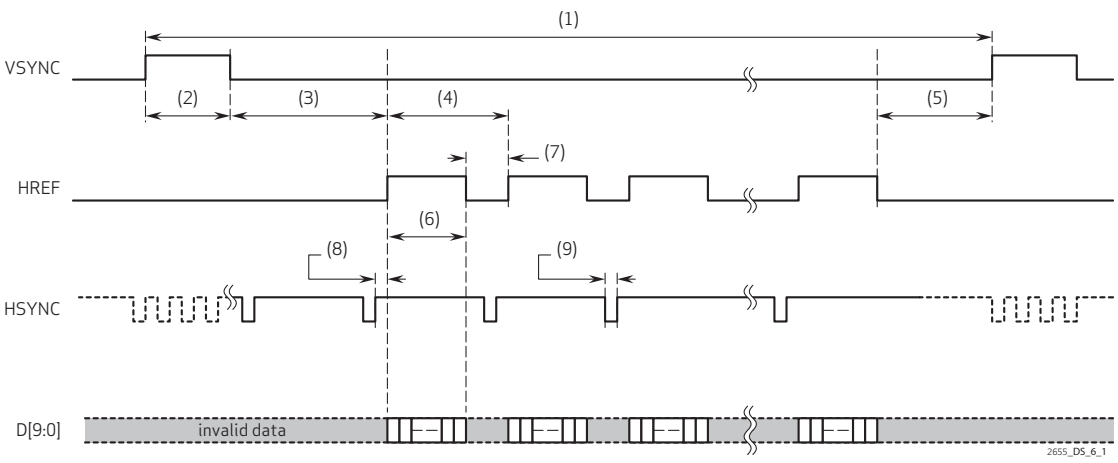


table 6-2 DVP timing specifications

mode	timing
UXGA 1600x1200	(1) 2397840 tp (2) 52413 tp (4 lines = 1940x4 = 5760 in HSYNC mode) (3) 17511 tp (4) 1940 tp (5) 256 tp (6) 1600 tp (7) 340 tp (8) 0 tp (9) 340 tp
XGA 1024x768	(1) 2397840 tp (2) 64050 tp (3) 8390 tp (4) 1940 tp (5) 256 tp (6) 1024 tp (7) 916 tp (8) n/a (9) n/a
SQCIF 128x96 (PCLK/8)	(1) 299730 tp (2) 7761 tp (3) 3737 tp (4) 2910 tp (5) 256 tp (6) 128 tp (7) 2782 tp (8) n/a (9) n/a

note
The timing values shown in **table 6-2** may vary depending upon register settings.

6.1.4 DVP image formats

6.1.4.1 YUV422 format

Uncompressed YUV422 data is sent out through DATA[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

table 6-3 YUYV format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]
odd	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]

table 6-4 UYVY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]
odd	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]

table 6-5 YVYU format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]
odd	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]

table 6-6 VYUY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]
odd	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]

6.1.4.2 YUV420 format

The data format of uncompressed YUV420 is similar to that of uncompressed YUV422 except that UV data of either even or odd lines is dropped by de-asserting PCLK.

6.1.4.3 Y8 format

Uncompressed Y8 data is sent out through DATA[9:2]. The frequency of PCLK is the same as that of raw data or half of YUV422/420.

6.1.4.4 RGB565 format

Uncompressed RGB565 data is sent out through DATA[9:2].

table 6-7 RGB565 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.4.5 RGB555 format

table 6-8 RGB555 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	0	B7	B6	B5	B4	B3

6.1.4.6 RGB444 format

The data format of uncompressed RGB444 is similar to RGB565 except that the lowest bit of R, B, and the lowest 2 bits of G are dummy bits.

table 6-9 RGB444 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	X	X	X	X	R7	R6	R5	R4
odd	G7	G6	G5	G4	B7	B6	B5	B4

6.2 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Two data lanes have full support for HS (uni-direction) and LP (bi-directional) data transfer mode. Contact your local OmniVision FAE for more details.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV2655. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

table 7-1 system control registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x3000	AGC[7:0]	0x00	RW	Auto Gain Control Bit[7:0]: Actual Gain Range from 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16)
0x3001	AGCs[7:0]	0x00	RW	Auto Gain Control Bit[7:0]: Actual Gain Range from 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) × (Bit[5]+1) × (Bit[4]+1) × (1+Bit[3:0]/16) Set Auto1[2] (0x3013[2]) = 0 to disable AGC.
0x3002	AEC[15:8]	0x00	RW	Auto Exposure Control - AEC[15:8]
0x3003	AEC[7:0]	0x01	RW	Auto Exposure Control - AEC[7:0] AEC[15:0]: Tex = Tline × AEC[15:0] Tline ≤ Tex ≤ 1 frame period Maximum exposure time will be 1 frame period even if Tex is set longer than 1 frame period. Set Auto1[0] (0x3013[0]) = 0 to disable AEC.
0x3004	AECL[7:0]	0x00	RW	Manual Extreme Bright Exposure Control - AECL[7:0] In extremely bright conditions where Tex must be less than Tline, exposure time may be set manually by this control. Tex = Tline – L1AEC[7:0] steps Tex min. ≤ Tex ≤ Tline Set Auto2[1] (0x3014[1]) = 1 to enable manual AECL.
0x3005 ~ 0x3007	RSVD	–	–	Reserved
0x300A	PIDH	0x26	R	Product ID MSBs (read only)
0x300B	PIDL	0x55	R	Product ID LSBs (read only)
0x300C	SCCB ID	0x60	RW	SCCB ID

table 7-1 system control registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x3011	CLK[7:0]	0x00	RW	Clock Rate Control Bit[7]: Digital frequency doubler 0: OFF 1: ON Bit[6]: PLL and clock divider bypass 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLK[5:0] + 1)
0x3012	SYS[7:0]	0x00	RW	Format Control Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6],[2]: Cropping QVGA Bit[5],[2]: Cropping SVGA Bit[4]: (average model, SVGA) Bit[4],[1]: (skip model, SVGA) Bit[3]: HDR model Bit[2]: Cropping option (partial sensor array) Bit[1]: Skip option (achieve data of only half of sensor array) Bit[0]: Not used

table 7-1 system control registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x3013	AUTO_1[7:0]/ ALG[143:136]	0xE7	RW	Auto Control 1 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps, slow (limited maximum exposure) 1: Big steps, fast (1/16 current exposure) Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Auto banding filter 0: Banding filter is always ON depending on if Bit[5] is low (0x3013[5]) setting 1: Automatically disable the banding filter under strong light condition Bit[3]: Extreme bright exposure control enable 0: OFF, Tline <= Tex min. 1: ON, enable minimum exposure Tex min. ≤ Tline Bit[2]: Auto gain control Auto/manual mode selection 0: Manual 1: Auto Bit[1]: Not used Bit[0]: Auto exposure control Auto/manual mode selection 0: Manual 1: Auto

table 7-1 system control registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x3014	AUTO_2[7:0]/ ALG[151:144]	0x04	RW	Auto Control 2 Bit[7]: Manually assign banding 0: 60 Hz 1: 50 Hz Bit[6]: Auto banding detection enable 0: Banding according to AUTO_2[7] (0x3014[7]) manual setting 1: Banding depending on auto 50/60 Hz detection result Bit[5]: AddLT1F in AGC Bit[4]: Freeze AEC/AGC Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2]: BDcAEC Enable banding AEC smooth switch between 50/60 Bit[1]: Manually assign extreme bright exposure enable 0: Auto exposure 1: Exposure based on LAEC[7:0] (0x3004[7:0]) steps Bit[0]: Banding filter option 0: Disable 1: Enable
0x3015	AUTO_3[7:0]/ ALG[159:152]	0x02	RW	Auto Control 3 Bit[7]: Not used Bit[6:4]: Dummy frame control 000: No dummy frame 001: Allow 1/2 dummy frame 010: Allow 1 dummy frames 011: Allow 2 dummy frames 100: Allow 3 dummy frames 101: Allow 5 dummy frames 110: Allow 7 dummy frames 111: Allow 11 dummy frames Bit[3]: Not used Bit[2:0]: AGC gain ceiling, GH[2:0]: 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x 111: 128x

table 7-1 system control registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x3016	Auto_4[7:0] / ALG[167:160	0x80	RW	Auto Control 4 Bit[7]: LGopt Low-gain option, speed up AGC to full Bit[6]: T7_opt Bit[5:4]: HLGopt[1:0] for AGC Bit[3]: AddVS_opt Bit[2]: Not used Bit[1:0]: Max exposure adjust option sub_exp[1:0] Maximum exposure time for 1 frame = Tframe - (sub_exp[1:0] x 2 + 1) x Tline
0x3017	AUTO_5[7:0]/ ALG[175:168]	0x00	RW	Auto Control 5 Bit[7]: DropF_EN 0: Disable data drop 1: Drop frame data if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range Bit[6]: Reserved Bit[5:0]: Manual banding counter
0x3018	WPT/HISH[7:0]/ alg[71:64]	0x78	RW	Luminance Signal/Histogram High Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value decreases in auto mode when average luminance/histogram is greater than WPT/HisH[7:0]
0x3019	BPT/HISL[7:0]/ alg[79:72]	0x68	RW	Luminance Signal/Histogram Low Range for AEC/AGC operation Shared by average and histogram based algorithm AEC/AGC value increases in auto mode when average luminance/histogram is less than BPT/HisL[7:0]
0x301A	VPT[7:0]/ alg[87:80]	0xD4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]

table 7-1 system control registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x301B	YAVG	0x00	RW	Luminance Average - this register will auto update Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
0x301C	AECG_MAX50/ ALG[95:88]	0x04	RW	50 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX50[5:0] 50 Hz smooth banding maximum steps
0x301D	AECG_MAX60/ ALG[103:96]	0x05	RW	60 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX60[5:0] 60 Hz smooth banding maximum steps
0x3020	HS[15:8]	0x01	RW	Horizontal Window Start 8 MSBs HS[15:0]:Horizontal start point of array, each bit represents 1 pixel
0x3021	HS[7:0]	0x18	RW	Horizontal Window Start 8 LSBs HS[15:0]:Horizontal start point of array, each bit represents 1 pixel
0x3022	VS[15:8]	0x00	RW	Vertical Window Start 8 MSBs VS[15:0]:Vertical start point of array, each bit represents 1 scan line
0x3023	VS[7:0]	0x0A	RW	Vertical Window Start 8 LSBs VS[15:0]:Vertical start point of array, each bit represents 1 scan line
0x3024	HW[15:8]	0x06	RW	Horizontal Width 8 MSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3025	HW[7:0]	0x58	RW	Horizontal Width 8 LSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3026	VH[15:8]	0x04	RW	Vertical Height 8 MSBs VH[15:0]:Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]

table 7-1 system control registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x3027	VH[7:0]	0xBC	RW	Vertical Height 8 LSBs VH[15:0]:Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3028	HTS[15:8]	0x07	RW	Horizontal Total Size 8 MSBs HTS[15:0]:Horizontal total size for 1 line
0x3029	HTS[7:0]	0x93	RW	Horizontal Total Size 8 LSBs HTS[15:0]:Horizontal total size for 1 line
0x302A	VTS[15:8]	0x04	RW	Vertical Total Size 8 MSBs VTS[15:0]:Vertical total size for 1 frame
0x302B	VTS[7:0]	0xD4	RW	Vertical Total Size 9 LSBs VTS[15:0]:Vertical total size for 1 frame
0x302C	EXHTS[7:0]	0x00	RW	Line Interval Adjustment Value (dummy pixels) Frame rate will be adjusted by changing the line interval. Each LSB will add 1/1940 Tframe to the frame period
0x302D	EXVTS[15:8]	0x00	RW	VSYNC Pulse Width 8 MSBs EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x302E	EXVTS[7:0]	0x00	RW	VSYNC Pulse Width LSB 8 bits EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x302F	RSVD	–	–	Reserved
0x3030	WEIGHT0	0x11	RW	16-Zone Average Weight Bit[7:6]: Zone 4, weight from 0 to 4 Bit[5:4]: Zone 3, weight from 0 to 4 Bit[3:2]: Zone 2, weight from 0 to 4 Bit[1:0]: Zone 1, weight from 0 to 4
0x3070	BD50[7:0]/ ALG[111:104]	0xF7	RW	50 Hz Banding 8 LSBs 50 Hz = 1 / (BD50[15:0] × Tline)
0x3071	BD50[15:8]/ ALG[119:112]	0x00	RW	50 Hz Banding 2 MSBs 50 Hz = 1 / (BD50[15:0] × Tline) Bit[7:2]: Reserved

table 7-1 system control registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x3072	BD60[7:0]/ ALG[127:120]	0xC6	RW	60 Hz Banding 2 LSBs 60 Hz = 1 / (BD60[15:0] × Tline)
0x3073	BD60[15:8]/ ALG[135:128]	0x00	RW	60 Hz Banding 2 MSBs 60 Hz = 1 / (BD60[15:0] × Tline) Bit[7:2]: Reserved
0x3076	TMC0	0x72	RW	Timing Control 0 Bit[7:2]: Reserved Bit[1]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[0]: Reserved
0x3077	TMC1	0x00	RW	Timing Control 1 Bit[7:4]: Reserved Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Reserved
0x307A	TMC4	0x00	RW	Timing Control 4 Bit[7]: Strobe function enable 0: Disable 1: Enable Bit[6]: Strobe output polarity control 0: Positive 1: Negative Bit[5:4]: Reserved Bit[3:2]: Xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines Bit[1:0]: Strobe mode select 00: Xenon mode 01: LED 1 and 2 mode 10: LED 1 and 2 mode 11: LED 3 mode
0x307C	TMC6	0x00	RW	Timing Control 6 Bit[7:2]: Reserved Bit[1]: Horizontal mirror Bit[:0]: Vertical flip

table 7-1 system control registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x307E	TMC8	0xC5	RW	Timing Control 8 Bit[7:6]: Digital gain source 00: From AGC[5:4] 01: From AGC[6:5] 1x: From AGC[7:6] Bit[5:0]: Reserved
0x3084	TMC_i2c	0x00	RW	Timing Control I2C Bit[7:1]: Not used Bit[0]: scale_div_man Manually adjust PLL control signal in scaling
0x3086	TMC10	0x00	RW	Timing Control 10 Bit[7:1]: Reserved Bit[0]: Sleep ON/OFF 0: OFF 1: ON
0x3087	TMC11	0x02	RW	Timing Control 11 Bit[7:6]: Reserved Bit[5]: Enable always do BLC 0: Disable 1: Enable Bit[4:0]: Reserved
0x3088	ISP_XOUT[15:8]	0x06	RW	ISP X-direction Output Size [15:8] Bit[7:4]: Not used Bit[3:0]: X_size_in[11:8]
0x3089	ISP_XOUT[7:0]	0x40	RW	ISP X-direction Output Size [7:0]
0x308A	ISP_YOUT[15:8]	0x00	RW	ISP Y-direction Output Size [15:8] Bit[7:3]: Not used Bit[2:0]: X_size_in[10:8]
0x308B	ISP_YOUT[7:0]	0x00	RW	ISP Y-direction Output Size [7:0]
0x308C	TMC12	0x00	RW	Timing Control 13 Bit[7]: DIS_MIPI_RW Bit[6:4]: Not used Bit[3]: grp_wr_en Bit[2:0]: Not used
0x308D	TMC13	0x00	RW	Timing Control 13 Bit[7:5]: Reserved Bit[4]: MIPI disable Bit[3:0]: Reserved
0x308F	OTP	0x80	R	OTP Internal Registers Data Read-out
0x30B0	IO_CTRL0	0x00	RW	IO Control 0 Bit[7:0]: Cy[7:0]

table 7-1 system control registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x30B1	IO_CTRL1	0x00	RW	IO Control 1 Bit[7:6]: Reserved Bit[5]: C_VSYNC Bit[4]: C_STROBE Bit[3]: C_PCLK Bit[2]: C_HREF Bit[1:0]: CY[9:8]
0x30B2	IO_CTRL2	0x00	RW	IO Control 2 Bit[7:4]: Reserved Bit[3:0]: R_PAD[3:0]

table 7-2 format registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3400	FORMAT_CTRL0		RW	FMT_CTRL00 0x00: YUV422 yuyvyuyv.../yuyvyuyv..... (data order can be adjusted by FMT_CTRL[3:0]) 0x10: YUV420 yyyyyyyy..../yuyvyuyv.... (data order can be adjusted by FMT_CTRL[3:0]) 0x20: Y8 yyyyyyy...../yyyyyyyyy.... 0x30: YUV444(RGB888): yuvyuv...../yuvyuv....(gbrgbr..../gbrgbr....) (based on rgb_sel, SC_CTRL0[1]) (data order can be adjusted by FMT_CTRL[3:0]) 0x40: RGB565 {b[4:0],g[5:3]}, {g[2:0],r[4:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x50: RGB555: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x60: RGB444 {bFMT_CTRL[3:0],1'b0,g[3:1]}, {g[0],2'h0,rFMT_CTRL[3:0],1'b0} (data order can be adjusted by FMT_CTRL[3:0]) 0x70: RGB444 {bFMT_CTRL[3:0], gFMT_CTRL[3:0]}, {rFMT_CTRL[3:0], bFMT_CTRL[3:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x80: RGB444 {4'b0,bFMT_CTRL[3:0]}, {gFMT_CTRL[3:0], rFMT_CTRL[3:0]} (data order can be adjusted by FMT_CTRL[3:0]) 0x90: Raw bgbgbg..../grgrgr..... (pixel order can be adjusted by FMT_CTRL[3:0]) 0xA0: YUV420 uyyuyyu..../vyyvyyvyy..... 0xB0: RGB555 {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} (data order can be adjusted by FMT_CTRL[3:0])

table 7-2 format registers (sheet 2 of 2)

address	register name	default value	R/W	description
				0xB0: RGB555 {b[4:0],1'b0,g[4:3]}, {g[2:0],r[4:0]} (data order can be adjusted by FMT_CTRL[3:0])
0x3401	FMT_CTRL01	0xC0	RW	Bit[7:6]: VMAX[1:0] Bit[5:4]: VMIN[1:0] Bit[3]: UV_SEL, for YUV422 or yUV420 0: Y0U_AVG,Y1,V_AVG 1: Y0U0,Y1V0 Bit[2:0]: Reserved
0x3402	FMT_CTRL02	0xCC	RW	Bit[7:6]: YMAX[1:0] Bit[5:4]: YMIN[1:0] Bit[3:2]: UMAX[1:0] Bit[1:0]: UMIN[1:0]
0x3403	FMT_CTRL03	0x00	RW	VMIN[9:2]
0x3404	FMT_CTRL04	0xFF	RW	VMAX[9:2]
0x3405	FMT_CTRL05	0x00	RW	UMIN[9:2]
0x3406	FMT_CTRL06	0xFF	RW	UMAX[9:2]
0x3407	FMT_CTRL07	0x00	RW	YMIN[9:2]
0x3408	FMT_CTRL08	0xFF	RW	YMAX[9:2]
0x3409	DITHER_CTRL0	0x40	RW	Bit[7]: Reserved Bit[6]: DITHER_SEL 0: Use register setting 1: Follow with FMT_CONTROL Bit[5:4]: R_DITHERING 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit BIt[3:2]: G_DITHERING 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit Bit[1:0]: B_DITHERING 000: Not used 001: 4-bit 010: 5-bit 011: 6-bit
0x341F~ 0x3422	RSVD	–	–	Reserved

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
stable operating temperature		0°C to +50°C
operating temperature		-20°C to +70°C
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
lead-free temperature, surface-mount process		245°C
lead-free temperature, surface-mount process		245°C

a. Exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device.

table 8-2 DC characteristics (T_A = 23°C ± 2°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.5	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
I_{DD-A}	active (operating) current		35	55	mA
I_{DD-IO}[b]			45	70	mA
$I_{DDS-SCCB}$	standby current		1	2	mA
$I_{DDS-PWDN}$			45	75	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[c]	SCL and SDA	1.26	1.8	2.3	V

a. using the internal regulator is strongly recommended for minimum power down currents

b. active current is based on sensor resolution at full size and full speed, with the MIPI function, the active current needs an additional 20mA.

c. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	setting time for hardware reset			<1	ms
	setting time for software reset			<1	ms
	setting time for UXGA/SVGA mode change			<1	ms
	setting time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27(54[a])	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

a. if using the internal clock pre-scaler

b. if using the internal PLL

figure 8-1 SCCB interface timing

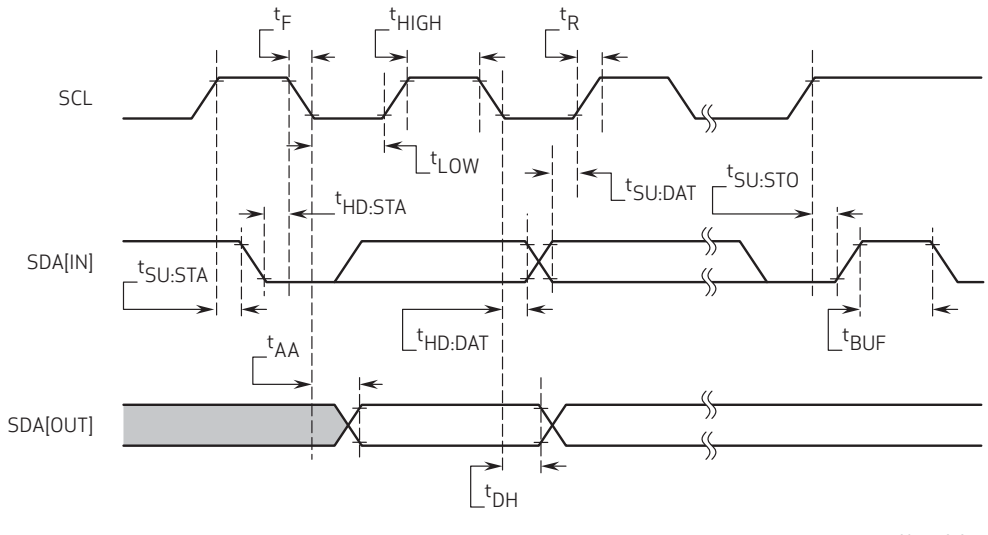


table 8-5 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400[b]	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	1.85			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. SCCB maximum speed is 400KHz when sensor master input clock (XVCLK) is greater than or equal to 13MHz. When XVCLK is less than 13MHz, the maximum SCCB speed is less than 400KHz (approximately XVCLK/32.5)

figure 8-2 line/pixel output timing

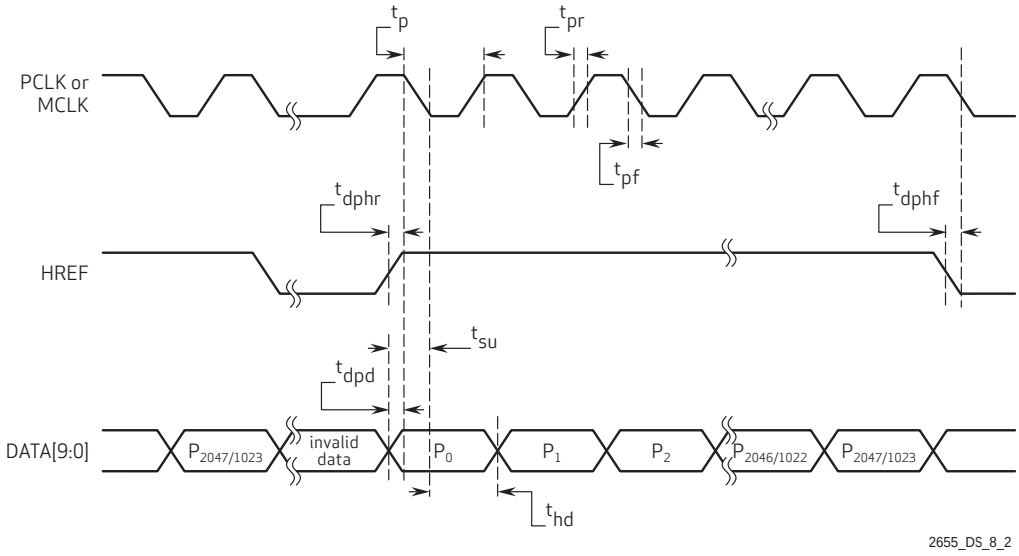


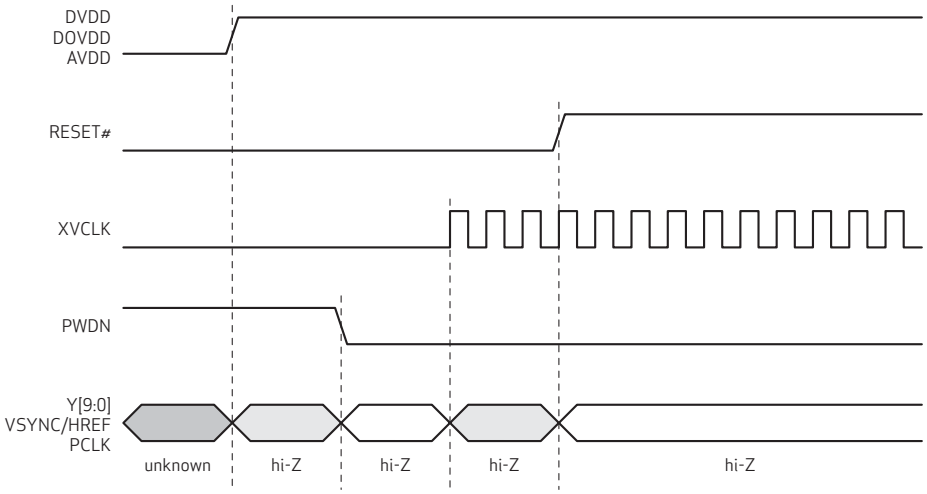
table 8-6 pixel timing specifications

symbol	parameter	min	typ	max	unit
t_p	PCLK period[a]		17.86		ns
t_{pr}	PCLK rising time[a]		2		ns
t_{pf}	PCLK falling time[a]		2		ns
t_{dphr}	PCLK negative edge to HREF rising edge		4		ns
t_{dphf}	PCLK negative edge to HREF negative edge		2		ns
t_{dpd}	PCLK negative edge to data output delay	1		4	ns
t_{su}	data bus setup time	4	6		ns
t_{hd}	data bus hold time	10	12		ns

a. PCLK running at 56 MHz, C_L = 15pF, and DOVDD = 1.8V

figure 8-3 illustrates the DVP pins status when power is turned ON.

figure 8-3 DVP state at power-on



note 1 hi-Z means IO is input pad

2655_DS_8_3

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

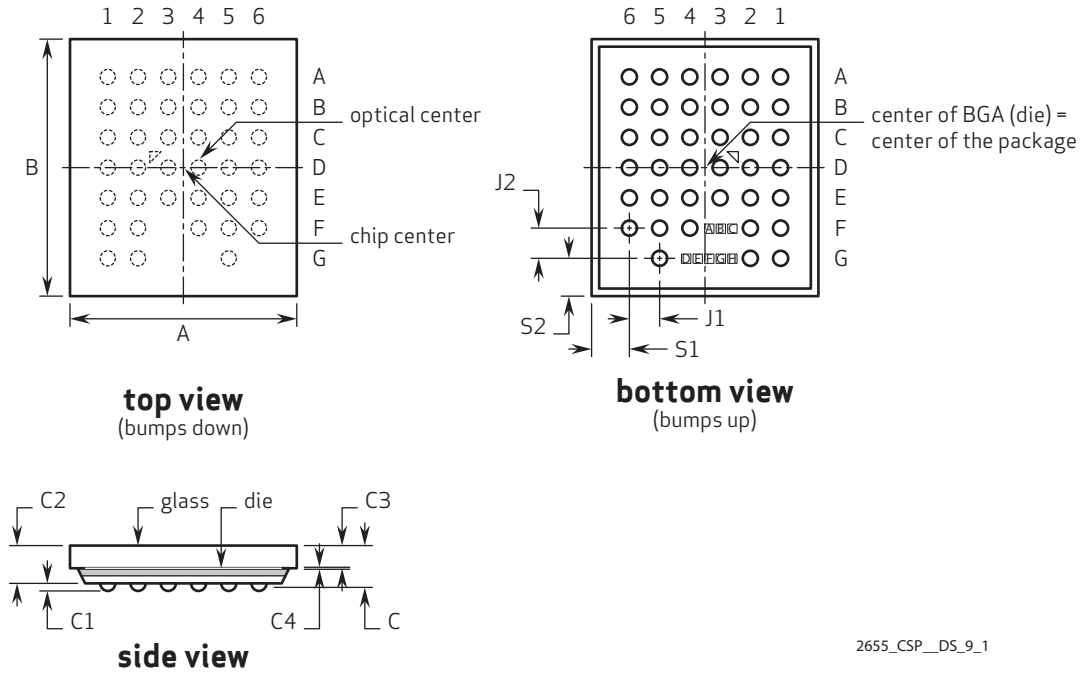


table 9-1 package dimensions (sheet 1 of 2)

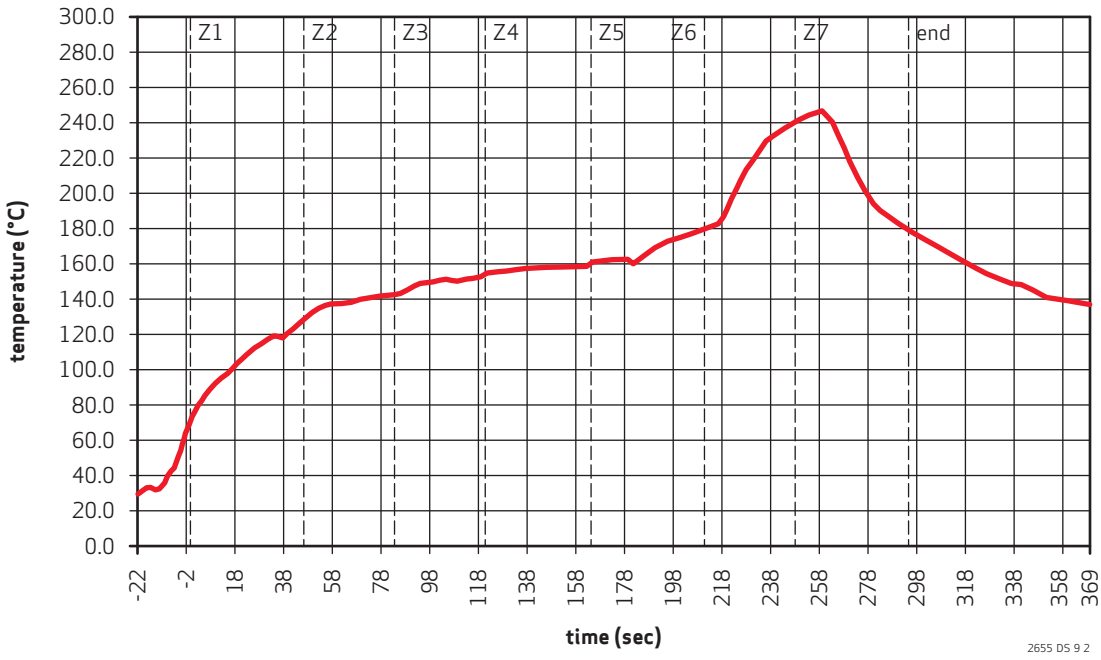
parameter	symbol	min	typ	max	unit
package body dimension x	A	4810	4835	4860	µm
package body dimension y	B	4870	4895	4920	µm
package height	C	825	885	945	µm
ball height	C1	130	160	190	µm
package body thickness	C2	680	725	770	µm
cover glass thickness	C3	390	400	410	µm
airgap between glass and sensor	C4	37	41	45	µm
ball diameter	D	270	300	330	µm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		38		
pin count x-axis	N1		6		
pin count y-axis	N2		7		
pins pitch x-axis	J1		730		µm
pins pitch y-axis	J2		600		µm
edge-to-pin center distance analog x	S1	563	593	623	µm
edge-to-pin center distance analog y	S2	618	648	678	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV2655 uses a lead free package.

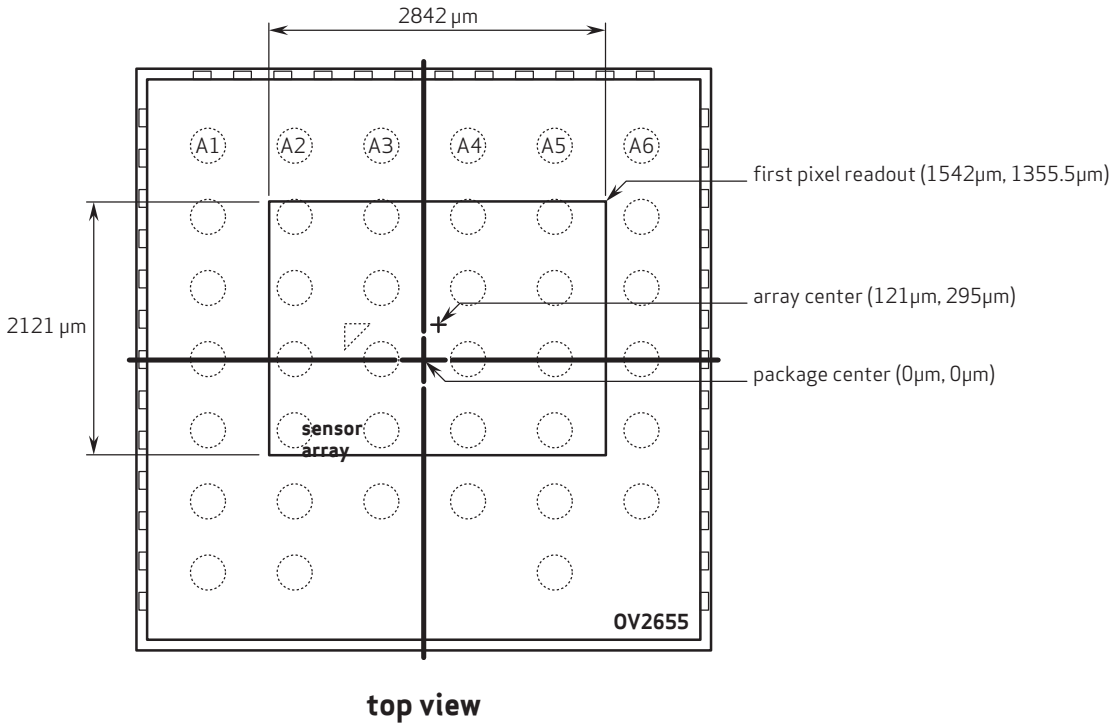
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

2655_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

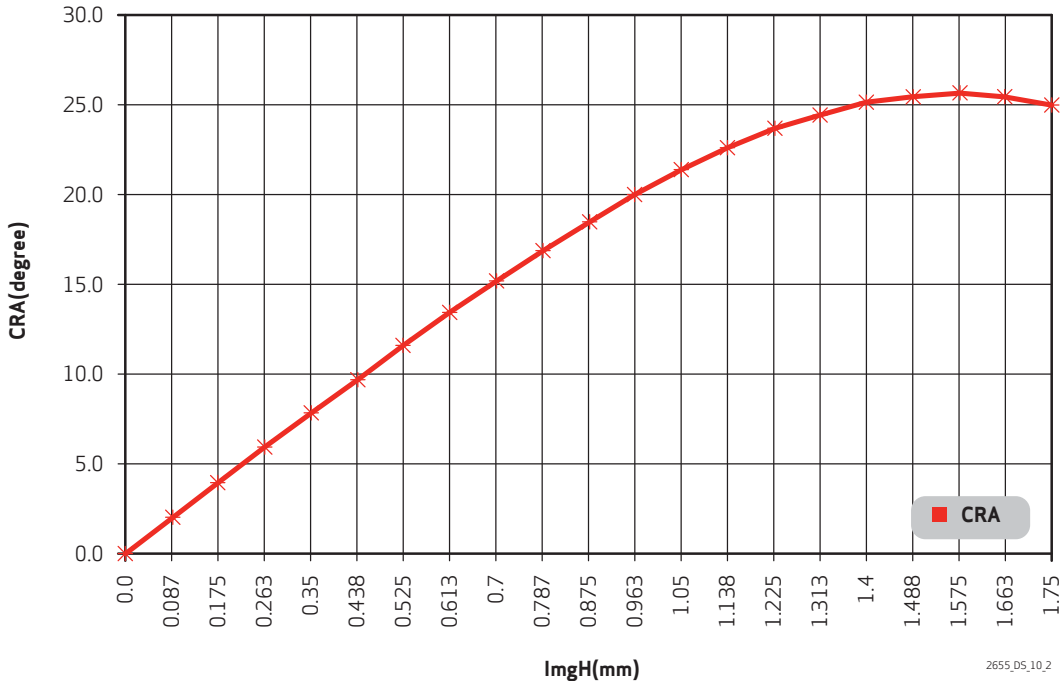


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.087	2
0.1	0.175	3.9
0.15	0.263	5.9
0.2	0.35	7.8
0.25	0.438	9.7
0.3	0.525	11.6
0.35	0.613	13.4
0.4	0.7	15.2
0.45	0.787	16.9

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	0.875	18.5
0.55	0.963	20
0.6	1.05	21.4
0.65	1.138	22.6
0.7	1.225	23.7
0.75	1.313	24.5
0.8	1.4	25.2
0.85	1.488	25.5
0.9	1.575	25.7
0.95	1.663	25.5
1	1.75	25

revision history

version 1.0 04.16.2008

- initial release

version 1.1 07.01.2008

- updated ordering information from OV02655-VL1A changed to OV02655-V38A
- under the features page, updated power requirements standby from 30 µA changed to 75 µA
- under the features page, updated S/N ratio from 38 dB changed to 37 dB
- under the features page, updated dynamic range from TBD changed to 66 dB
- under the features page, updated sensitivity from 520 mV/(Lux • sec) changed to 1030 mV/(Lux • sec)
- under the features page, updated well capacity from 9Ke changed to 7 Ke
- under the features page, updated dark current from 3 mv/s changed to 4 mV/sec @ 60°C
- under the features page, updated fixed pattern noise from 2.5e changed to 1% of $V_{PEAK\ to\ PEAK}$
- under chapter 2, removed a sentence from 2.1 overview "The OV2655 provides an anti-shake function with an internal anti-shake engine."
- under chapter 2, section 2.9 standby and sleep; from “To initiate hardware standby mode: 0x30AB=08 and 0x30AD=04 when DOVDD=1.8V; 0x30AB=00 and 0x30AD=0A when DOVDD is another voltage” changed to under chapter 2, section 2.9 standby and sleep; updated “0x30AB=00 and 0x30AD=0A when DOVDD is another voltage” changed to “To initiate hardware standby mode: 1. Set 0x30AB=00 and 0x30AD=0A; 2. Set 0x30AE = 27 and 0x363B = 01; 3.The PWDN pin must be tied to high.”
- under chapter 2, section 2.9 added power down/wake up procedure diagram.
- under chapter 8, updated table 8-1; removed abient humidity and added lead-free temperature, surface-mount process: 245°C
- under chapter 8, updated table 8-1; removed "IDD-D"
- under chapter 8, updated table 8-1; removed "IDD-D"
- under chapter 8, added notes to table 8-1; a) using the internal regulator is strongly recommended for minimum power down currents and b) active current is based on sensor resolution at full size and full speed, with the MIPI function, the active current needs an additional 20mA.
- under chapter 8, updated table 8-1; IDD-A MIN:TBD, TYP:TBD, MAX:TBD changed to TYP:35, MAX:55
- under chapter 8, updated table 8-1; IDD-IO MIN:TBD, TYP:TBD, MAX:TBD changed to TYP:45, MAX:70

version 1.2 **08.15.2008**

- under chapter 2, added figure 2-3 power on sequence diagram
- under chapter 2, updated table 2-2 by removing variopixel references
- under chapter 2, added figure 2-4 power on timing diagram
- under chapter 2, added figure 2-5 power down/ wake up sequence diagram
- under chapter 2, added figure 2-6 power down timing diagram
- under chapter 2, added figure 2-7 power off sequence diagram
- under chapter 2, added figure 2-8 power off timing diagram
- under chapter 7, updated register 0x3012[4] by removing Variopixel

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