HBDLH

HBDLH **1/1.7-Inch CMOS Digital Image Sensor**

ON Semiconductor HBDLH is a 1/1.7−inch CMOS digital image sensor with a 1928 H x 1088 V active−pixel array. This advanced image sensor captures images in either linear or line−interleaved high dynamic range, with rolling−shutter readout. HBDLH is optimized for both low light and challenging high dynamic range scene performance with 4.2 μm BSI pixels. The sensor includes flexible functions such as in−pixel binning, windowing, and both video and single frame modes. The device is programmable through a simple two−wire serial interface, and supports both MIPI and HiSPi output interfaces.

Table 1. KEY PARAMETERS

Parameter		Value
Optical Format		1/1.7 inch (9.298 mm, Diagonal)
Active Pixels		1928 (H) x1088 (V), 16:9
Pixel Size		4.2 μm x 4.2 μm BSI
Chief Ray Angle		0° (See Note)
Color Filter Array		RGB Bayer
Shutter Type		Electronic Rolling Shutter
Input Clock Range		6−50 MHz
Output Clock Maximum		80 MHz
Output Interface		4/2−lane MIPI/HiSPi
Frame Rate, 1080p		60 fps, Linear Mode 30 fps, 3−exposure line−interleaved HDR
Responsivity		58.89 Ke−/lux*s
SNR_{MAX}		41.2 dB
Maximum Dynamic Range		66 dB, Linear Mode 122 dB, 3−exposure LIM HDR , estimated
Supply Voltage	I/O	1.8 or 2.8 V
	Digital	1.2 V
	Analog	2.8 V
	MIPI	1.2 V
Power Consumption (Typical)		300 mW, 1080p 60fps Linear Mode, HiSPi 284 mW, 1080p 60fps Linear Mode, MIPI 369 mW, 1080p 30fps 3−exposure LIM HDR, HiSPi 365 mW, 1080p 30fps 3−exposure LIM HDR, MIPI
Operating Temperature		−30°C to +85°C (Junction)
Package Options		87−iBGA 12 x 9 mm

NOTE: Accommodates lens CRA up to 20°.

Features

- High Performance 4.2 μm Backside Illuminated (BSI) Pixel with DR−Pix™ Technology

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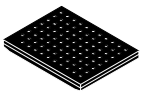


IBGA87 12 x 9
CASE 503BR

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features (continued)

- Advanced Line−Interleaved HDR with Flexible Exposure Ratio Control
- Fast Full Resolution Video Capture of 1928 x 1088 at up to 60 fps in linear mode and 30 fps in 3−exposure HDR
- Data Interfaces: 4−lane MIPI CSI−2 and HiSPi SLVS
- Selectable Automatic or User Controlled Black Level Control
- Frame to Frame Switching Among 2 Contexts to Enable Multi−function Systems
- Spread−spectrum Input Clock Support
- Multi−Camera Synchronization Support
- These are Pb−Free Devices

Applications

- “Starlight” and “Long Range View” Security Camera
- High Dynamic Range Imaging

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
HBDLHSRSC00SUEA0−DPBR	2 MP 1/1.7” Image Sensor, RGB, 0° CRA, iBGA87 Package	AR coating and protective film
HBDLHSR2C00SUEA0−DRBR	2 MP 1/1.7” Image Sensor, RGB, 0° CRA, iBGA87 Package	AR coating and No Protective Film
HBDLHSR2C00SUEAH3−GEVB	Demo3 Headboard, HiSPi/MIPI Output	Headboard

1. Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.sunnywale.com.

GENERAL DESCRIPTION

The ON Semiconductor HBDLH can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1928 x 1088 resolution image at 60 frames per second (fps). In linear mode, it outputs 12−bit raw data, using serial MIPI or HiSPi output port. In high dynamic range mode, it outputs 12−bit line−interleaved data using the MIPI or HiSPi port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID, LINE_VALID and pixel clock can be programmed to output by GPIO pins in serial mode.

The HBDLH includes additional features to allow application−specific tuning: windowing and offset, auto black level correction, and on−board temperature sensor.

Optional register information and histogram statistic information can be embedded in first and last two lines of the image frame.

The sensor is designed to operate in a wide temperature range (−30°C to +85°C Junction).

FUNCTIONAL OVERVIEW

The HBDLH is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 80 MHz. Figure 1 shows a block diagram of the sensor.

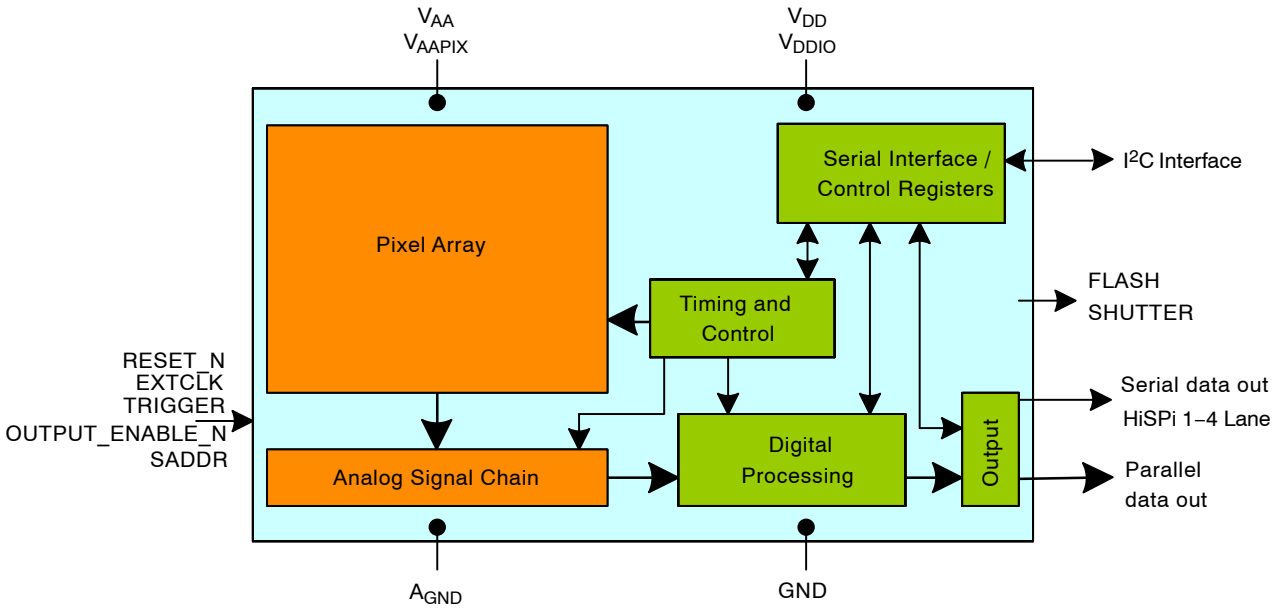


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.1 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a line−interleaved high dynamic range mode of operation where multiple images of different exposures are output separately. The off−chip ISP could combines these images into a HDR image. The pixel data are output at a rate of up to 80 MHz.

Features Overview

The HBDLH has a wide array of features to enhance functionality and to increase versatility. A summary of features follows.

- Operating Modes

  The HBDLH works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, and then generates the exposure and readout timing. The exposure time is programmed through the two−wire serial interface for both modes
- Window Control

  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations
- Context Switching

  Context switching may be used to rapidly switch between two sets of register values
- Gain

  The HBDLH can be configured for dual conversion gain, analog gain of up to 8x, and digital gain of up to 16x
- MIPI

  The HBDLH image sensor supports 4/2−line MIPI CSI−2 D−PHY
- HiSPi

  The HBDLH image sensor supports 4/2−line HiSPi SLVS
- PLL

  An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance

- Reset

  The HBDLH may be reset by a register write, or by a dedicated input pin
- Output Enable

  The HBDLH output pins may be tri−stated using dedicated register bits
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Test Patterns

  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1 s test pattern

Pixel Array

The HBDLH pixel array is configured as 1936 columns by 1096 rows (see Figures 2 and 3). The dark pixels are optically black and are used internally to monitor black level. There are 1928 columns by 1088 rows of optically active pixels. While the sensor's format is 1920 x 1080, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 967 and 968, and between Y_ADDR 547 and 548.

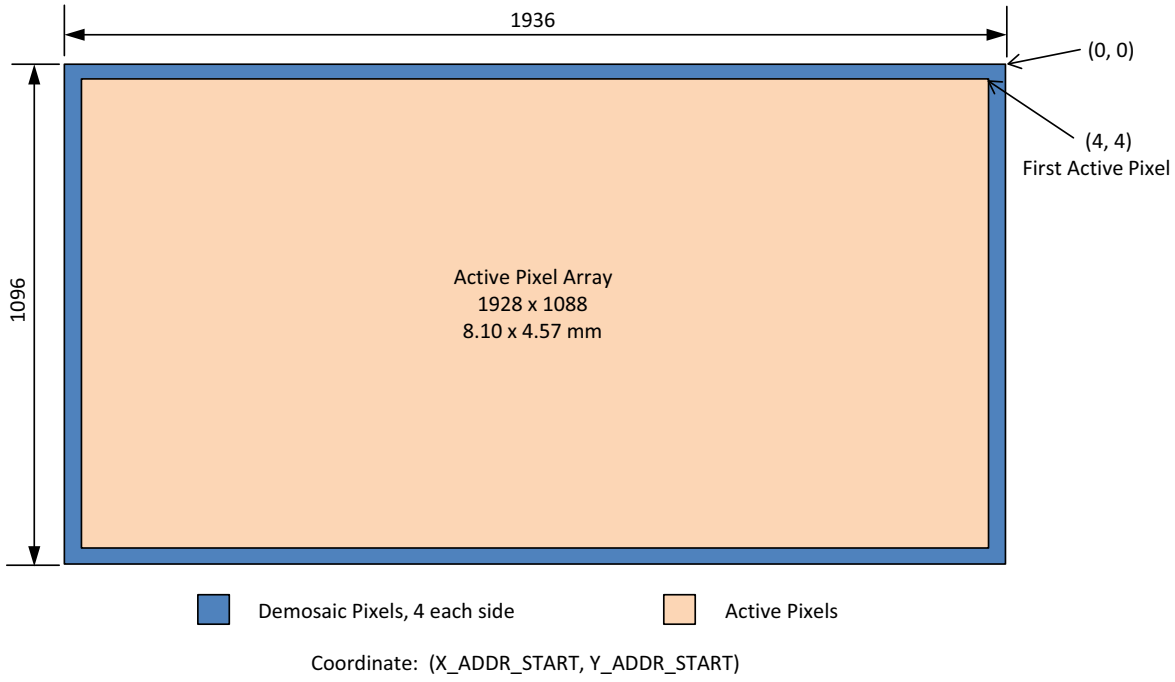


Figure 2. Pixel Array Description

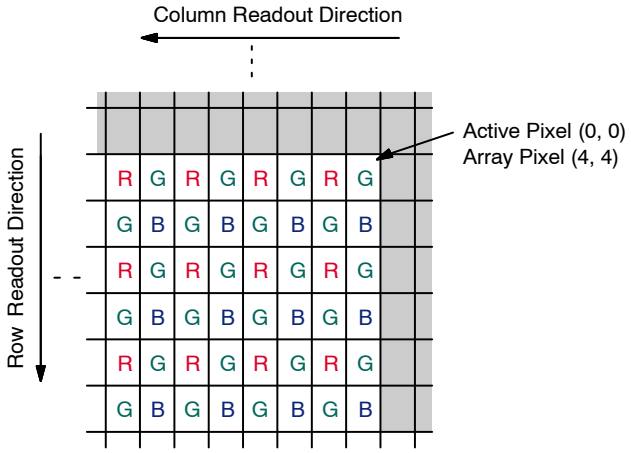


Figure 3. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 4. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 4.

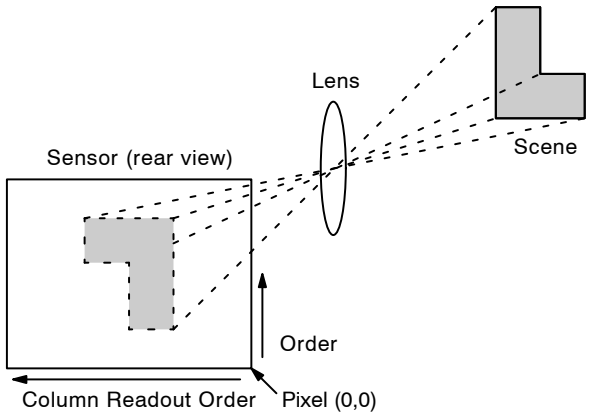
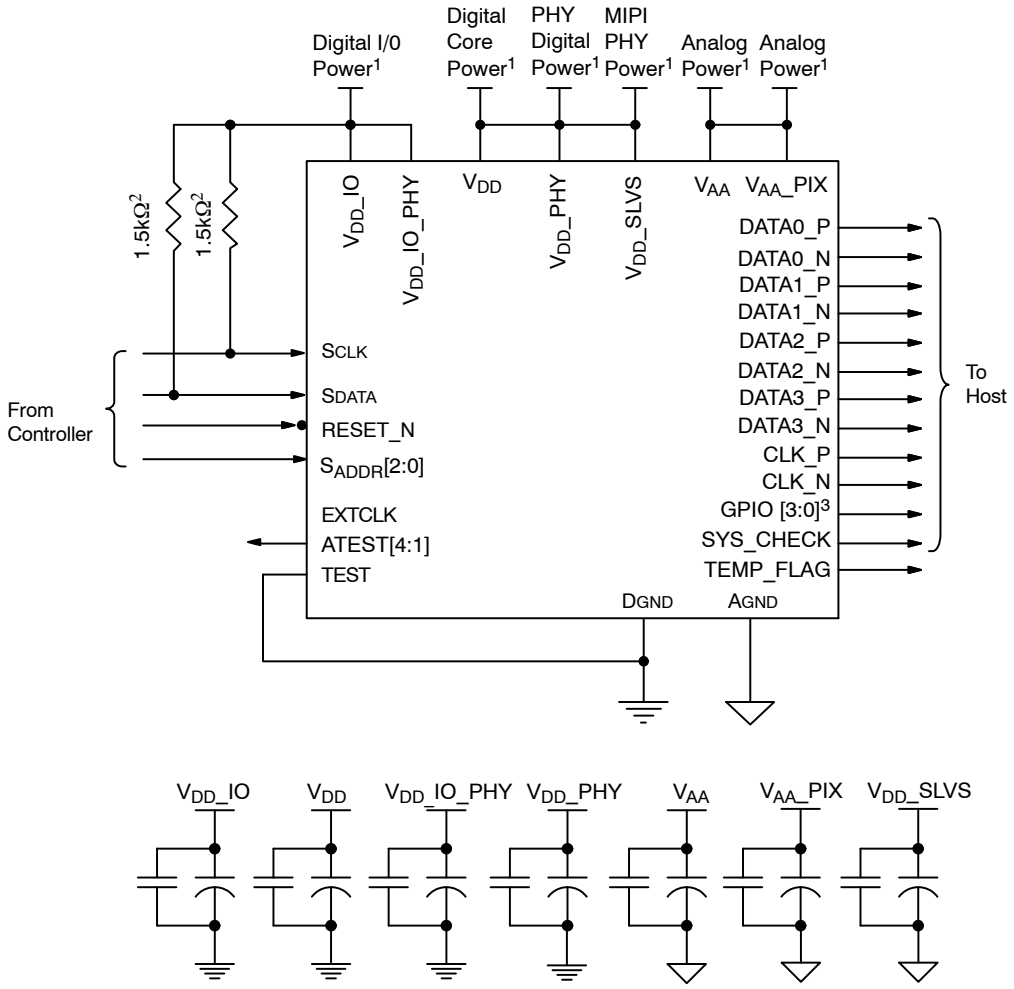


Figure 4. Imaging a Scene

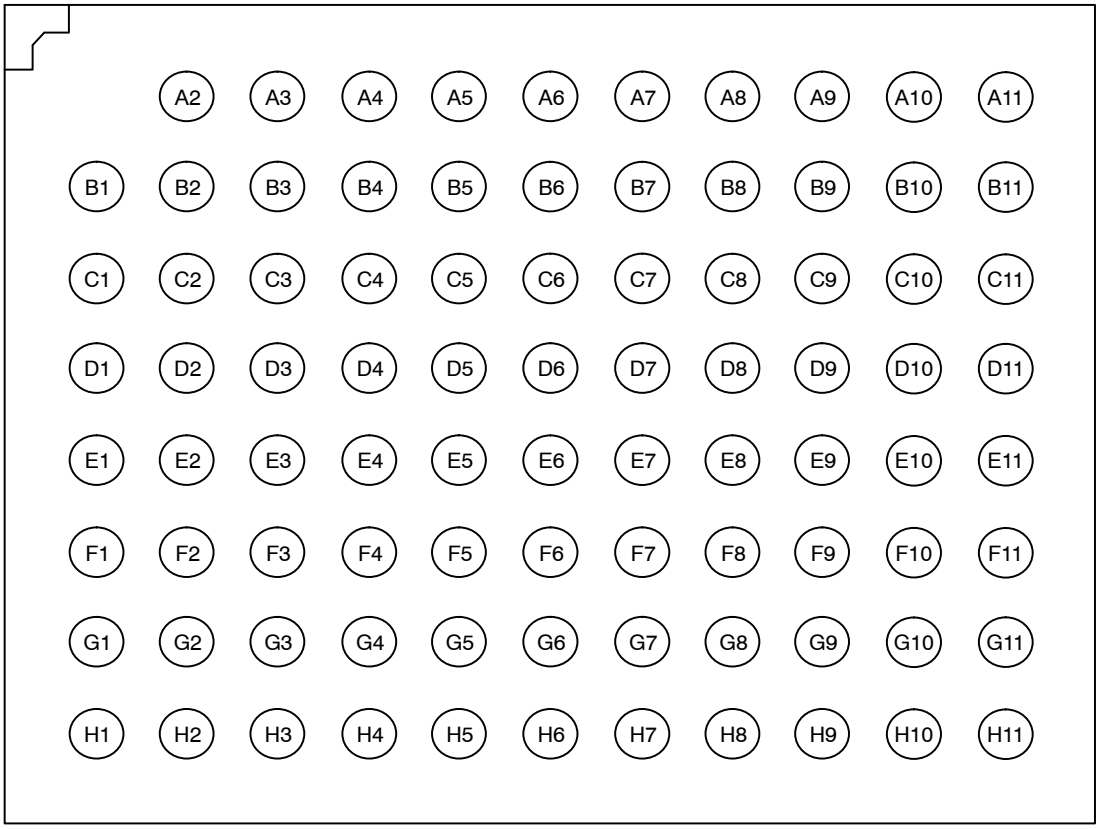
CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the HBDLH image sensor and show the package pinout.



1. All power supplies should be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. Different ATEST pins should not be tied together and should be left floating. It is recommended to have the ATEST pins brought out on the PCB and be placed as close as possible to the sensor for debug purpose.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0221 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
8. V_{AA} and V_{AA}_PIX are independent on chip but should be tied together externally.
9. Most voltage combinations of V_{DDIO}/V_{DDIO}_PHY are allowed, except V_{DD}_IO = 1V8, V_{DD}_IO_PHY = 2V8.

Figure 5. Typical Configuration: Four−Lane MIPI/HiSPi



Top View
(Ball Down)

Figure 6. 12 x 9 mm 87−Ball iBGA Package

Table 3. 87−BALL iBGA BALL MAP

	1	2	3	4	5	6	7	8	9	10	11
A		D_{GND}	VDDIO	V_{DD}	D_{GND}	D_{GND}	D_{GND}	D_{GND}	V_{DD}	V_{AA}	D_{GND}
B	V_{AA}	A_{GND}	D_{GND}	V_{DDIO}	D_{GND}	D_{GND}	ATEST3	ATEST2	ATEST1	A_{GND}	V_{AA}_PIX
C	DATA3P	DATA3N	V_{DD}	V_{DD}_SLVS	CAP_1UF_PHY	D_{GND}	D_{GND}	ATEST4	A_{GND}	A_{GND}	RESERVED
D	DATA2N	DATA2P	D_{GND}	V_{AA}_PHY	$S_{ADDR}1$	$S_{ADDR}2$	D_{GND}	SCL	SDA	D_{GND}	V_{DDIO}
E	CLKN	CLKP	V_{DD}IO_PHY	V_{DD}	GPIO_1	D_{GND}	GPIO_0	D_{GND}	$S_{ADDR}0$	V_{DDIO}	V_{DD}
F	DATA1N	DATA1P	D_{GND}	V_{DD}_PHY	RESET_N	GPIO_3	D_{GND}	GPIO_2	D_{GND}	V_{DD}	D_{GND}
G	DATA0P	DATA0N	EXTCLK	D_{GND}	SYS_CHECK	D_{GND}	TEMP_FLAG	D_{GND}	TEST	D_{GND}	V_{DDIO}
H	D_{GND}	V_{DD}IO	V_{DD}	D_{GND}	V_{DDIO}	D_{GND}	V_{DD}	D_{GND}	V_{DDIO}	V_{DD}	D_{GND}

Table 4. PIN DESCRIPTIONS, 12 x 9 mm, 87−BALL iBGA

Pin Name	Pin	Type	Description
D_{GND}	A2, A5, A6, A7, A8, A11, B3, B5, B6, C6, C7, D3, D7, D10, E6, E8, F3, F7, F9, F11, G4, G6, G8, G10, H1, H4, H6, H8, H11	Power	Digital ground
V_{DDIO}	A3, B4, D11, E10, G11, H2, H5, H9	Power	Digital I/O power. 1.8 V or 2.8 V nominal

Table 4. PIN DESCRIPTIONS, 12 x 9 mm, 87−BALL iBGA (continued)

Pin Name	Pin	Type	Description
V_{DD}	A4, A9, C3, E4, E11, F10, H3, H7, H10	Power	Core Digital power. 1.2 V nominal
V_{AA}	A10, B1	Power	Analog power. 2.8 V nominal
A_{GND}	B2, B10, C9, C10	Power	Analog ground
ATEST3	B7		Reserved, NC
ATEST2	B8		Reserved, NC
ATEST1	B9		Reserved, NC
V_{AA}_PIX	B11	Power	Analog pixel array power. 2.8 V nominal
DATA3P	C1	Output	Differential MIPI/HiSPi serial data lane 3
DATA3N	C2	Output	Differential MIPI/HiSPi serial data lane 3
V_{DD}_SLVS	C4	Power	Reference voltage for HiSPi serial interface. 1.2 V nominal
CAP_1UF_PHY	C5	Power	external bypass capacitor for MIPI Regulator
ATEST4	C8	I/O	NC in normal operation
RESERVED	C11		Reserved, NC
DATA2N	D1	Output	Differential MIPI/HiSPi serial data lane 2
DATA2P	D2	Output	Differential MIPI/HiSPi serial data lane 2
V_{AA}_PHY	D4	Power	Analog MIPI/HiSPi power. 2.8 V nominal
$S_{ADDR}1$	D5	Input	Serial interface device ID select
$S_{ADDR}2$	D6	Input	Serial interface device ID select
SCL	D8	Input	Serial clock for access to control and status registers.
SDA	D9	I/O	Serial data for reads from and writes to control and status registers
CLKN	E1	Output	Differential MIPI/HiSPi serial clock
CLKP	E2	Output	Differential MIPI/HiSPi serial clock
V_{DDIO}_PHY	E3	Power	Power to MIPI and HiSPi PHYs. 1.8 V nominal
GPIO_1	E5	I/O	GPIO pin
GPIO_0	E7	I/O	GPIO pin
$S_{ADDR}0$	E9	Input	Serial interface device ID select
DATA1N	F1	Output	Differential MIPI/HiSpi serial data lane 1
DATA1P	F2	Output	Differential MIPI/HiSPi serial data lane 1
V_{DD}_PHY	F4	Power	PHY Digital power. 1.2 V nominal
RESET_N	F5	Input	Asynchronous active−low reset. When low, the sensor asynchronously resets
GPIO_3	F6	I/O	GPIO pin
GPIO_2	F8	I/O	GPIO pin
DATA0P	G1	Output	Differential MIPI/HiSPi serial data lane 0
DATA0N	G2	Output	Differential MIPI/HiSPi serial data lane 0
EXTCLK	G3	Input	Master input clock. PLL input clock. 6 ~ 50 MHz
SYS_CHECK	G5	Output	Combined OR of all error flags
TEMP_FLAG	G7	Output	Temperature monitoring flag
TEST	G9	Input	Tied to GND for normal operation

Power−Up Sequence

The available power supplies (VDD_IO, VDD, VDD_SLVS, VAA, VAA_PIX) must have the separation specified below.

10. Turn on VAA and VAA_PIX power supply
11. After 100 μs, turn on VDD_IO power supply
12. After 100 μs, turn on VDDIO_PHY(1.8 V) power supply
13. After 100 μs, turn on VDD power supply
14. After 100 μs, turn on VDD_SLVS power supply
15. After the last power supply is stable, enable EXTCLK
16. Assert RESET_N for at least 1 ms. The parallel interface will be tri−stated during this time
17. Wait for ~150000 EXTCLKs for internal initialization into soft standby where M3ROM and full OTPM upload would be complete
18. Set streaming mode (mode_select/stream (R0x301A[2]) = 1) and the internal PLL would be enabled (not locked yet)
19. Wait for 1 ms for PLL lock to complete, part will then go into streaming mode

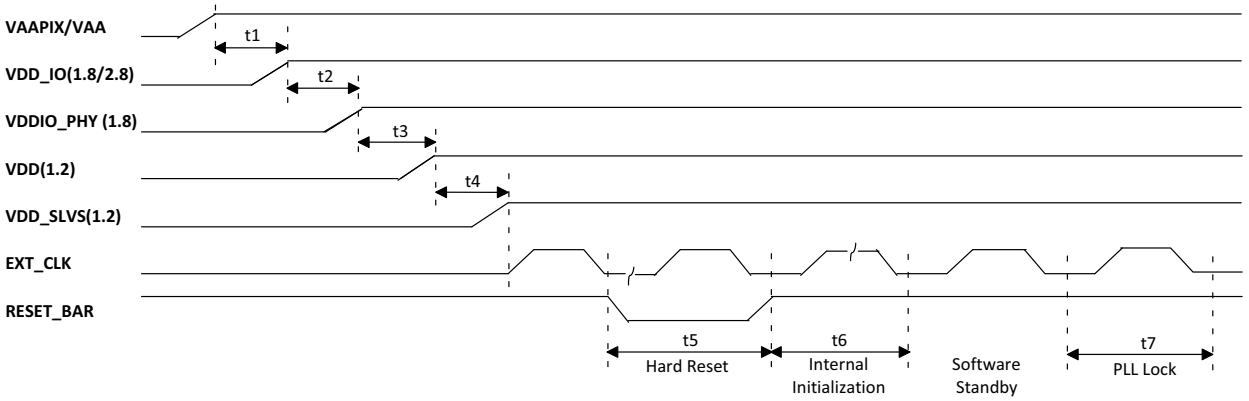


Figure 7. Power−Up Sequence

Table 5. POWER−UP SEQUENCE

SN	Definition	Symbol	Min	Typ	Max
1	VAA/VAA_PIX to VDD_IO (Note 2)	t1	0	100 μs	–
2	VDD_IO to VDDIO_PHY	t2	0	100 μs	–
3	VDDIO_PHY to VDD	t3	0	100 μs	–
4	VDD to VDD_SLVS (Note 3)	t4	0	100 μs	–
5	Xtal Settle Time (Component Dependent)	tx	–	30 ms	–
6	Hard Reset	t5	1 ms	–	–
7	Internal Initialization	t6	150000 ext clk cycles	–	–
8	PLL Lock Time	t7	1 ms	–	–

2. V_{DD}_IO if 2.8 V can be tied together with V_{AA}/V_{AA}PIX (t1 becomes ‘0’ in this case).
3. V_{DD} and V_{DD}_SLVS can be tied together (t4 becomes ‘0’ in this case).

Power Down Sequence

Here is the description:

The available power supplies (V_{DD}_IO, V_{DD}, V_{DDIO}_PHY, V_{DD}_SLVS, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301A[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended
3. Turn off V_{DD}_SLVS
4. Turn off V_{DD}/V_{DD}_IO_PHY*
5. Turn off V_{DD}_IO
6. Turn off V_{AA}/V_{AA}_PIX

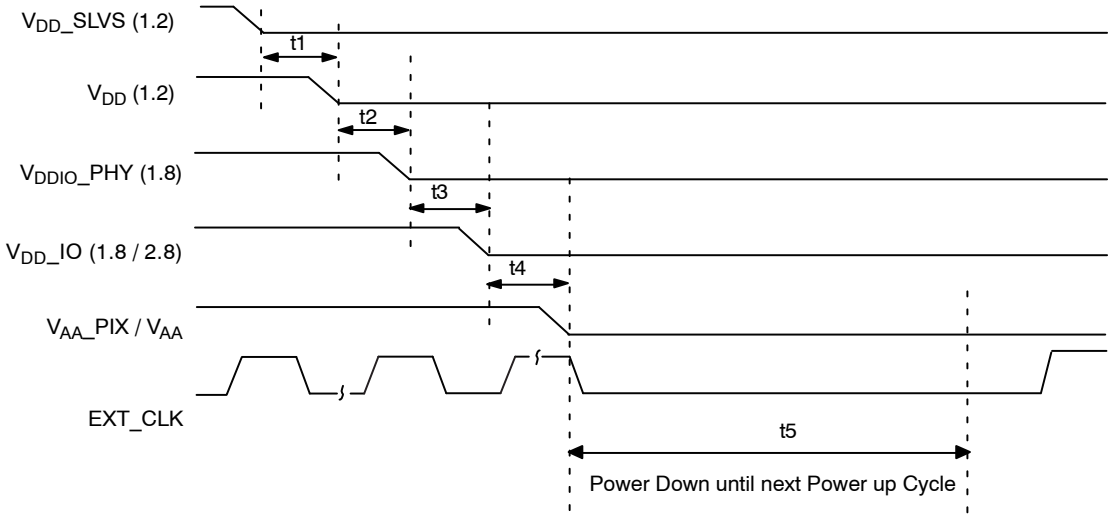


Figure 8. Power Down Sequence

Table 6. POWER−DOWN SEQUENCE

SN	Definition	Symbol	Min	Typ	Max
1	VDD_SLVS to VDD (Note 4)	t1	0	–	–
2	VDDIO_PHY (1.8)	t2	0	–	–
3	VDDIO_PHY to VDD_IO	t3	0	–	–
4	VDD_IO to VAA/VAA_PIX (Note 5)	t4	0	–	–
5	PwrDn until Next Pwrup Time	t5	100 ms	–	–

4. V_{DD} and V_{DD}_SLVS can be tied together
5. V_{DD}_IO If 2.8 V can be tied together with V_{AA}/VAA_PIX

TWO-WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the HBDLH. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW−the interface protocol determines which device is allowed to drive S_{DATA} at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive S_{CLK} LOW; the HBDLH uses S_{CLK} as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

1. A (repeated) start condition
2. A slave address/data direction byte
3. An (a no) acknowledge bit
4. A message byte
5. A stop condition

The bus is idle when both S_{CLK} and S_{DATA} are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on S_{DATA} while S_{CLK} is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on S_{DATA} while S_{CLK} is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the HBDLH are 0x20 (write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the S_{ADDR} [2:0] inputs.

Table 7. DEVICE SLAVE ADDRESS AND SADDR PINS

SADDR2	SADDR1	SADDR0	Device Address	Register
0	0	0	0x20	R0x3420[7:0]
0	0	1	0x30	R0x3420[15:8]
0	1	0	0x6C	R0x3422[7:0]
0	1	1	0x6E	R0x3422[15:8]
1	0	0	0x40	R0x3424[7:0]
1	0	1	0x50	R0x3424[15:8]
1	1	0	0x60	R0x3426[7:0]
1	1	1	0x70	R0x3426[15:8]

Note:
6. The defaut device slave address is 0x20, which is implemented by having all SADDR pins grounded.
7. After power up, device slave address in registers, R0x3420, 3422, and 3424 could be configured to other address.
8. The device slave addresses in R0x3426 are hard−coded and could not be changed.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the S_{CLK} clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases S_{DATA}. The receiver indicates an acknowledge bit by driving S_{DATA} LOW. As for data transfers, S_{DATA} can change when SCLK is LOW and must be stable while S_{CLK} is HIGH.

No Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive S_{DATA} LOW during the S_{CLK} clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 9) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 9 shows how the internal register address maintained by the HBDLH is loaded and incremented as the sequence proceeds.

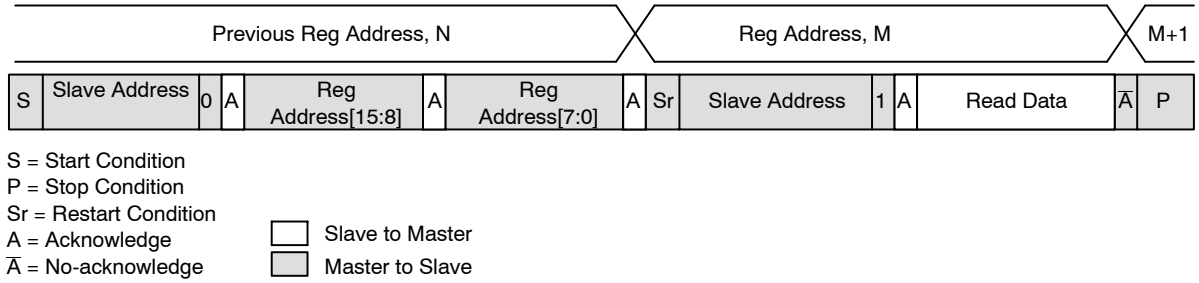


Figure 9. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 10) performs a read using the current value of the HBDLH internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

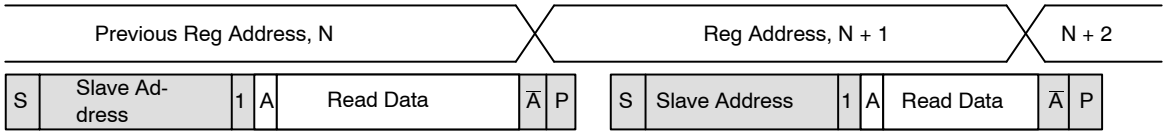


Figure 10. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 11) starts in the same way as the single READ from random location (Figure 9). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

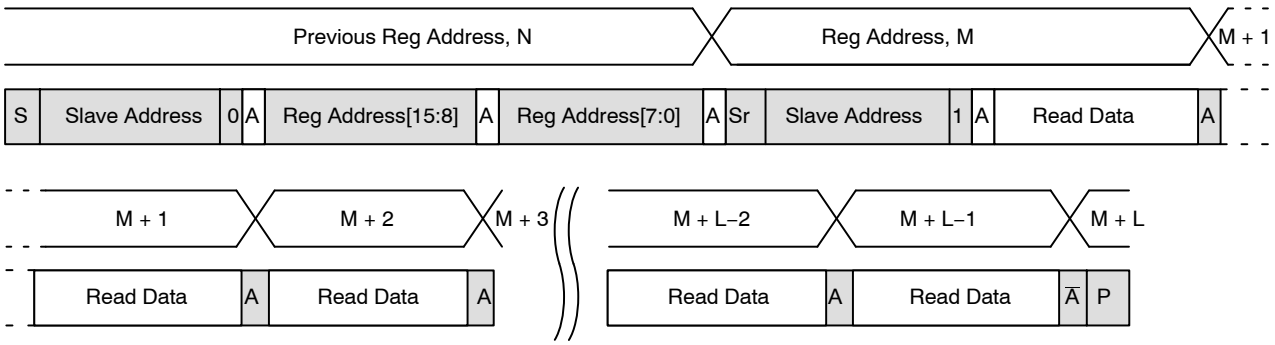


Figure 11. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 12) starts in the same way as the single READ from current location (Figure 10). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

Figure 12. Sequential READ, Start from Current Location

Single Write to Random Location

This sequence (Figure 13) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

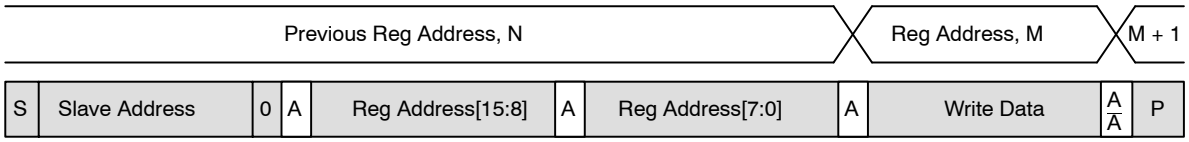


Figure 13. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 14) starts in the same way as the single WRITE to random location (Figure 13). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

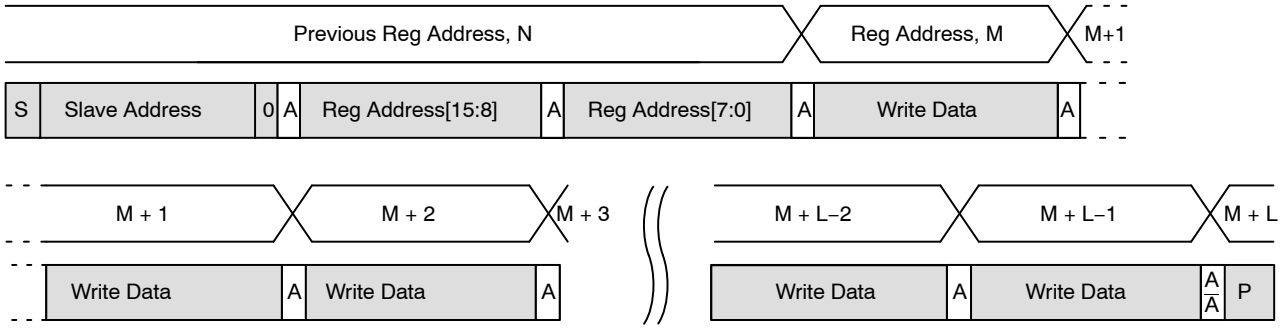


Figure 14. Sequential WRITE, Start at Random Location

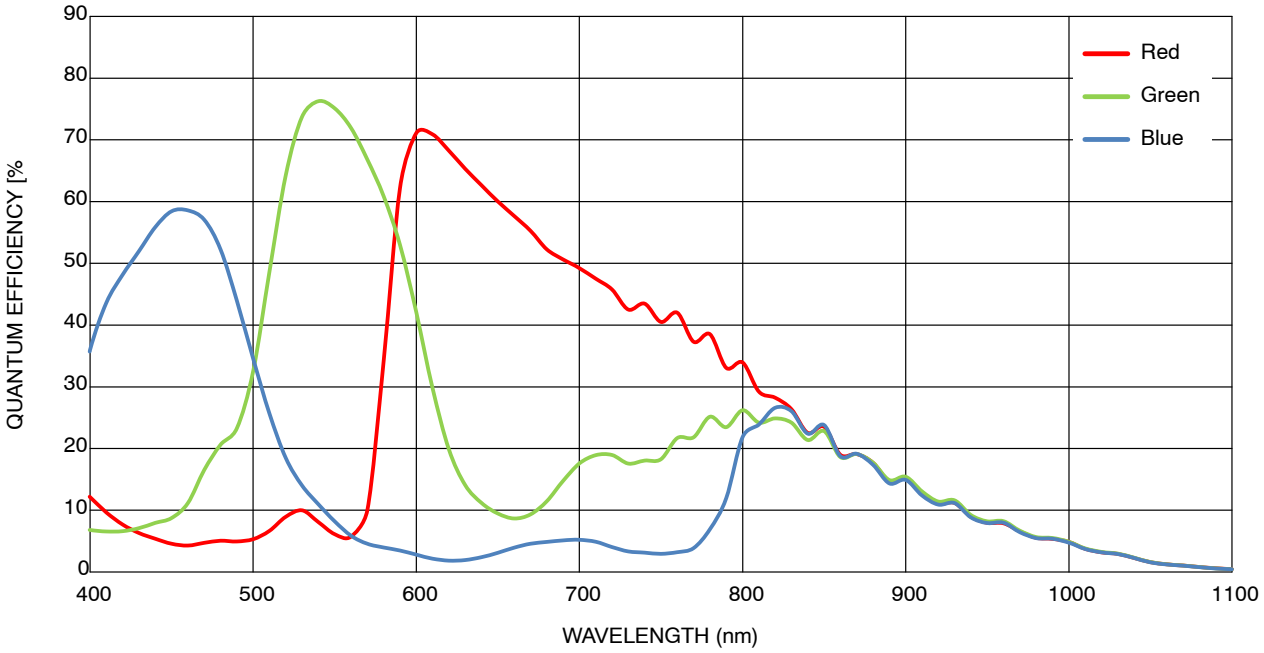


Figure 15. Quantum Efficiency

ELECTRICAL SPECIFICATIONS

Table 8. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
V_{AA}_MAX	Analog Voltage		–0.3	4	V
V_{AA}_PIX	Pixel Supply Voltage		–0.3	4	V
V_{DD}_IO_MAX	I/O Digital Voltage		–0.3	4	V
V_{DD}_IO_PHY	Power to MIPI		–0.3	2.4	V
V_{DD}_MAX	Core Digital Voltage		–0.3	2.4	V
V_{DD}_SLVS_MAX	HiSPi I/O Digital Voltage		–0.3	2.4	V
^{t}ST	Storage Temperature		–40	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 9. OPERATING CONDITIONS

Symbol	Definition	Min	Typ	Max	Unit
V_{AA}	Analog Power	2.6	2.8	3	V
V_{AA}_PIX	Analog Pixel Voltage	2.6	2.8	3	
V_{AA}_PHY	Power to MIPI	2.6	2.8	3	
V_{DDIO}	IO Power	1.7/2.6	1.8/2.8	1.9/3	
V_{DDIO}_PHY	Power to MIPI	1.7	1.8	1.9	
V_{DD}	Digital Power	1.14	1.2	1.26	
V_{DD}_PHY	Power to MIPI	1.14	1.2	1.26	
V_{DD}_SLVS	SLVS PHY Power	1.14	1.2	1.26	

Table 10. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
VIH	Input HIGH Voltage		VDD_IO x 0.7	–	–	V
VIL	Input LOW Voltage		–	–	VDD_IO x 0.3	V
IIN	Input leakage Current	No Pull−up Resistor; VIN = VDD_IO or DGND	–	–	20	μA
VOH	Output HIGH Voltage		VDD_IO – 0.3	–	–	V
VOL	Output LOW Voltage		–	–	0.4	V
IOH	Output HIGH Current	At Specified VOH	10	–	30	mA
IOL	Output LOW Current	At Specified VOL	10	–	30	mA

Table 11. OPERATING CURRENT CONSUMPTION

T_J = 55°C (±35°C), V_{AA} = V_{AA}_PIX = 2.8 V, V_{DD} = V_{DD}_PHY = V_{DD}_SLVS = 1.2 V, V_{DD}_IO = V_{DDIO}_PHY = 2.8 V − ANALOG GAIN 1X LCG

Conditions	Symbol	Min	Typ	Max	Unit
1080p30 Linear 74.7 MHz HiSPi SLVS	IAA	−	36.14	90	mA
	IAA_PIX		6.54	30	
	IDDIO	−	0.18	10	
	IDDIO_PHY	−	6.29	30	
	IDD		109.34	200	
	IDD_PHY		10.28	30	
	IDD_SLVS	−	11.15	25	
	Power	−	295	754	mW
1080p60 Linear 74.7 MHz HiSPi SLVS	IAA	−	36.15	90	mA
	IAA_PIX		6.55	30	
	IDDIO	−	0.17	10	
	IDDIO_PHY	−	7.39	30	
	IDD	−	110.95	200	
	IDD_PHY		10.27	30	
	IDD_SLVS		11.37	25	
	Power	−	300	754	mW
1080p30 Linear 74.7 MHz MIPI	IAA	−	36.1	90	mA
	IAA_PIX		6.54	30	
	IDDIO	−	0.17	10	
	IDDIO_PHY	−	5.29	30	
	IDD	−	101.19	200	
	IDD_PHY		8.08	30	
	IDD_SLVS		5.09	25	
	Power	−	272	754	mW
1080p60 Linear 74.7 MHz MIPI	IAA	−	36.15	90	mA
	IAA_PIX		6.54	30	
	IDDIO	−	0.17	10	
	IDDIO_PHY	−	6.61	30	
	IDD	−	105.14	200	
	IDD_PHY		8.95	30	
	IDD_SLVS		7.36	25	
	Power	−	284	754	mW
1080p30 Line−Interleaved 72 MHz HiSPi SLVS	IAA	−	49.98	90	mA
	IAA_PIX		9.73	30	
	IDDIO	−	0.18	10	
	IDDIO_PHY	−	9.01	30	
	IDD	−	124.81	300	
	IDD_PHY		10.49	30	
	IDD_SLVS		11.68	25	
	Power	−	369	754	mW

Table 11. OPERATING CURRENT CONSUMPTION (continued)
T_J = 55°C (±35°C), V_{AA} = V_{AA}_PIX = 2.8 V, V_{DD} = V_{DD}_PHY = V_{DD}_SLVS = 1.2 V, V_{DD}_IO = V_{DDIO}_PHY = 2.8 V − ANALOG GAIN 1X LCG

Conditions	Symbol	Min	Typ	Max	Unit
1080p30 Line−Interleaved 72 MHz MIPI	IAA	−	49.96	90	mA
	IAA_PIX		9.72	30	
	IDDIO	−	0.17	10	
	IDDIO_PHY	−	8.58	30	
	IDD	−	124	200	
	IDD_PHY		10.19	30	
	IDD_SLVS		10.5	25	
	Power	−	365	754	mW

Table 12. I/O TIMING CHARACTERISTICS (2.8 V V_{DD}_IO) (Note 9)

Symbol	Definition	Condition	V_{DD}_IO = 2.8 V			Unit
			Min	Typ	Max	
f_{EXTCLK}	Input clock frequency	PLL Enabled	6	−	50	MHz
t_{EXTCLK}	Input clock period	PLL Enabled	20	−	166	ns
t_R	Input clock rise time		−	3	−	ns
t_F	Input clock fall time		−	3	−	ns
t_{JITTER}	Input clock jitter		−	−	100	ps

9. All values are taken at the 50% transition point. The loading used is 20 pF.

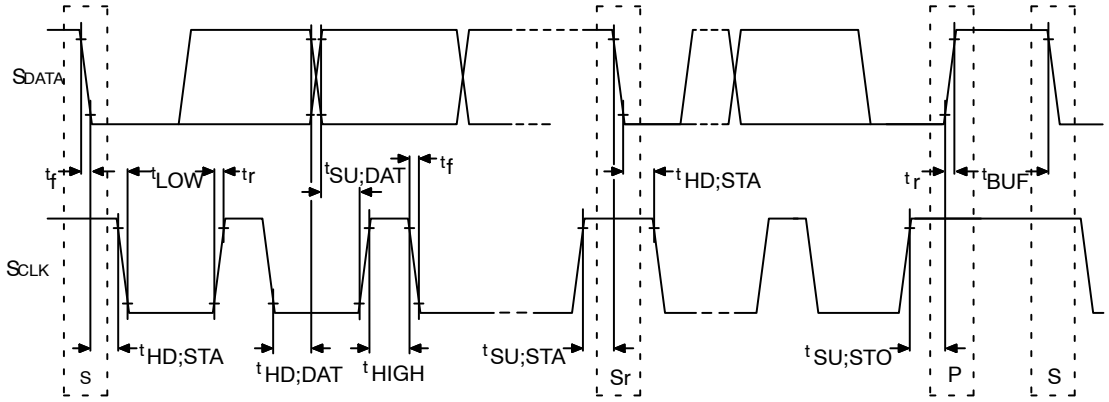
Table 13. I/O TIMING CHARACTERISTICS (1.8 V V_{DD}_IO) (Note 10)

Symbol	Definition	Condition	V_{DD}_IO = 1.8 V			Unit
			Min	Typ	Max	
f_{EXTCLK}	Input clock frequency	PLL Enabled	6	−	50	MHz
t_{EXTCLK}	Input clock period	PLL Enabled	20	−	166	ns
t_R	Input clock rise time		−	3	−	ns
t_F	Input clock fall time		−	3	−	ns
t_{JITTER}	Input clock jitter		−	−	100	ps

10. All values are taken at the 50% transition point. The loading used is 20 pF.

Two-Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 16 and Table 14.



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 16. Two-Wire Serial Bus Timing Parameters

Table 14. TWO−WIRE SERIAL BUS CHARACTERISTICS

f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = V_{DD}_SLVS = 1.2 V; V_{DD}_IO = V_{DD}_IO_PHY = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
M_SCLK Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
SCLK High		8 * EXTCLK + SCLK rise time		8 * EXTCLK + SCLK rise time		8 * EXTCLK + SCLK rise time		μs
SCLK Low	f_{SCL}	6 * EXTCLK + SCLK rise time		6 * EXTCLK + SCLK rise time		6 * EXTCLK + SCLK rise time		μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	–	0.26	–	μs
LOW period of the SCLK clock	t_{LOW}	4.7	–	1.2	–	0.5	–	μs
HIGH period of the SCLK clock	t_{HIGH}	4	–	0.6	–	0.26	–	μs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	μs
Data hold time	$t_{HD;DAT}$	0 (Note 14)	3.45 (Note 15)	0 (Note 14)	0.9 (Note 15)	0	–	μs
Data set−up time	$t_{SU;DAT}$	250	–	100 (Note 16)	–	50	–	ns
Rise time of both SDATA and SCLK signals	t_r	–	1000	20 + 0.1Cb (Note 17)	300	–	120	ns
Fall time of both SDATA and SCLK signals	t_f	–	300	20 + 0.1Cb (Note 17)	300	–	120	ns
Set−up time for STOP condition	$t_{SU;STO}$	4	–	0.6	–	0.26	–	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	–	550	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	–	3.3	pF

Table 14. TWO−WIRE SERIAL BUS CHARACTERISTICS (continued)

f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = V_{DD}_SLVS = 1.2 V; V_{DD}_IO = V_{DD}_IO_PHY = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SDATA max load capacitance	C_{LOAD_SD}	−	30	−	30	−	30	pF
SDATA pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

11. This table is based on i2c−bus specification.
12. Two−wire control is I2C−compatible.
13. All values referred to VIHmin = 0.7 VDD and VILmax = 0.3 VDD levels. Sensor EXCLK = 27 MHz.
14. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
15. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCLK signal.
16. A Fast−mode I2C−bus device can be used in a Standard−mode I2C−bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I2C−bus specification) before the SCLK line is released.
17. Cb = total capacitance of one bus line in pF.

MIPI Electrical Specifications

The ON Semiconductor HBDLH sensor supports four lanes of MIPI data. Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.0
- MIPI Alliance Standard for D−PHY version 1.1

MIPI AC AND DC ELECTRICAL CHARACTERISTICS

Table 15. MIPI HIGH−SPEED TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	HS transmit differential voltage	140	–	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	–	250	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential−1 or Differential−0	–	–	14	mV
$\Delta V_{CMTX}(1,0)$	V_{CMTX} mismatch when output is Differential−1 or Differential−0	–	–	5	mV
V_{OHHS}	HS output HIGH voltage	–	–	360	mV
Z_{OS}	Single−ended output impedance	40	–	62.5	Ω
ΔZ_{OS}	Single−ended output impedance mismatch	–	–	10	%

Table 16. MIPI HIGH−SPEED TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate	–	–	600	Mb/s
Data Lane t_{rise}	20–80% rise time	100	–	500	ps
Data Lane t_{fall}	20–80% fall time	100	–	500	ps
Clock Lane t_{rise}	20–80% rise time	150	–	500	ps
Clock Lane t_{fall}	20–80% fall time	150	–	500	ps

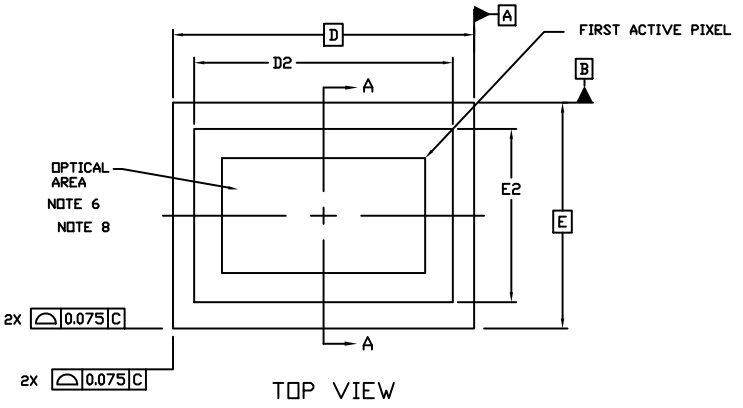
Table 17. MIPI LOW−POWER TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Thevenin output low level	–	–	50	mV
V_{OH}	Thevenin output high level	1.1	1.15	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110	–	–	

Table 18. MIPI LOW−POWER TRANSMITTER AC CHARACTERISTICS

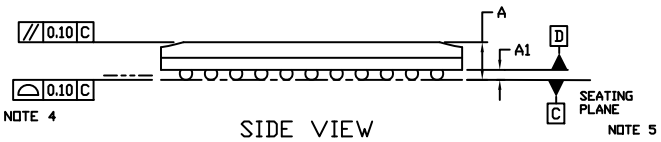
Symbol	Parameter	Min	Typ	Max	Unit
t_{rise}	15–85% rise time	–	–	25	ns
t_{fall}	15–85% fall time	–	–	25	ns
Slew	Slew rate (C_{LOAD} 5–20 pF)	–	–	250	mV/ns
Slew	Slew rate (C_{LOAD} 20–70 pF)	–	–	150	mV/ns

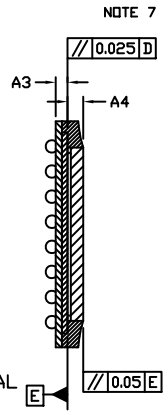
IBGA87 12x9
CASE 503BR
ISSUE A



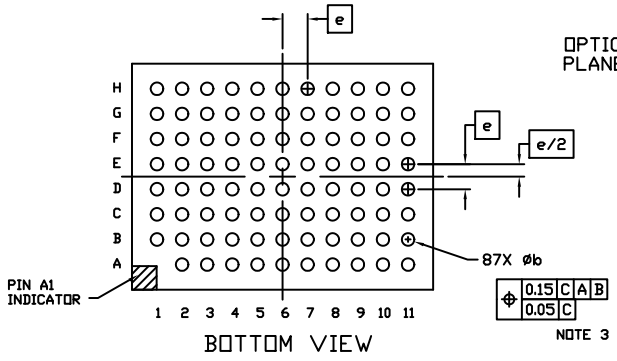
NOTES:

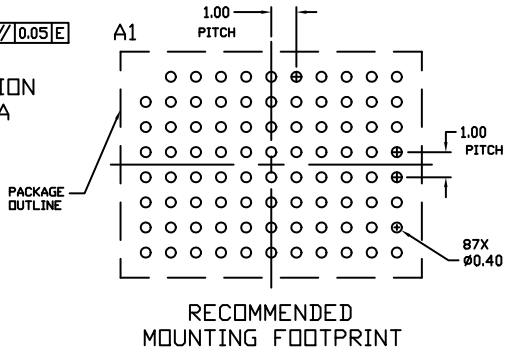
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. MAXIMUM ROTATION OF THE OPTICAL AREA RELATIVE TO D AND E WILL BE 0.5°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATASHEET FOR TOTAL ARRAY AND FIRST PIXEL DEFINITIONS.
7. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
8. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X=−220.41 MICRONS, Y=−147.01 MICRONS ±75 MICRONS.





DIM	MILLIMETERS	
	MIN.	MAX.
A	---	1.65
A1	0.35	0.45
A3	0.425	0.525
A4	0.575	0.675
b	0.45	0.55
D	12.00 BSC	
D2	10.20	10.40
E	9.00 BSC	
E2	6.80	7.00
e	1.00 BSC	





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