SONY

Diagonal 13.4 mm (Type 1/1.2) CMOS solid-state Image Sensor with Square Pixel for B/W Cameras

Preliminary

IMX174LLJ-C

Description

The IMX174LLJ-C is a diagonal 13.4 mm (Type 1/1.2) CMOS active pixel type solid-state image sensor with a square pixel array and 2.35 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: FA cameras, ITS cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Global shutter function
- ◆ Input frequency
  37.125 MHz / 74.25 MHz
- ◆ Number of recommended recording pixels: 1920 (H) × 1200 (V) approx. 2.30 M pixels

  Readout mode
  WUXGA All-pixel scan mode
  UXGA readout mode
  1080p-Full HD readout mode
  ROI mode
  Vertical / Horizontal ‐ Normal / Inverted readout mode
- ◆ Readout rate
  Maximum frame rate in WUXGA All-pixel scan mode: 10 bit 164.5 frame/s, 12 bit 128.2 frame/s
- ◆ Variable-speed shutter function (resolution 1 H units)
- ◆ 10-bit / 12-bit A/D converter
- ◆ CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆ I/O interface
  Low voltage LVDS (150 mVp-p) serial (2 ch / 4 ch / 8 ch switching) DDR output
- ◆ Recommended lens F number: 2.8 or more (Close side)
- ◆ Recommended exit pupil distance: –100 mm to –∞

Exmor™

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Rev 0.2

Device Structure

- ◆ CMOS image sensor
- ◆ Image size

Diagonal 13.4 mm (Type 1/1.2)	Approx. 2.35 M pixels	WUXGA
Diagonal 11.9 mm (Type 1/1.35)	Approx. 1.97 M pixels	UXGA
Diagonal 13.0 mm (Type 1/1.23)	Approx. 2.12 M pixels	1080p-Full HD

- ◆ Total number of pixels

1936 (H) × 1226 (V)	Approx. 2.37 M pixels

- ◆ Number of effective pixels

1936 (H) × 1216 (V)	Approx. 2.35 M pixels

- ◆ Number of active pixels

1936 (H) × 1216 (V)	Approx. 2.35 M pixels

- ◆ Number of recommended recording pixels

1920 (H) × 1200 (V)	Approx. 2.30 M pixels	WUXGA
1600 (H) × 1200 (V)	Approx. 1.92 M pixels	UXGA
1920 (H) × 1080 (V)	Approx. 2.07 M pixels	1080p-Full HD

- ◆ Unit cell size
  5.86 μm (H) × 5.86 μm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 10 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	AV_{DD}	–0.3	to	+4.0	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	–0.3	to	+3.3	V	
Supply voltage (Digital 1.2 V)	DV_{DD}	–0.3	to	+2.0	V	
Input voltage	VI	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Output voltage	VO	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Operating temperature	Topr	TBD	to	TBD	˚C	
Storage temperature	Tstg	-40	to	+85	˚C	
Performance guarantee temperature	Tspec	–10	to	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	AV_{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (Digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

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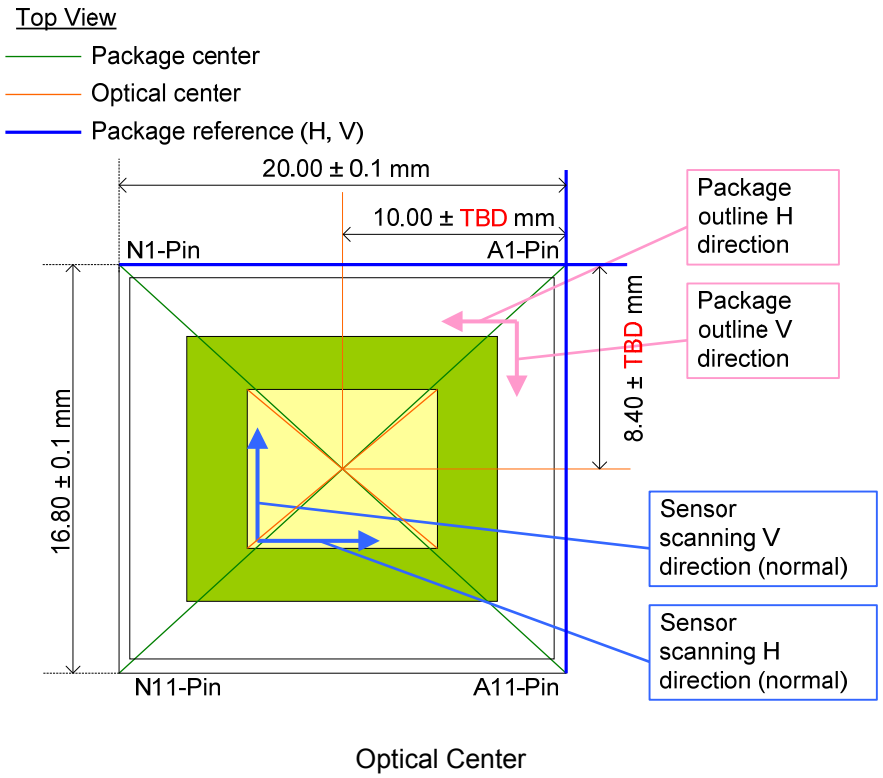
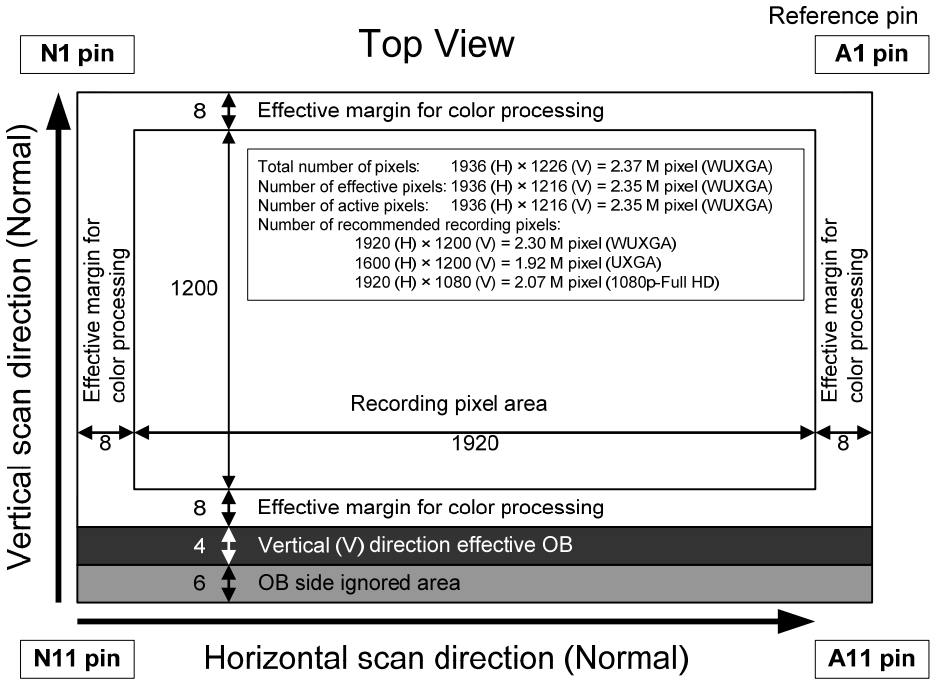
Chip Center and Optical Center



Optical Center

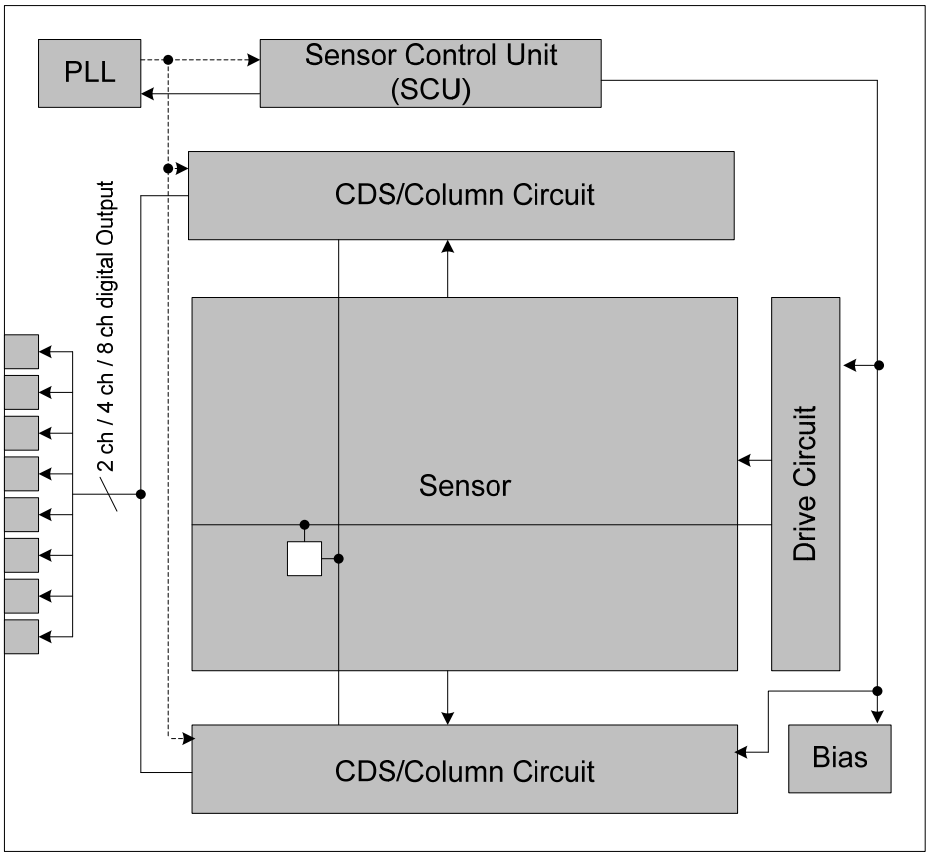
Pixel Arrangement



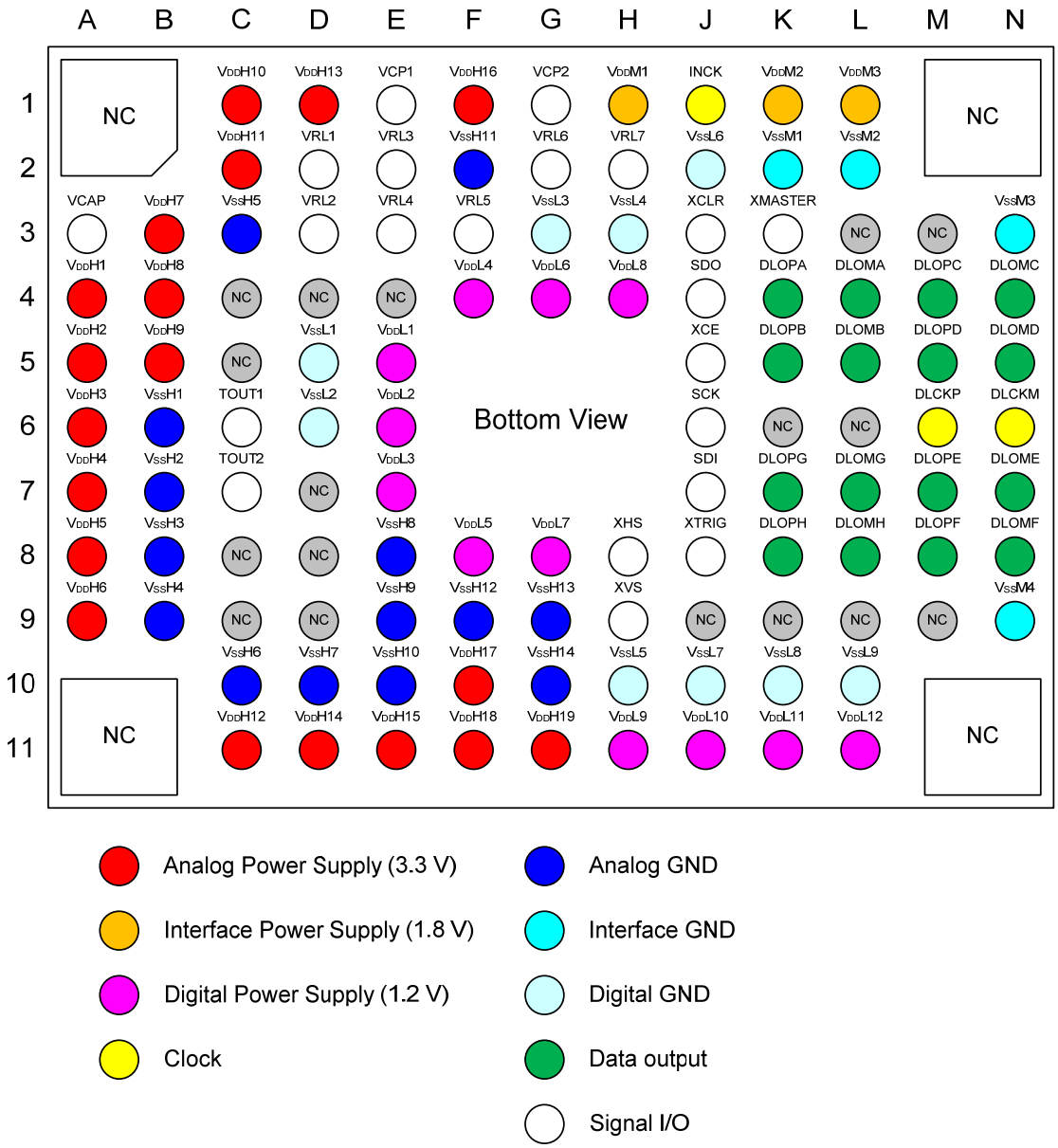
Pixel Arrangement

Block Diagram and Pin Configuration

(Top View)



Block Diagram



Pin Configuration

Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C	—
2	A3	O	A	VCAP	Reference pin (Connect to a 0.22 µF to GND)
3	A4	Power	A	V_{DD}H1	3.3 V power supply
4	A5	Power	A	V_{DD}H2	3.3 V power supply
5	A6	Power	A	V_{DD}H3	3.3 V power supply
6	A7	Power	A	V_{DD}H4	3.3 V power supply
7	A8	Power	A	V_{DD}H5	3.3 V power supply
8	A9	Power	A	V_{DD}H6	3.3 V power supply
9	A11	—	—	N.C.	—
10	B3	Power	A	V_{DD}H7	3.3 V power supply
11	B4	Power	A	V_{DD}H8	3.3 V power supply
12	B5	Power	A	V_{DD}H9	3.3 V power supply
13	B6	GND	A	V_{SS}H1	3.3 V GND
14	B7	GND	A	V_{SS}H2	3.3 V GND
15	B8	GND	A	V_{SS}H3	3.3 V GND
16	B9	GND	A	V_{SS}H4	3.3 V GND
17	C1	Power	A	V_{DD}H10	3.3 V power supply
18	C2	Power	A	V_{DD}H11	3.3 V power supply
19	C3	GND	A	V_{SS}H5	3.3 V GND
20	C4	—	—	N.C	—
21	C5	—	—	N.C	—
22	C6	O	D	TOUT1	Pulse1 output pin
23	C7	O	D	TOUT2	Pulse2 output pin
24	C8	—	—	N.C	—
25	C9	—	—	N.C	—
26	C10	GND	A	V_{SS}H6	3.3 V GND
27	C11	Power	A	V_{DD}H12	3.3 V power supply
28	D1	Power	A	V_{DD}H13	3.3 V power supply
29	D2	I	A	VRL1	Connect to VCP1
30	D3	I	A	VRL2	Connect to VCP1
31	D4	—	—	N.C	—
32	D5	GND	D	V_{SS}L1	1.2 V GND
33	D6	GND	D	V_{SS}L2	1.2 V GND
34	D7	—	—	N.C	—
35	D8	—	—	N.C	—
36	D9	—	—	N.C	—
37	D10	GND	A	V_{SS}H7	3.3 V GND
38	D11	Power	A	V_{DD}H14	3.3 V power supply
39	E1	O	A	VCP1	Connect to VRL1, 2, 3, 4, 5 (Connect to 4.7 µF × 2 to GND)
40	E2	I	A	VRL3	Connect to VCP1
41	E3	I	A	VRL4	Connect to VCP1
42	E4	—	—	N.C	—
43	E5	Power	D	V_{DD}L1	1.2 V power supply
44	E6	Power	D	V_{DD}L2	1.2 V power supply
45	E7	Power	D	V_{DD}L3	1.2 V power supply
46	E8	GND	A	V_{SS}H8	3.3 V GND
47	E9	GND	A	V_{SS}H9	3.3 V GND
48	E10	GND	A	V_{SS}H10	3.3 V GND
49	E11	Power	A	V_{DD}H15	3.3 V power supply
50	F1	Power	A	V_{DD}H16	3.3 V power supply
51	F2	GND	A	V_{SS}H11	3.3 V GND
52	F3	I	A	VRL5	Connect to VCP1
53	F4	Power	D	V_{DD}L4	1.2 V power supply
54	F8	Power	D	V_{DD}L5	1.2 V power supply
55	F9	GND	A	V_{SS}H12	3.3 V GND
56	F10	Power	A	V_{DD}H17	3.3 V power supply
57	F11	Power	A	V_{DD}H18	3.3 V power supply
58	G1	O	A	VCP2	Connect to VRL6, 7 (Connect to 4.7 µF × 2 to GND)
59	G2	I	A	VRL6	Connect to VCP2
60	G3	GND	D	V_{SS}L3	1.2 V GND
61	G4	Power	D	V_{DD}L6	1.2 V power supply
62	G8	Power	D	V_{DD}L7	1.2 V power supply

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
63	G9	GND	A	V_{SS}H13	3.3 V GND
64	G10	GND	A	V_{SS}H14	3.3 V GND
65	G11	Power	A	V_{DD}H19	3.3 V power supply
66	H1	Power	D	V_{DD}M1	1.8 V power supply
67	H2	I	A	VRL7	Connect to VCP2
68	H3	GND	D	V_{SS}L4	1.2 V GND
69	H4	Power	D	V_{DD}L8	1.2 V power supply
70	H8	I/O	D	XHS	horizotal sync signal
71	H9	I/O	D	XVS	Vertical sync signal
72	H10	GND	D	V_{SS}L5	1.2 V GND
73	H11	Power	D	V_{DD}L9	1.2 V power supply
74	J1	I	D	INCK	Master clock input
75	J2	GND	D	V_{SS}L6	1.2 V GND
76	J3	I	D	XCLR	Sytem clear (Normal: High = OV_{DD}, Clear: Low = GND)
77	J4	O	D	SDO	4-wire serial communication I/F SDO pin
78	J5	I	D	XCE	4-wire serial communication I/F XCE pin
79	J6	I	D	SCK	4-wire serial communication I/F SCK pin
80	J7	I	D	SDI	4-wire serial communication I/F SDI pin
81	J8	I	D	XTRIG	Trigger input
82	J9	—	—	N.C	—
83	J10	GND	D	V_{SS}L7	1.2 V GND
84	J11	Power	D	V_{DD}L10	1.2 V power supply
85	K1	Power	D	V_{DD}M2	1.8 V power supply
86	K2	GND	D	V_{SS}M1	1.8 V GND
87	K3	I	D	XMASTER	Master / Slave select (In Slave mode: High = OV_{DD}, In Master mode: Low = GND)
88	K4	O	D	DLOPA	Low voltage LVDS serial output (Data)
89	K5	O	D	DLOPB	Low voltage LVDS serial output (Data)
90	K6	—	—	N.C	—
91	K7	O	D	DLOPG	Low voltage LVDS serial output (Data)
92	K8	O	D	DLOPH	Low voltage LVDS serial output (Data)
93	K9	—	—	N.C	—
94	K10	GND	D	V_{SS}L8	1.2 V GND
95	K11	Power	D	V_{DD}L11	1.2 V power supply
96	L1	Power	D	V_{DD}M3	1.8 V power supply
97	L2	GND	D	V_{SS}M2	1.8 V GND
98	L3	—	—	N.C	—
99	L4	O	D	DLOMA	Low voltage LVDS serial output (Data)
100	L5	O	D	DLOMB	Low voltage LVDS serial output (Data)
101	L6	—	—	N.C	—
102	L7	O	D	DLOMG	Low voltage LVDS serial output (Data)
103	L8	O	D	DLOMH	Low voltage LVDS serial output (Data)
104	L9	—	—	N.C	—
105	L10	GND	D	V_{SS}L9	1.2 V GND
106	L11	Power	D	V_{DD}L12	1.2 V power supply
107	M3	—	—	N.C	—
108	M4	O	D	DLOPC	Low voltage LVDS serial output (Data)
109	M5	O	D	DLOPD	Low voltage LVDS serial output (Data)
110	M6	O	D	DLCKP	Low voltage LVDS serial output (Clock)
111	M7	O	D	DLOPE	Low voltage LVDS serial output (Data)
112	M8	O	D	DLOPF	Low voltage LVDS serial output (Data)
113	M9	—	—	N.C	—
114	N1	—	—	N.C	—
115	N3	GND	D	V_{SS}M3	1.8 V GND
116	N4	O	D	DLOMC	Low voltage LVDS serial output (Data)
117	N5	O	D	DLOMD	Low voltage LVDS serial output (Data)
118	N6	O	D	DLCKM	Low voltage LVDS serial output (Clock)
119	N7	O	D	DLOME	Low voltage LVDS serial output (Data)
120	N8	O	D	DLOMF	Low voltage LVDS serial output (Data)
121	N9	GND	D	V_{SS}M4	1.8 V GND
122	N11	—	—	N.C	—

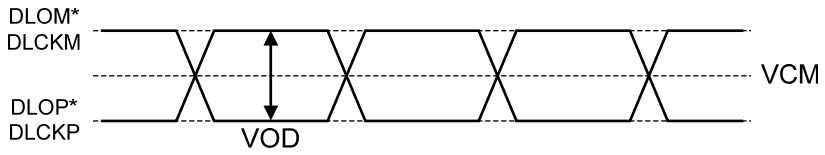
* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}Hx	AV_{DD}	—	3.15	3.30	3.45	V
	Interface	V_{DD}Mx	OV_{DD}	—	1.70	1.80	1.90	V
	Digital	V_{DD}Lx	DV_{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SCK SDI XCE XTRIG	VIH	XVS / XHS in Slave mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		DLOPx DLOMx DCKPx DCKMx	VCM	Low voltage LVDS (termination resistance: 100 Ω)	—	OV_{DD}/2	—	V
			VOD		100	150	210	mV
		XHS XVS SDO TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} -0.4	—	—	V
			VOL		—	—	0.4	V

LVDS output



Power Consumption

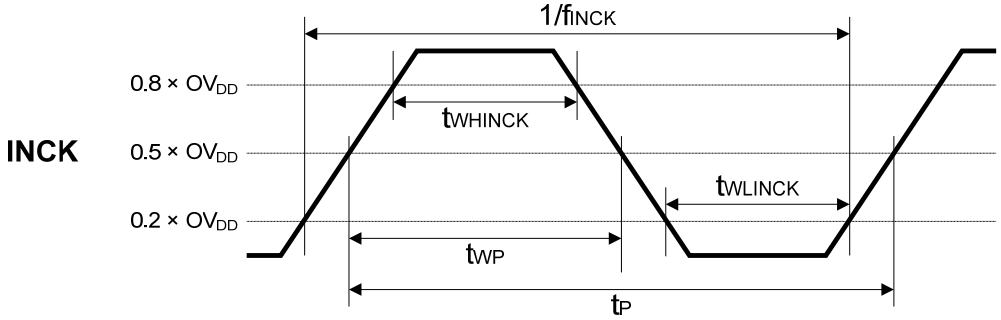
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current (TBD)	V_{DD}H	IAV_{DD}	TBD	TBD	mA
	V_{DD}M	IOV_{DD}	TBD	TBD	mA
	V_{DD}L	IDV_{DD}	TBD	TBD	mA
Standby current	V_{DD}H	IAV_{DD}_STB	—	TBD	mA
	V_{DD}M	IOV_{DD}_STB	—	TBD	mA
	V_{DD}L	IDV_{DD}_STB	—	TBD	mA

Operating current:
(Typical value condition) : Supply voltage: 3.30 V / 1.80 V / 1.20 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

AC Characteristics

Master Clock (INCK) Waveform Diagram

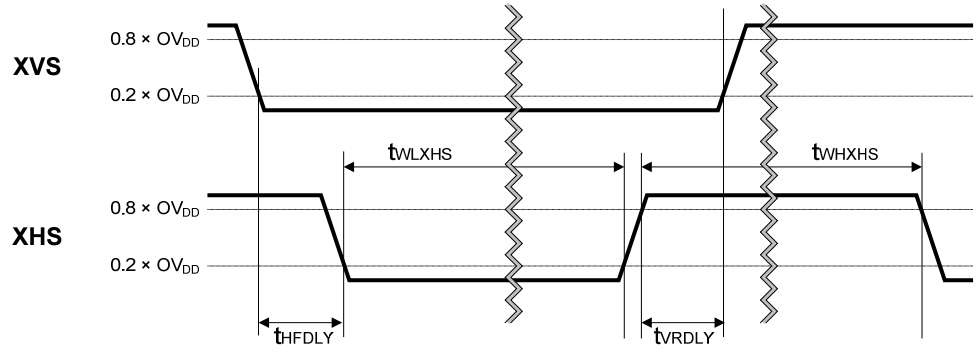


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

* The INCK fluctuation affects the frame rate.

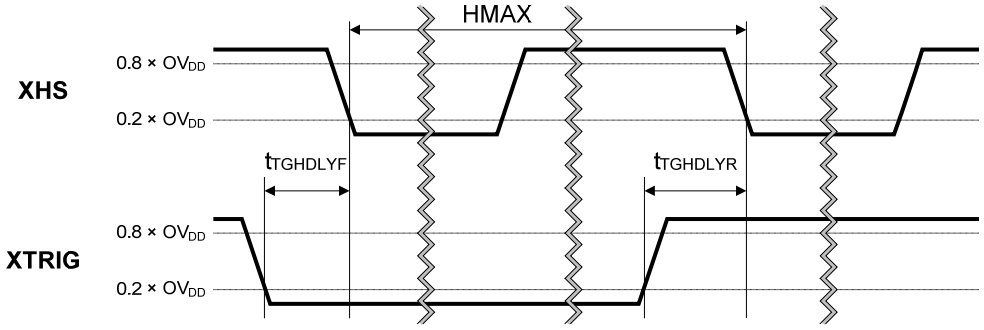
XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

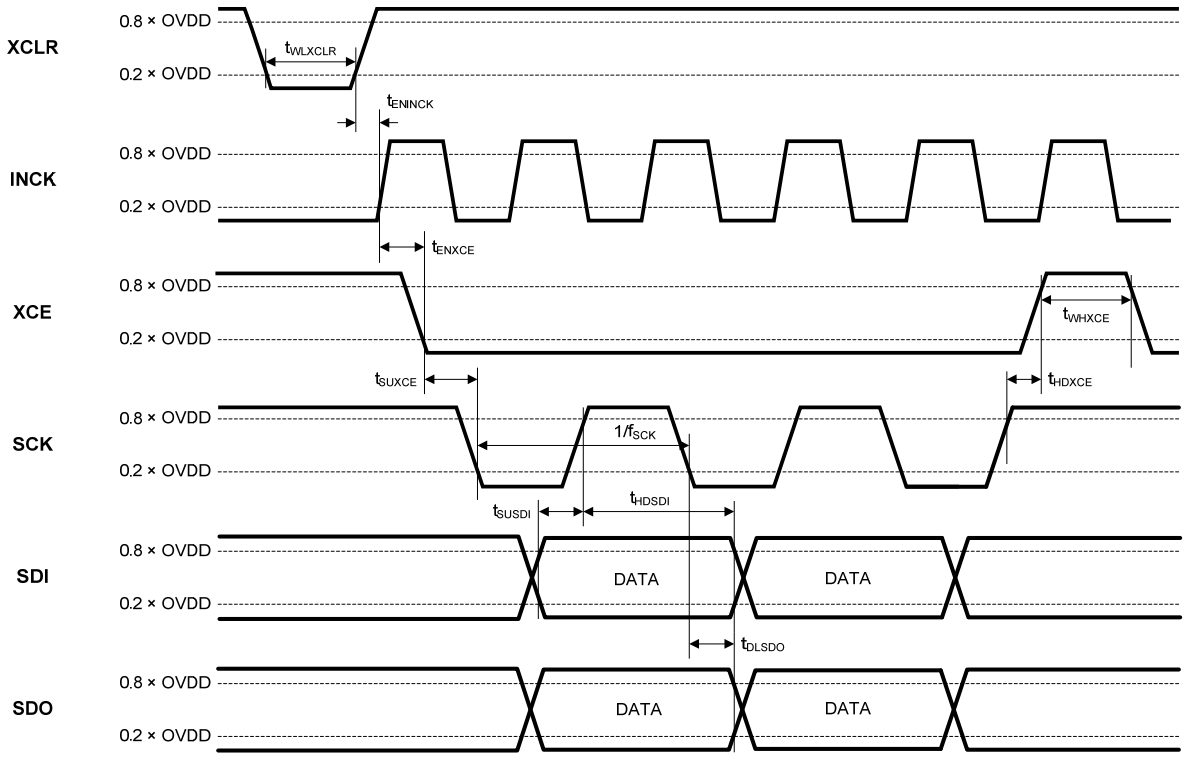
XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK
XTRIG fall - XHS rise width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK

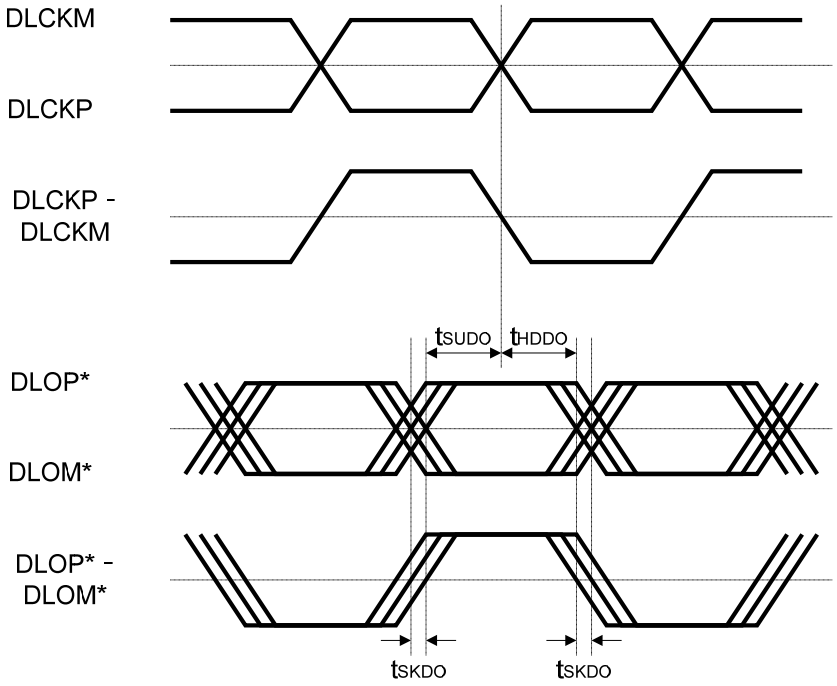
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
INCK effective margin	t_{ENINCK}	1	—	—	µs	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

DLCKP / DLCKM, DLOPx / DLOMx



(Output load capacitance: 8 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DLCK clock duty	—	40	50	60	%	DCK freq = 297 MHz (Max.)
DLO skew time	t_{SKDO}	—	—	400	ps	Data Rate 297 MHz DDR
DLO setup time	t_{SUDO}	400	—	—	ps	Data Rate 297 MHz DDR
DLO hold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

TBD

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

TBD

Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, All-pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	TBD (TBD)	TBD (TBD)	—	Digit (mV)	1	1/30 s storage
Saturation signal	Vsat2D	TBD (TBD)	—	—	Digit (mV)	2	Zone0 to II'
Video signal shading	SH01	—	—	TBD	%	3	Zone0, I
	SH2D	—	—	TBD	%		Zone0 to II'
Dark signal	Vdt	—	—	TBD (TBD)	Digit (mV)	4	1/30 s storage
Dark signal shading	ΔVdt	—	—	TBD (TBD)	Digit (mV)	5	1/30 s storage

Note) 1. Converted value into mV using 1Digit = 0.2256 mV for 12-bit output and 1Digit = 0.9023 mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

Zone Definition of Video Signal Shading

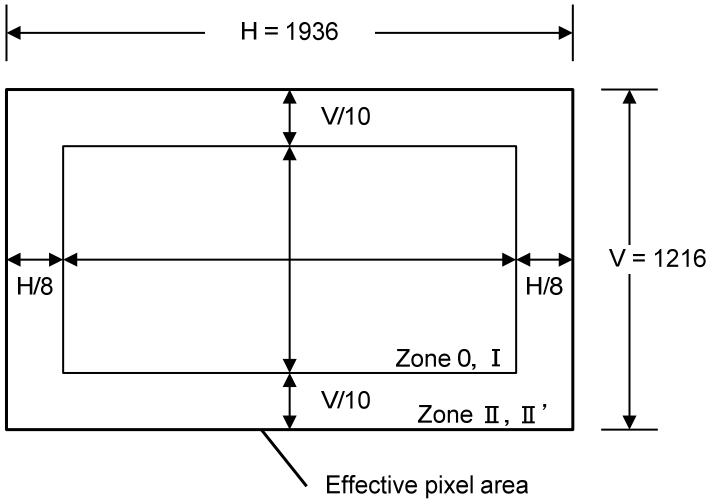


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

Definition of srandard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the signal outputs (V) at the center of the screen, and substitute the values into the following formula.

   $$S = (V) \times 100/30 \text{ [mV]}$$

2. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal outputs, TBD mV, measure the average values of the signal outputs.

3. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the signal outputs is TBD mV. Then measure the maximum value (Vmax [mV]) and the minimum value (Vmin [mV]) of the signal outputs, and substitute the values into the following formula.

   $$SH = (Vmax - Vmin) / TBD \times 100 \text{ [\%]}$$

4. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

5. Dark signal shading
   After the measurement item 4, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

Setting Registers Using Serial Communication

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

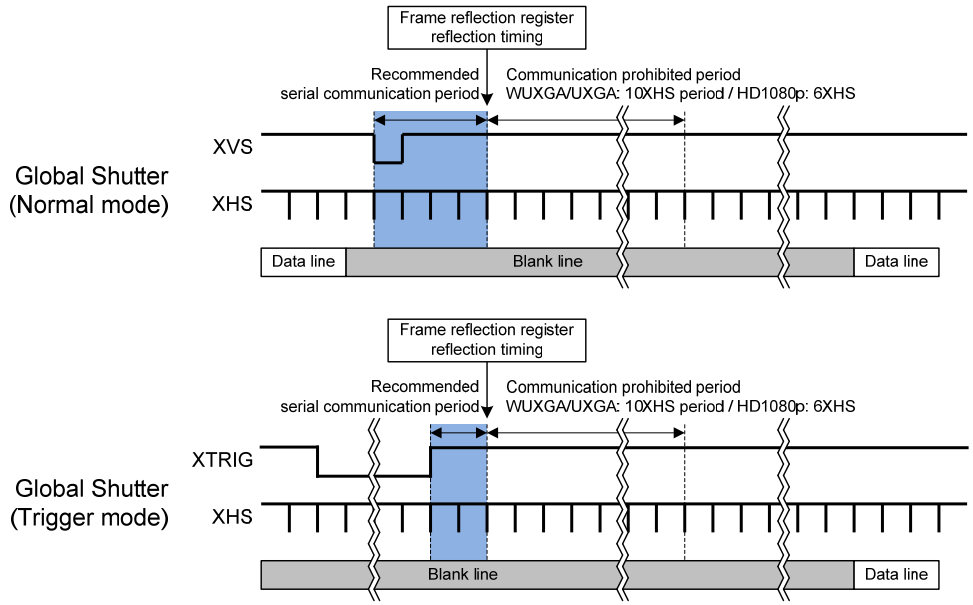
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers, set them in sensor standby state.)



Register Write and Read

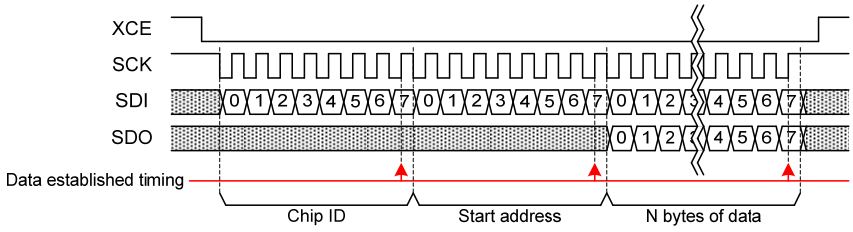
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 09h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

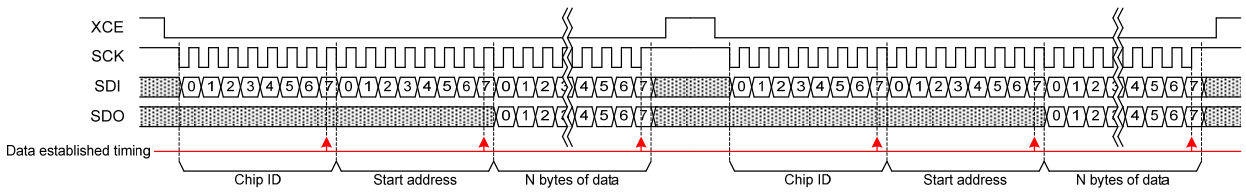
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 89h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Register Map

This sensor has a total of 2048 bytes of registers, composed of registers with address 00h to FEh that correspond to Chip ID = 02h to 09h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 2048 bytes.

There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers below, set them in sensor standby state.

・STBLVDS
・ADBIT
・ODBIT
・OPORTSEL
・INCKSEL0
・INCKSEL1
・INCKSEL2

For the register that is writing "*" to the setting value in description, change the value from the default value after the reset.

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors.

Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
01h to 04h	[7:0] to [7:0]		Fixed to 00h	00h to 00h	00h to 00h	—
05h	0		Fixed to 0	0	00h	—
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4	STBLVDS [3:0]	LVDS channels that not using be standby 0h: 8 ch active 1h: 4 ch active 2h: 2 ch active Others: Setting prohibited	0h		Immediately
	5					
	6					
	7					
06h to 0Bh	[7:0] to [7:0]		Fixed to 00h	00h to 00h	00h to 00h	—
0Ch	0	REGHOLD [0]	Register hold (Function not to update V reflection regsiters) 0: Invalid 1: Valid	0	00h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
0Dh to 11h	[7:0] to [7:0]		Fixed to 00h	00h to 00h	00h to 00h	—
12h	0	XMSTA [0]	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
13h	0	TRIGEN [0]	Global shutter mode setting 0: Normal mode 1: Trigger mode	0	00h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
14h	0	ADBIT [0]	AD conversion bits setting 0: 10 bit 1: 12 bit	1	01h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
15h	0	MODE [3:0]	Drive mode setting 0h: WUXGA 2h: UXGA 4h: 1080p-Full HD Others: Setting prohibited	0h	00h	V
	1					
	2					
	3					
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
16h	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
	1	HREVERSE [0]	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
17h	0	VMAX [11:0]	LSB When sensor master mode vertical span setting. (Number of operation lines count from 1)	4E6h	E6h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
18h	0				04h	
	1					
	2					
	3		MSB			
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
19h	[7:0]		Fixed to 00h	00h	00h	—
1Ah	0	HMAX [15:0]	LSB	01CEh	CEh	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		When sensor master mode horizontal span setting. (Number of operation clocks count from 1)			
1Bh	0				01h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
1Ch	0	ODBIT [0]	Number of output bit setting 0: 10 bit 1: 12 bit	1	11h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4	OPORTSEL [2:0]	Output channel selection 1h: 8 ch 3h: 4 ch 4h: 2 ch Others: Setting prohibited	1h		Immediately
	5					
	6					
	7		Fixed to 0	0		—
1Dh	[7:0]		Fixed to 01h	01h	01h	—
1Eh	[7:0]		Fixed to 02h	02h	02h	—
1Fh	0	CKSEL [0]	The value is set according to drive mode. When WUXGA, UXGA, ROI: 0 When 1080p-Full HD: 1	0	00h	Immediately
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
20h	[7:0]		Fixed to 01h	01h	01h	—
21h	0	FREQ [1:0]	Set to datarate.	0h	00h	V
	1					
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
22h to 2Dh	[7:0] to [7:0]		Do not rewrite	—	—	—
2Eh	0	XVSOUTSEL[1:0]	XVS pin setting 0h: Slave mode 2h: Master mode	2h	0Ah	Immediately
	1					
	2	XHSOUTSEL[1:0]	XHS pin setting 0h: Slave mode 2h: Master mode	2h		Immediately
	3					
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
2Fh	0	TOUT1SEL[1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output	0h	00h	Immediately
	1					
	2	TOUT2SEL[1:0]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output	0h		Immediately
	3					
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
30h	0		Fixed to 00h	00h	00h	—
31h	0		Fixed to 00h	00h	00h	—
32h	0	TRIG_TOUT1_SEL[2:0]	TOUT1 pin setting 0h: Low fixed 1h: Pulse1 output	0h	00h	Immediately
	1					
	2					
	3		Fixed to 0	0		—
	4	TRIG_TOUT2_SEL[2:0]	TOUT2 pin setting 0h: Low fixed 2h: Pulse2 output	0h		Immediately
	5					
	6					
	7		Fixed to 0	0		—

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
33h to 75h	[7:0] to [7:0]		Do not rewrite	—	—	—
76h	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	Immediately
	1	PULSE1_EN_TRIG [0]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		Immediately
	2	PULSE1_POL [0]	Pulse1 polarity selection 0: High active 1: Low active	0		Immediately
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
77h	0	PULSE1_UP [15:0]	LSB	0000h	00h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
78h	0				00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
79h	[7:0]		Fixed to 00h	00h	00h	—
7Ah	0	PULSE1_DN [15:0]	LSB	0000h	00h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)			
7Bh	0				00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
7Ch	[7:0]		Fixed to 00h	00h	00h	—
7Dh	[7:0]		Fixed to 00h	00h	00h	—

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
7Eh	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	Immediately
	1	PULSE2_EN_TRIG [0]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		Immediately
	2	PULSE2_POL [0]	Pulse2 polarity selection 0: High active 1: Low active	0		Immediately
	3		Fixed to 1 *	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
7Fh	0	PULSE2_UP [15:0]	LSB	0000h	00h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7		Pulse2 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
80h	0				00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
81h	[7:0]		Fixed to 00h	00h	00h	—
82h	0	PULSE2_DN [15:0]	LSB	0000h	00h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
83h	0				00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
84h	[7:0]		Fixed to 00h	00h	00h	—

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
85h to 91h	[7:0] to [7:0]		Do not rewrite	—	—	—
92h	[7:0]	INCKSEL0 [7:0]	The value is set according to drive mode. When WUXGA, UXGA, ROI: 20h When 1080p-Full HD: 18h	20h	20h	Immediately
93h	[7:0]	INCKSEL1 [7:0]	The value is set according to INCK. 00h: INCK = 37.125 MHz 04h: INCK = 74.25 MHz	00h	00h	Immediately
94h	[7:0]		Fixed to 20h	20h	20h	—
95h	[7:0]	INCKSEL2 [7:0]	The value is set according to INCK. 00h: INCK = 37.125 MHz 04h: INCK = 74.25 MHz	00h	00h	Immediately
96h	[7:0]		Fixed to 00h	00h	00h	—
97h	[7:0]		Fixed to 00h	00h	00h	—
98h	[7:0]		Fixed to 00h	00h	00h	—
99h	[7:0]		Fixed to 00h	00h	00h	—
9Ah	0	SHS [11:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9Bh	0				00h	
	1					
	2					
	3		MSB			
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
9Ch	[7:0]		Fixed to 00h	00h	00h	—
9Dh	[7:0]		Fixed to 00h	00h	00h	—
9Eh	[7:0]		Fixed to 00h	00h	00h	—
9Fh	[7:0]		Fixed to 00h	00h	00h	—
A0h	[7:0]	GTWAIT [7:0]	The value is set according to drive mode. When WUXGA, UXGA, ROI: A4h When 1080p-Full HD: 64h	A4h	A4h	Immediately
A1h	[7:0]		Fixed to 02h	02h	02h	—
A2h	[7:0]		Fixed to 01h	01h	01h	—
A3h	[7:0]		Fixed to 00h	00h	00h	—
A4h	[7:0]		Fixed to 00h	00h	00h	—
A5h	[7:0]	GSDLY [7:0]	The value is set according to drive mode. When WUXGA, UXGA, ROI: 08h When 1080p-Full HD: 04h	08h	08h	Immediately
A6h to FFh	[7:0] to [7:0]		Do not rewrite	—	—	—

Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h	0	ROIH1ON [0]	The horizontal setting of ROI area (1, y) (y = 1 to 4) 0: Disable 1: Enable	0	00h	V
	1	ROIV1ON [0]	The vertical setting of ROI area (x, 1) (x = 1 to 4) 0: Disable 1: Enable	0		Immediately
	[7:2]		Fixed to 00h	00h		—
01h	[7:0]	ROIPH1 [10:0]	Designation of horizontal cropping position on area (1, y) (y = 1 to 4)	000h	00h	V
02h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
03h	[7:0]	ROIPV1 [10:0]	Designation of vertical cropping position on area (x, 1) (x = 1 to 4)	000h	00h	Immediately
04h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
05h	[7:0]	ROIWH1 [10:0]	Designation of horizontal cropping size on area (1, y) (y = 1 to 4)	000h	00h	V
06h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
07h	[7:0]	ROIWV1 [10:0]	Designation of vertical cropping size on area (x, 1) (x = 1 to 4)	000h	00h	Immediately
08h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
09h	0	ROIH2ON [0]	The horizontal setting of ROI area (2, y) (y = 1 to 4) 0: Disable 1: Enable	0	00h	V
	1	ROIV2ON [0]	The vertical setting of ROI area (x, 2) (x = 1 to 4) 0: Disable 1: Enable	0		Immediately
	[7:2]		Fixed to 00h	00h		—
0Ah	[7:0]	ROIPH2 [10:0]	Designation of horizontal cropping position on area (2, y) (y = 1 to 4)	000h	00h	V
0Bh	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
0Ch	[7:0]	ROIPV2 [10:0]	Designation of vertical cropping position on area (x, 2) (x = 1 to 4)	000h	00h	Immediately
0Dh	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
0Eh	[7:0]	ROIWH2 [10:0]	Designation of horizontal cropping size on area (2, y) (y = 1 to 4)	000h	00h	V
0Fh	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
10h	[7:0]	ROIWV2 [10:0]	Designation of vertical cropping size on area (x, 2) (x = 1 to 4)	000h	00h	Immediately
11h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
12h	0	ROIH3ON [0]	The horizontal setting of ROI area (3, y) (y = 1 to 4) 0: Disable 1: Enable	0	00h	V
	1	ROIV3ON [0]	The vertical setting of ROI area (x, 3) (x = 1 to 4) 0: Disable 1: Enable	0		Immediately
	[7:2]		Fixed to 00h	00h		—
13h	[7:0]	ROIPH3 [10:0]	Designation of horizontal cropping position on area (3, y) (y = 1 to 4)	000h	00h	V
14h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
15h	[7:0]	ROIPV3 [10:0]	Designation of vertical cropping position on area (x, 3) (x = 1 to 4)	000h	00h	Immediately
16h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
17h	[7:0]	ROIWH3 [10:0]	Designation of horizontal cropping size on area (3, y) (y = 1 to 4)	000h	00h	V
18h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
19h	[7:0]	ROIWV3 [10:0]	Designation of vertical cropping size on area (x, 3) (x = 1 to 4)	000h	00h	Immediately
1Ah	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
1Bh	0	ROIH4ON [0]	The horizontal setting of ROI area (4, y) (y = 1 to 4) 0: Disable 1: Enable	0	00h	V
	1	ROIV4ON [0]	The vertical setting of ROI area (x, 4) (x = 1 to 4) 0: Disable 1: Enable	0		Immediately
	[7:2]		Fixed to 00h	00h		—
1Ch	[7:0]	ROIPH4 [10:0]	Designation of horizontal cropping position on area (4, y) (y = 1 to 4)	000h	00h	V
1Dh	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
1Eh	[7:0]	ROIPV4 [10:0]	Designation of vertical cropping position on area (x, 4) (x = 1 to 4)	000h	00h	Immediately
1Fh	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
20h	[7:0]	ROIWH4 [10:0]	Designation of horizontal cropping size on area (4, y) (y = 1 to 4)	000h	00h	V
21h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
22h	[7:0]	ROIWV4 [10:0]	Designation of vertical cropping size on area (x, 4) (x = 1 to 4)	000h	00h	Immediately
23h	[2:0]				00h	
	[7:3]		Fixed to 00h	00h		—
24h to FFh	[7:0] to [7:0]		Do not rewrite	—	—	—

Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h	[7:0]		Fixed to 01h	01h	01h	—
01h	[7:0]		Fixed to 00h	00h	00h	—
02h	[7:0]		Fixed to F0h	F0h	F0h	—
03h	[7:0]		Fixed to 00h	00h	00h	—
04h	0	GAIN [8:0]	LSB Gain setting 0 dB (000d) to 48 dB (480d) 0.1 dB Step	000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
05h	0		MSB		00h	
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
06h to 57h	[7:0] to [7:0]		Do not rewrite	—	—	—
58h	0	BLKLEVEL [8:0]	LSB Black level offset value setting Recommended value: 60d (10 bit), 240d (12 bit)	0F0h	F0h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
59h	0		MSB		00h	
	1		Fixed to 0	0		—
	2		Fixed to 0	0		—
	3		Fixed to 0	0		—
	4		Fixed to 0	0		—
	5		Fixed to 0	0		—
	6		Fixed to 0	0		—
	7		Fixed to 0	0		—
5Ah to FFh	[7:0] to [7:0]		Do not rewrite	—	—	—

Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h to FFh	[7:0] to [7:0]	Reserved	*These registers may change by update.			

Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h to FFh	[7:0] to [7:0]	Reserved	*These registers may change by update.			

Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h)

Address	Bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h to FFh	[7:0] to [7:0]	Reserved	*These registers may change by update.			

Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h to FFh	[7:0] to [7:0]	Reserved	*These registers may change by update.			

Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h)

Address	bit	Register Name	Description	Default value after reset		Reflection timing
				By register	By address	
00h to FFh	[7:0] to [7:0]	Reserved	*These registers may change by update.			

Readout Drive Modes

The table below lists the operating modes available with this sensor.

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	Serial LVDS ch[*1]			A/D conversion	Number of recording pixels		Total number of pixels[*2]		Number of INCK in 1H	
			2 ch	4 ch	8 ch		H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz
WUXGA	164.5	4.752	N/A	N/A	○	10	1920	1200	2304	1254	180	360
	82.3	2.376	N/A	○	○						360	720
	41.2	1.188	○	○	○						720	1440
	128.2	4.752	N/A	N/A	○	12			2464		231	462
	64.1	2.376	N/A	○	○						462	924
	32.1	1.188	○	○	○						924	1848
UXGA	164.5	4.752	N/A	N/A	○	10	1600	1200	2304	1254	180	360
	82.3	2.376	N/A	○	○						360	720
	41.2	1.188	○	○	○						720	1440
	128.2	4.752	N/A	N/A	○	12			2464		231	462
	64.1	2.376	N/A	○	○						462	924
	32.1	1.188	○	○	○						924	1848
HD1080p	120	3.564	N/A	N/A	○	10	1920	1080	2640	1125	275	550
	60	1.782	N/A	○	○						550	1100
	30	0.891	○	○	○						1100	2200
	120	3.564	N/A	N/A	○	12			2200		275	550
	60	1.782	N/A	○	○						550	1100
	30	0.891	○	○	○						1100	2200
ROI	*4	4.752	N/A	N/A	○	10	*3	*3	2304	*4	180	360
	*4	2.376	N/A	○	○						360	720
	*4	1.188	○	○	○						720	1440
	*4	4.752	N/A	N/A	○	12			2464		231	462
	*4	2.376	N/A	○	○						462	924
	*4	1.188	○	○	○						924	1848

*1 The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.
Example) In WUXGA 164.5 [frame/s] mode: 4.752 [Gbps] / 8 = 594 [Mbps]

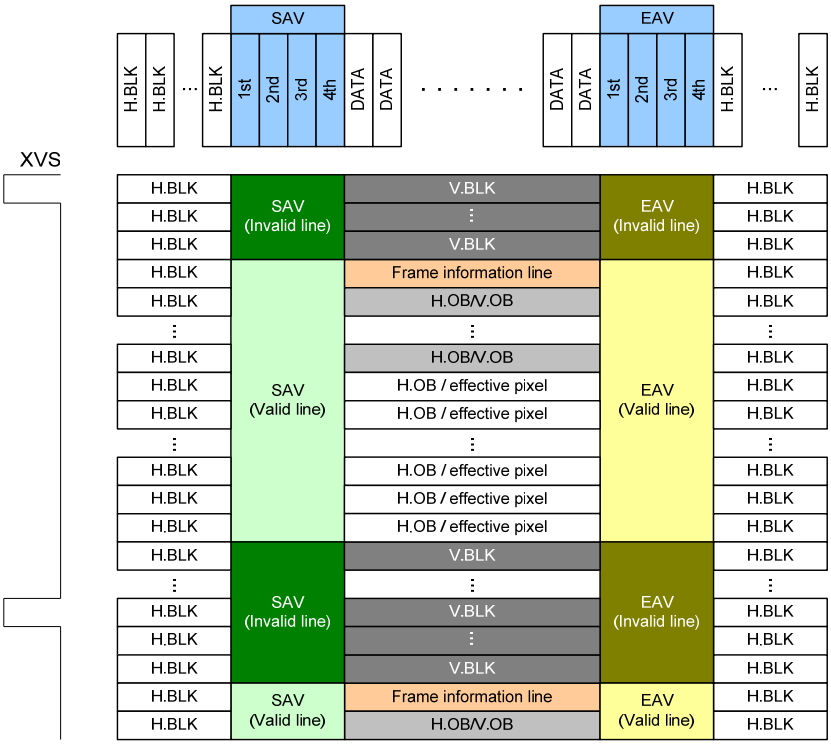
*2 For the setting value to register HMAX / VMAX, see the section of each drive mode settings

*3 Designated cropping area (ROI)

*4 See the section of “ROI mode”

Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



Sync Code Output Timing

List of Sync Code

Sync code	1st code		2nd code		3rd code		4th code	
	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit
SAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

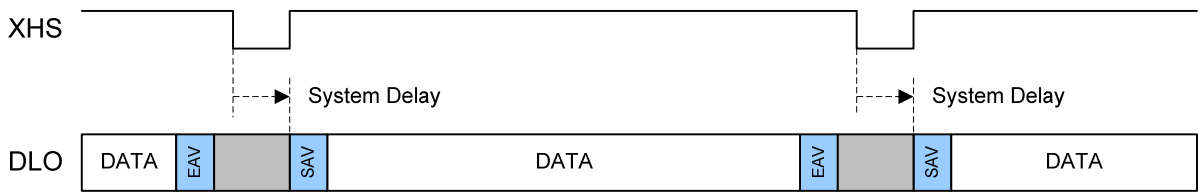
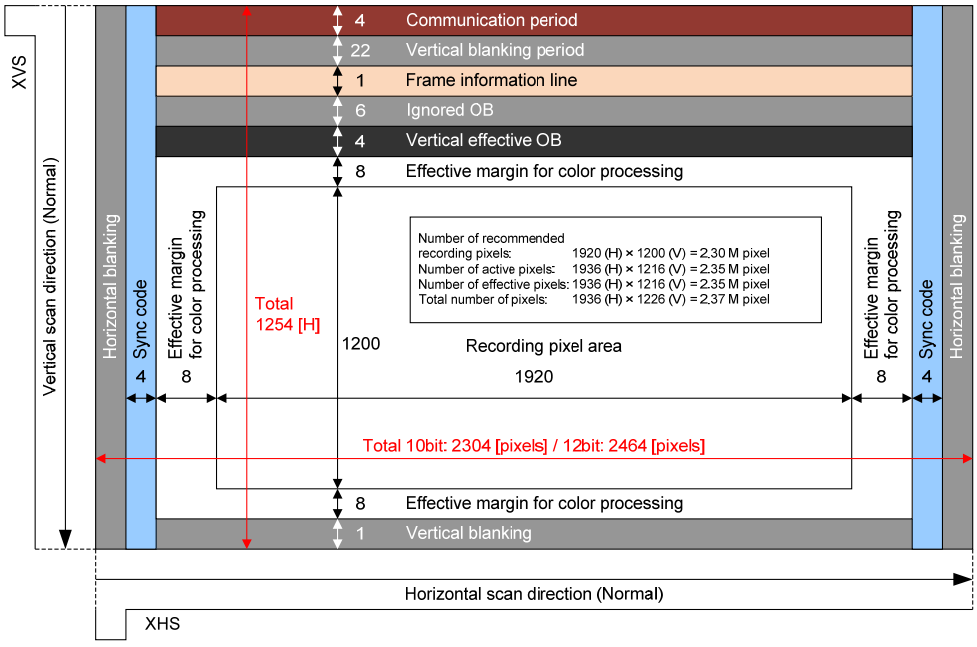


Image Data Output Format

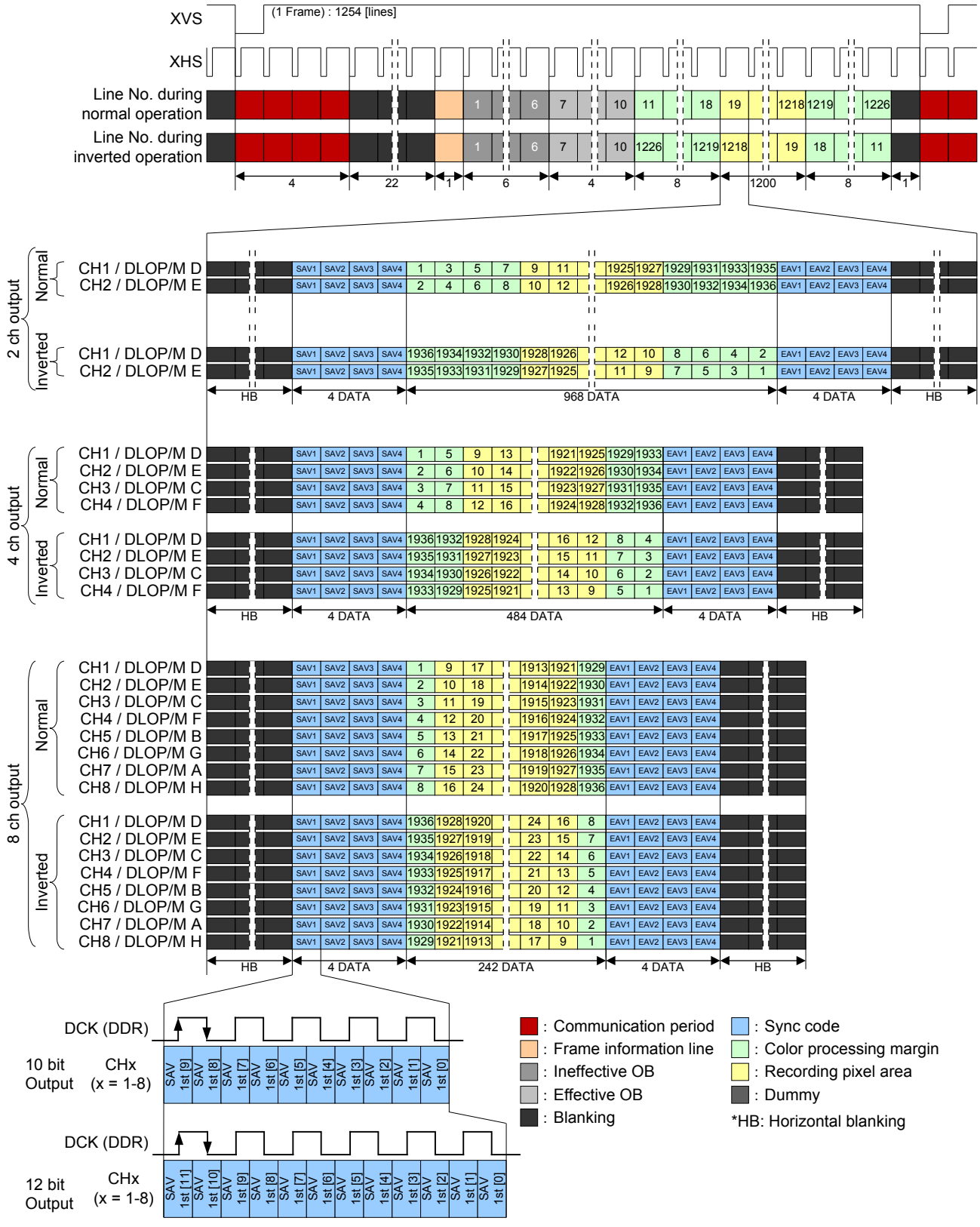
WUXGA mode (All-pixel scan)

Register List of WUXGA mode

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 10 bit			AD = 12 bit			
				164.5 [frame/s]	82.3 [frame/s]	41.2 [frame/s]	128.2 [frame/s]	64.1 [frame/s]	32.1 [frame/s]	
Chip ID = 02h										
05h	[7:4]	STBLVDS	0h	0h						8 ch LVDS
				N/A	1h		N/A	1h		4 ch LVDS
				N/A	N/A	2h	N/A	N/A	2h	2 ch LVDS
14h	[0]	ADBIT	1	0			1			0: 10 bit 1: 12 bit
15h	[3:0]	MODE	0h	0h						WUXGA mode
17h	[7:0]	VMAX	4E6h	4E6h						1254 line
18h	[3:0]									
1Ah	[7:0]	HMAX	1CEh	168h	2D0h	5A0h	1CEh	39Ch	738h	
1Bh	[7:0]									
1Ch	[0]	ODBIT	1	0			1			0: 10 bit 1: 12 bit
	[6:4]	OPORTSEL	1h	1h						8 ch LVDS
				N/A	3h		N/A	3h		4 ch LVDS
				N/A	N/A	4h	N/A	N/A	4h	2 ch LVDS
1Fh	[7:0]	CKSEL	00h	00h						
21h	[1:0]	FREQ	0h	0h	1h	2h	0h	1h	2h	8 ch LVDS
				N/A	0h	1h	N/A	0h	1h	4 ch LVDS
				N/A	N/A	0h	N/A	N/A	0h	2 ch LVDS
92h	[7:0]	INCKSEL0	20h	20h						
93h	[7:0]	INCKSEL1	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
95h	[7:0]	INCKSEL2	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
A0h	[7:0]	GTWAIT	A4h	A4h						
A5h	[7:0]	GSDLY	08h	08h						



Pixel Array Image Drawing in WUXGA Mode

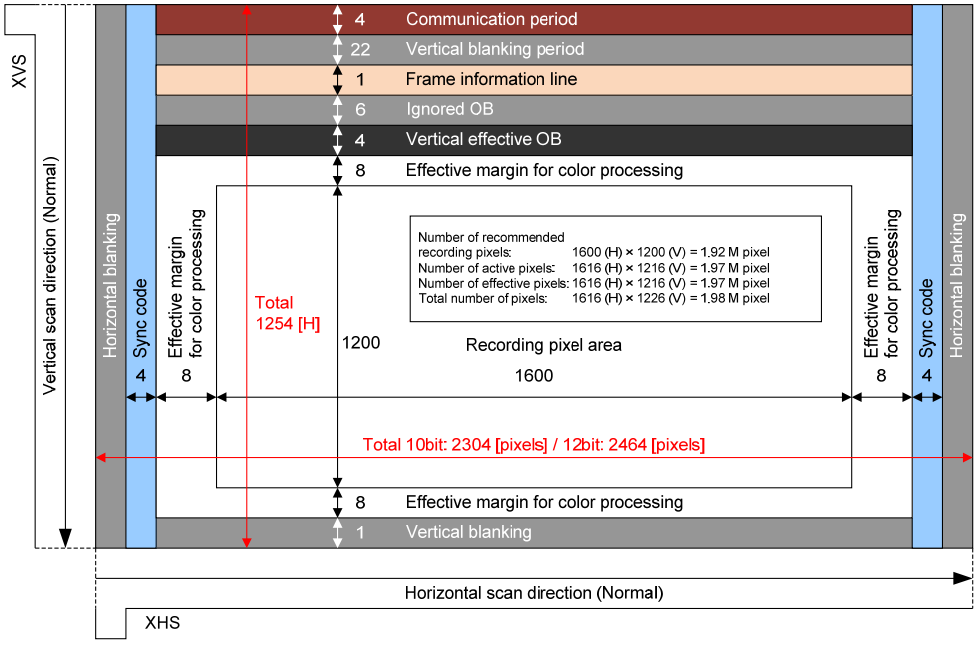


Drive Timing Chart for Serial Output in WUXGA Mode

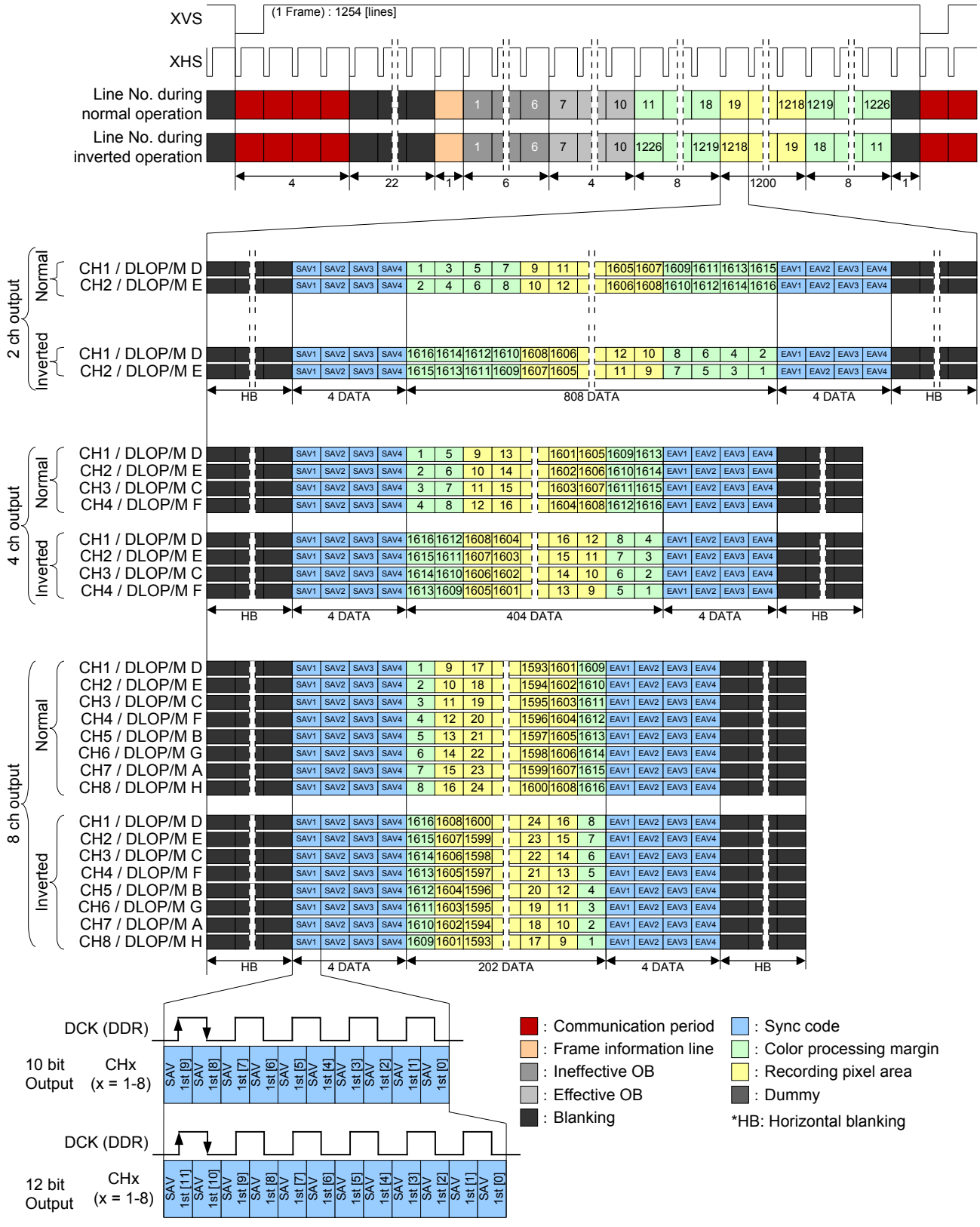
UXGA mode

Register List of UXGA mode

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 10 bit			AD = 12 bit			
				164.5 [frame/s]	82.3 [frame/s]	41.2 [frame/s]	128.2 [frame/s]	64.1 [frame/s]	32.1 [frame/s]	
Chip ID = 02h										
05h	[7:4]	STBLVDS	0h	0h						8 ch LVDS
				N/A	1h		N/A	1h		4 ch LVDS
				N/A	N/A	2h	N/A	N/A	2h	2 ch LVDS
14h	[0]	ADBIT	1	0			1			0: 10 bit 1: 12 bit
15h	[3:0]	MODE	0h	2h						UXGA mode
17h	[7:0]	VMAX	4E6h	4E6h						1254 line
18h	[3:0]									
1Ah	[7:0]	HMAX	1CEh	168h	2D0h	5A0h	1CEh	39Ch	738h	
1Bh	[7:0]									
1Ch	[0]	ODBIT	1	0			1			0: 10 bit 1: 12 bit
	[6:4]	OPORTSEL	1h	1h						8 ch LVDS
				N/A	3h		N/A	3h		4 ch LVDS
				N/A	N/A	4h	N/A	N/A	4h	2 ch LVDS
1Fh	[7:0]	CKSEL	00h	00h						
21h	[1:0]	FREQ	0h	0h	1h	2h	0h	1h	2h	8 ch LVDS
				N/A	0h	1h	N/A	0h	1h	4 ch LVDS
				N/A	N/A	0h	N/A	N/A	0h	2 ch LVDS
92h	[7:0]	INCKSEL0	20h	20h						
93h	[7:0]	INCKSEL1	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
95h	[7:0]	INCKSEL2	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
A0h	[7:0]	GTWAIT	A4h	A4h						
A5h	[7:0]	GSDLY	08h	08h						



Pixel Array Image Drawing in UXGA Mode

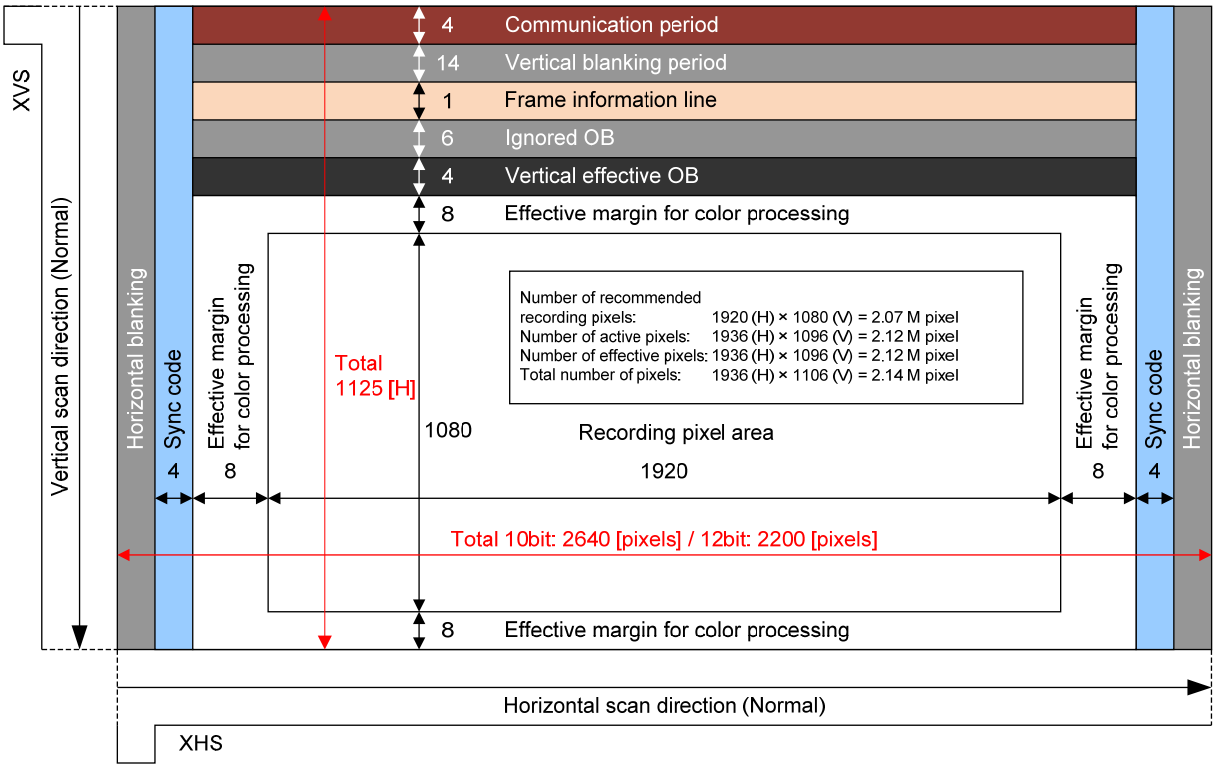


Drive Timing Chart for Serial Output in UXGA Mode

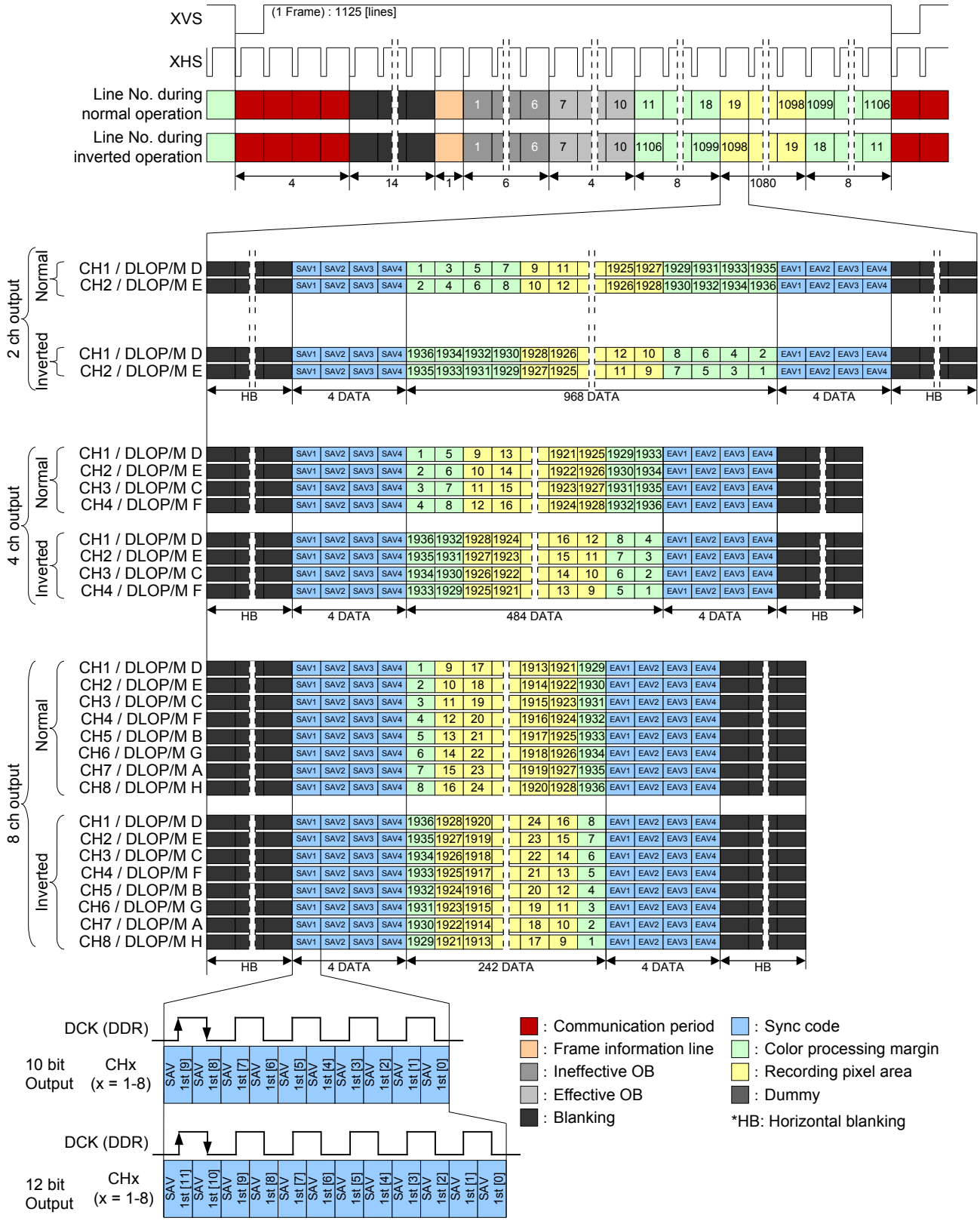
1080p-Full HD mode

Register List of 1080p-Full HD mode

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 10 bit			AD = 12 bit			
				120 [frame/s]	60 [frame/s]	30 [frame/s]	120 [frame/s]	60 [frame/s]	30 [frame/s]	
Chip ID = 02h										
05h	[7:4]	STBLVDS	0h	0h						8 ch LVDS
				N/A	1h		N/A	1h		4 ch LVDS
				N/A	N/A	2h	N/A	N/A	2h	2 ch LVDS
14h	[0]	ADBIT	1	0			1			0: 10 bit 1: 12 bit
15h	[3:0]	MODE	0h	4h						1080p-Full HD mode
17h	[7:0]	VMAX	4E6h	465h						1125 line
18h	[3:0]									
1Ah	[7:0]	HMAX	1CEh	226h	44Ch	898h	226h	44Ch	898h	
1Bh	[7:0]									
1Ch	[0]	ODBIT	1	0			1			0: 10 bit 1: 12 bit
	[6:4]	OPORTSEL	1h	1h						8 ch LVDS
				N/A	3h		N/A	3h		4 ch LVDS
				N/A	N/A	4h	N/A	N/A	4h	2 ch LVDS
1Fh	[7:0]	CKSEL	00h	01h						
21h	[1:0]	FREQ	0h	0h	1h	2h	0h	1h	2h	8 ch LVDS
				N/A	0h	1h	N/A	0h	1h	4 ch LVDS
				N/A	N/A	0h	N/A	N/A	0h	2 ch LVDS
92h	[7:0]	INCKSEL0	20h	18h						
93h	[7:0]	INCKSEL1	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
95h	[7:0]	INCKSEL2	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
A0h	[7:0]	GTWAIT	A4h	64h						
A5h	[7:0]	GSDLY	08h	04h						



Pixel Array Image Drawing in 1080p-Full HD Mode



Drive Timing Chart for Serial Output in 1080p-Full HD Mode

ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 16 areas that specified by horizontal 4 points and vertical 4 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from WUXGA mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (4, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 4)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.

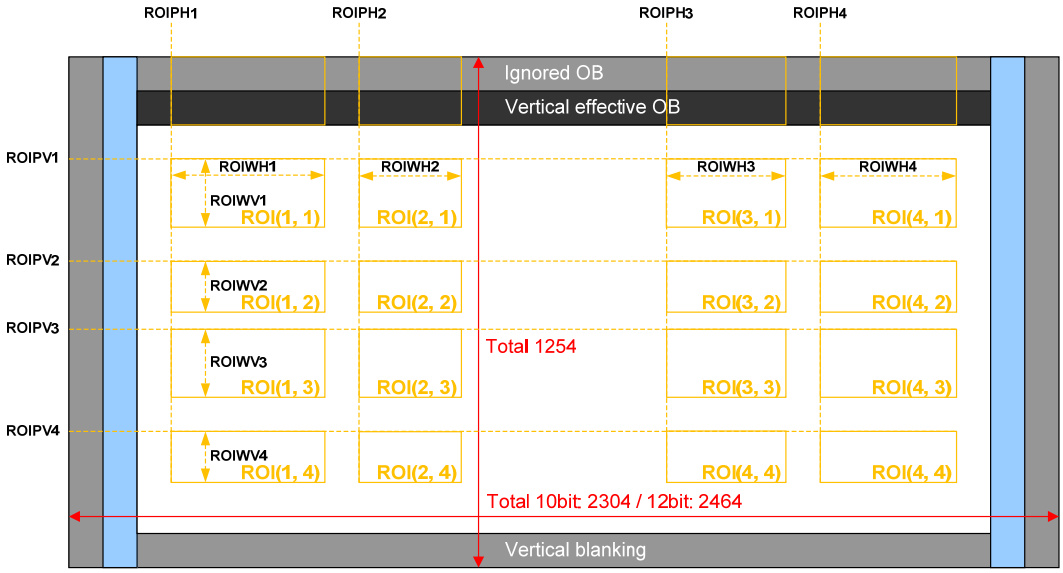
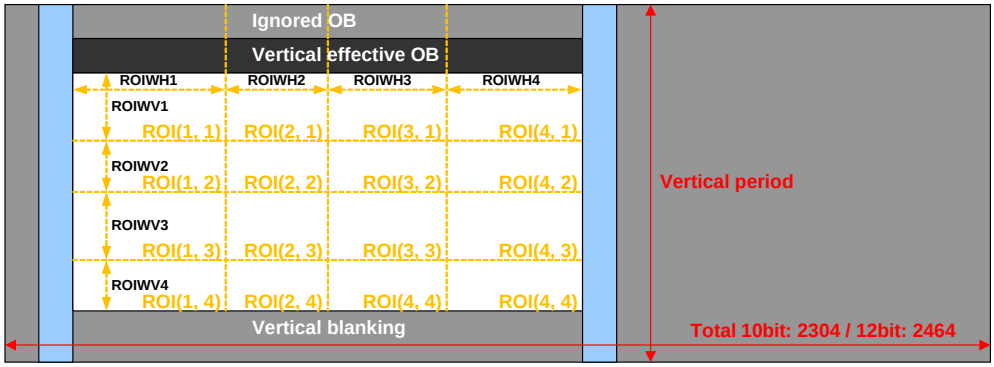


Image Drawing of Designated Areas in ROI Mode



Details of Image Drawing

Register List of ROI mode

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 10 bit			AD = 12 bit			
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
05h	[7:4]	STBLVDS	0h	0h						8 ch LVDS
				N/A	1h		N/A	1h		4 ch LVDS
				N/A	N/A	2h	N/A	N/A	2h	2 ch LVDS
14h	[0]	ADBIT	1	0			1			0: 10 bit 1: 12 bit
15h	[3:0]	MODE	0h	0h						WUXGA mode
17h	[7:0]	VMAX	4E6h	*1	*2	*3	*4	*5	*6	
18h	[3:0]									
1Ah	[7:0]	HMAX	1CEh	168h	2D0h	5A0h	1CEh	39Ch	738h	
1Bh	[7:0]									
1Ch	[0]	ODBIT	1	0			1			0: 10 bit 1: 12 bit
	[6:4]	OPORTSEL	1h	1h						8 ch LVDS
				N/A	3h		N/A	3h		4 ch LVDS
				N/A	N/A	4h	N/A	N/A	4h	2 ch LVDS
1Fh	[7:0]	CKSEL	00h	00h						
21h	[1:0]	FREQ	0h	0h	1h	2h	0h	1h	2h	8 ch LVDS
				N/A	0h	1h	N/A	0h	1h	4 ch LVDS
				N/A	N/A	0h	N/A	N/A	0h	2 ch LVDS
92h	[7:0]	INCKSEL0	20h	20h						
93h	[7:0]	INCKSEL1	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
95h	[7:0]	INCKSEL2	00h	INCK = 37.125 MHz: 00h INCK = 74.25 MHz: 04h						
A0h	[7:0]	GTWAIT	A4h	A4h						
A5h	[7:0]	GSDLY	08h	08h						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 10 bit			AD = 12 bit			
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 03h										
00h	[0]	ROIH1ON	0	The horizontal setting of ROI area (1, y) (y = 1 to 4) 0: Disable 1: Enable						
	[1]	ROIV1ON	0	The vertical setting of ROI area (x, 1) (x = 1 to 4) 0: Disable 1: Enable						
01h	[7:0]	ROIPH1	000h	Designation of horizontal cropping position on area (1, y) (y = 1 to 4)						
02h	[2:0]									
03h	[7:0]	ROIPV1	000h	Designation of vertical cropping position on area (x, 1) (x = 1 to 4)						
04h	[2:0]									
05h	[7:0]	ROIWH1	000h	Designation of horizontal cropping size on area (1, y) (y = 1 to 4)						
06h	[2:0]									
07h	[7:0]	ROIWV1	000h	Designation of vertical cropping size on area (x, 1) (x = 1 to 4)						
08h	[2:0]									
09h	[0]	ROIH2ON	0	The horizontal setting of ROI area (2, y) (y = 1 to 4) 0: Disable 1: Enable						
	[1]	ROIV2ON	0	The vertical setting of ROI area (x, 2) (x = 1 to 4) 0: Disable 1: Enable						
0Ah	[7:0]	ROIPH2	000h	Designation of horizontal cropping position on area (2, y) (y = 1 to 4)						
0Bh	[2:0]									
0Ch	[7:0]	ROIPV2	000h	Designation of vertical cropping position on area (x, 2) (x = 1 to 4)						
0Dh	[2:0]									
0Eh	[7:0]	ROIWH2	000h	Designation of horizontal cropping size on area (2, y) (y = 1 to 4)						
0Fh	[2:0]									
10h	[7:0]	ROIWV2	000h	Designation of vertical cropping size on area (x, 2) (x = 1 to 4)						
11h	[2:0]									
12h	[0]	ROIH3ON	0	The horizontal setting of ROI area (3, y) (y = 1 to 4) 0: Disable 1: Enable						
	[1]	ROIV3ON	0	The vertical setting of ROI area (x, 3) (x = 1 to 4) 0: Disable 1: Enable						
13h	[7:0]	ROIPH3	000h	Designation of horizontal cropping position on area (3, y) (y = 1 to 4)						
14h	[2:0]									
15h	[7:0]	ROIPV3	000h	Designation of vertical cropping position on area (x, 3) (x = 1 to 4)						
16h	[2:0]									
17h	[7:0]	ROIWH3	000h	Designation of horizontal cropping size on area (3, y) (y = 1 to 4)						
18h	[2:0]									
19h	[7:0]	ROIWV3	000h	Designation of vertical cropping size on area (x, 3) (x = 1 to 4)						
1Ah	[2:0]									
1Bh	[0]	ROIH4ON	0	The horizontal setting of ROI area (4, y) (y = 1 to 4) 0: Disable 1: Enable						
	[1]	ROIV4ON	0	The vertical setting of ROI area (x, 4) (x = 1 to 4) 0: Disable 1: Enable						
1Ch	[7:0]	ROIPH4	000h	Designation of horizontal cropping position on area (4, y) (y = 1 to 4)						
1Dh	[2:0]									
1Eh	[7:0]	ROIPV4	000h	Designation of vertical cropping position on area (x, 4) (x = 1 to 4)						
1Fh	[2:0]									
20h	[7:0]	ROIWH4	000h	Designation of horizontal cropping size on area (4, y) (y = 1 to 4)						
21h	[2:0]									
22h	[7:0]	ROIWV4	000h	Designation of vertical cropping size on area (x, 4) (x = 1 to 4)						
23h	[2:0]									

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
  ROIPH1 + ROIWH1 < ROIPH2
  ROIPH2 + ROIWH2 < ROIPH3
  ROIPH3 + ROIWH3 < ROIPH4
  ROIPH4 + ROIWH4 < 1936d

  ROIPV1 + ROIWV1 < ROIPV2
  ROIPV2 + ROIWV2 < ROIPV3
  ROIPV3 + ROIWV3 < ROIPV4
  ROIPV4 + ROIWV4 < 1216d

* Set the horizontal and vertical setting in even number

Frame rate on ROI mode

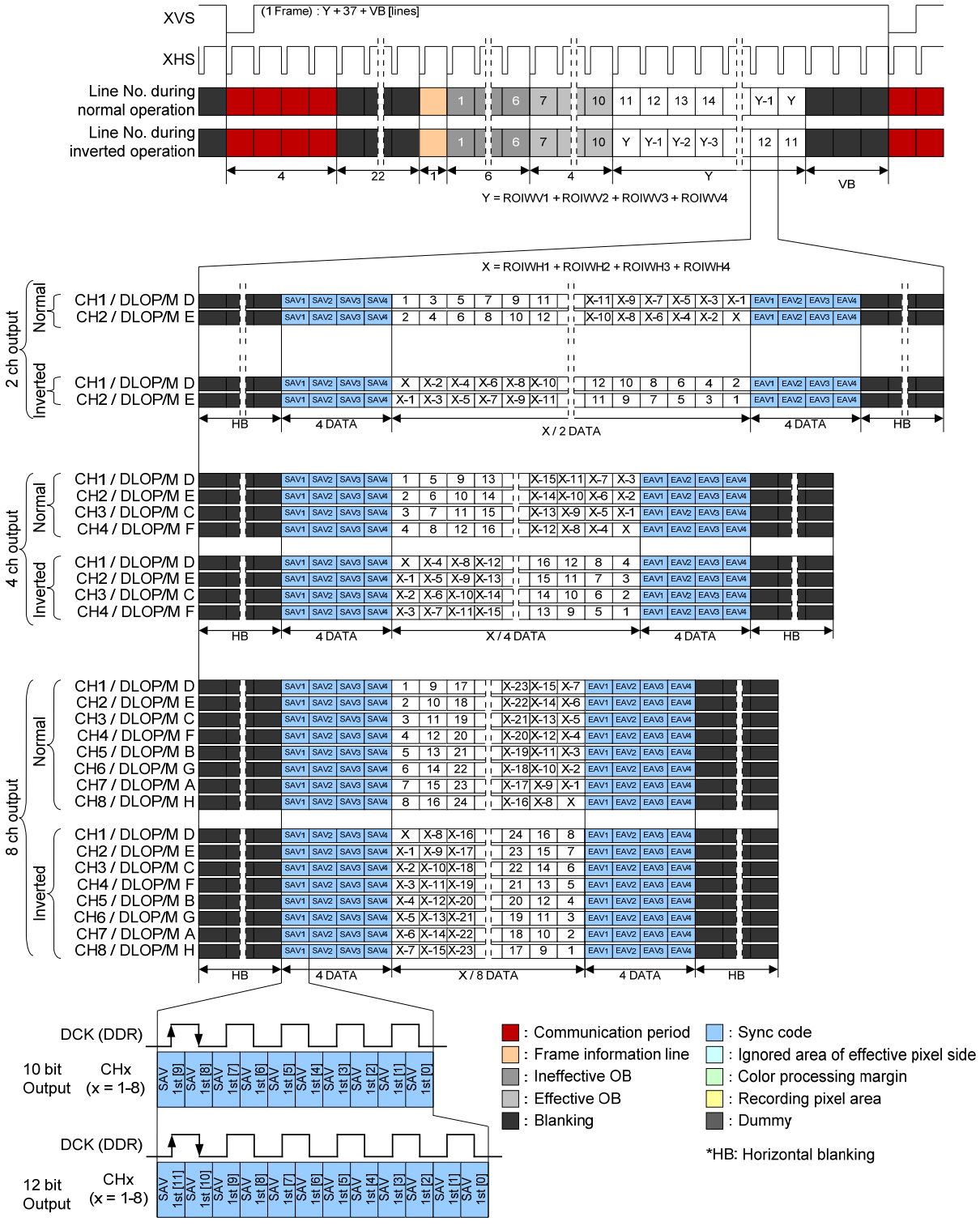
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

* Number of lines per frame or VMAX = ROIWV1 + ROIWV2 + ROIWV3 + ROIWV4 + 37
* 1 period: Change according to the data rate settings and the number of LVDS channels. Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
ROIWV1 + ROIWV2 + ROIWV3 + ROIWV4 = 600
ROIWV1 + ROIWV2 + ROIWV3 + ROIWV4 = 2 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [µs]	Frame rate [frame/s]	
		Total number of ROI: 600 [line]	Total number of ROI: 2 [line]
*1	4.849	323.8	5288.5
*2	9.697	161.9	2644.2
*3	19.394	80.9	1322.1
*4	6.222	252.3	4120.9
*5	12.444	126.1	2060.4
*6	24.889	63.1	1030.2



Drive Timing Chart for Serial Output in ROI Mode

Description of Various Function

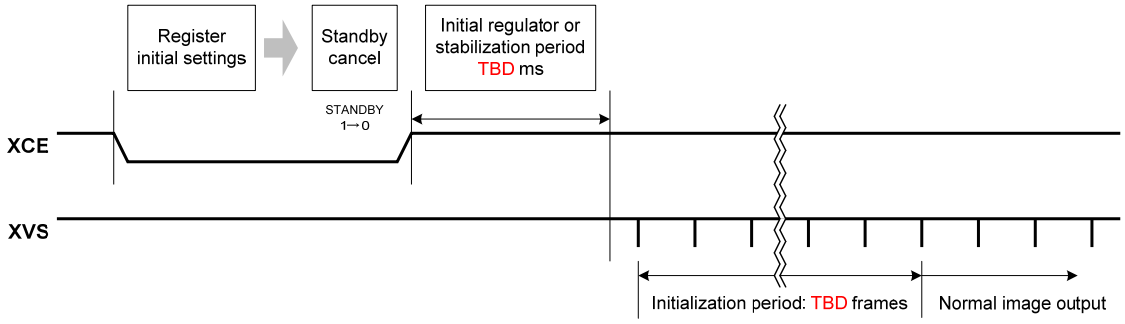
Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address	bit			
STANDBY	02h	00h	[0]	1h	1h: Standby 0h: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
After standby mode is canceled, a normal image is output from the TBD frames after internal regulator stabilization (TBD ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [11:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.

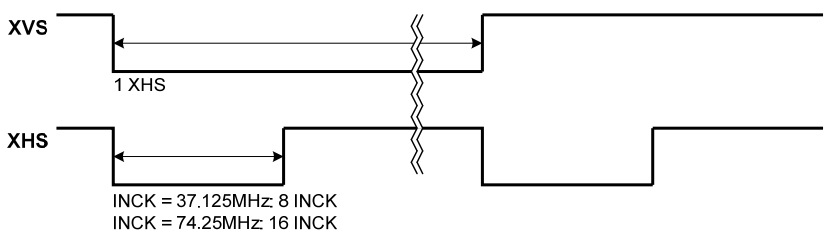
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address	Bit			
XMSTA	02h	12h	[0]	1h	1h: Master operation ready (Initial value) 0h: Master operation start	The master operation starts by setting 0.
VMAX [11:0]		17h	[7:0]	4E6h	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		18h	[3:0]			
HMAX [15:0]		1Ah	[7:0]	01CEh	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		1Bh	[7:0]			
XVSOUTSEL [1:0]		2Eh	[1:0]	0h	0h: High level output 2h: VSYNC output Other: Setting prohibited	Set to 2h in master mode Set to 0h in slave mode
XHSOUTSEL [1:0]			[3:2]	0h	0h: High level output 2h: HSYNC output Other: Setting prohibited	Set to 2h in master mode Set to 0h in slave mode

XVS / XHS Output Waveform in Master Mode



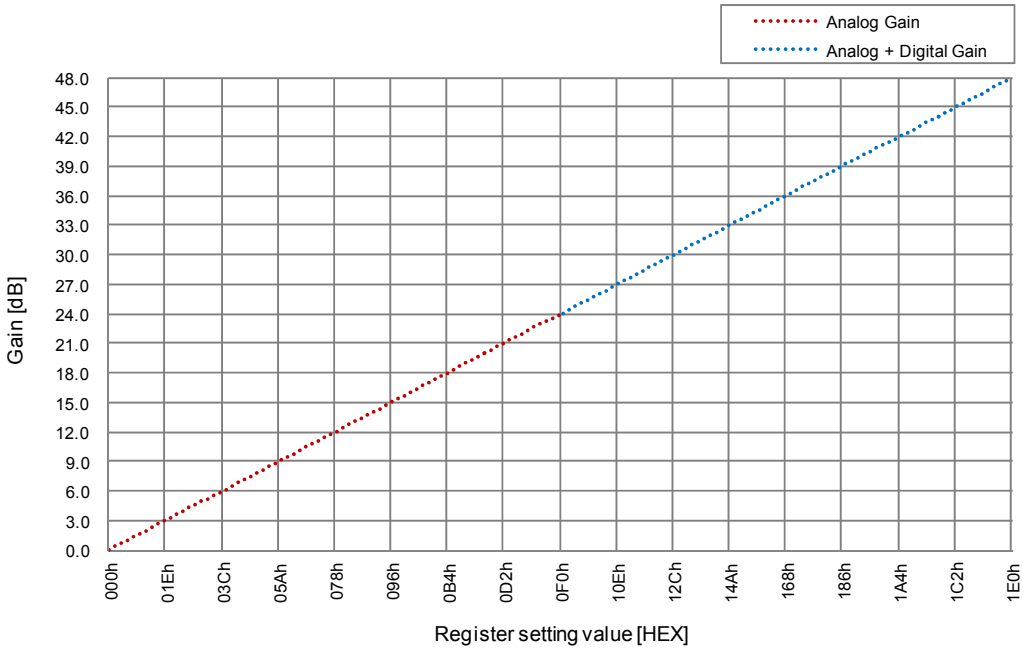
Gain Adjustment Function

PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.
The value which is ten times the gain is set to register.

Example)
When set to 6 dB:

6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address	bit		Setting range	
GAIN [8:0]	04h	04h	[7:0]	000h	000h to 1E0h (0d to 480d)	Setting value: Gain [dB] × 10
		05h	[0]			

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL register. When the BLKLEVEL [8:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  10 bit output: 03Ch (60 d)
  12 bit output: 0F0h (240 d)

Register List of Black level adjustment

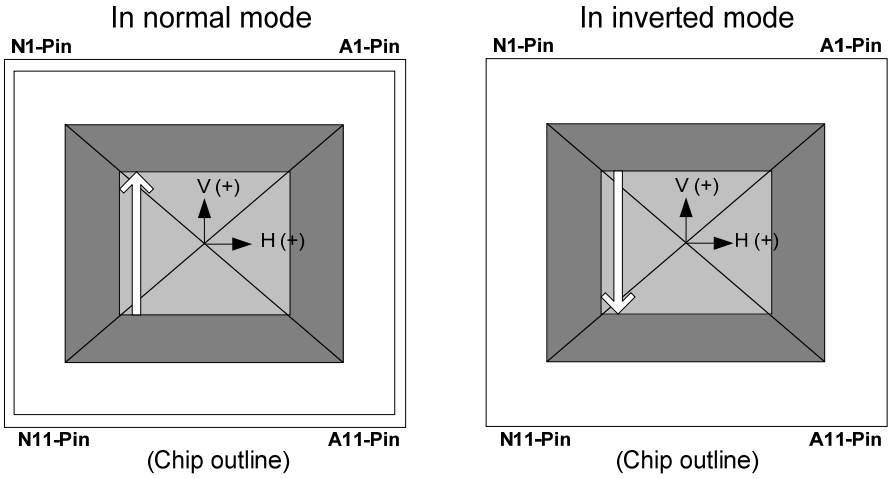
Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
BLKLEVEL	04h	58h	[7:0]	0F0h	000h to 1FFh
		59h	[0]		

Horizontal / Vertical Normal Operation and Inverted Operation

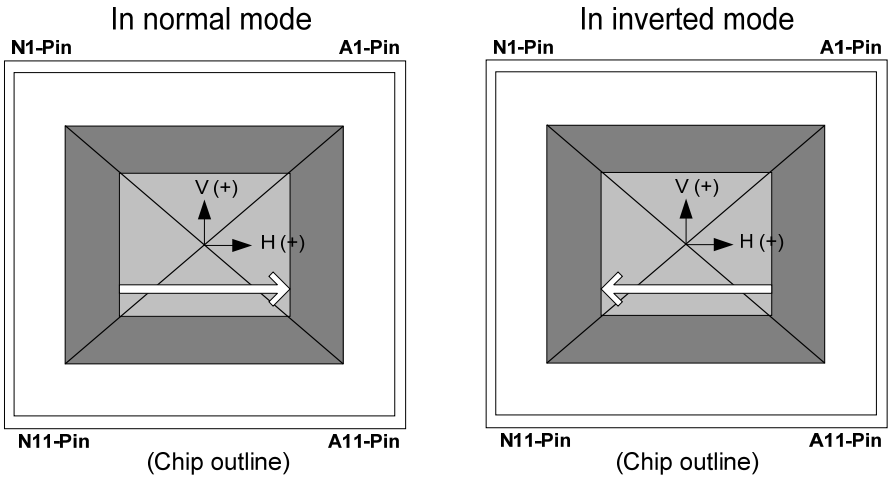
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
VREVERSE	02h	16h	[0]	0h	0h: Normal (Initial value) 1h: Inverted
HREVERSE			[1]	0h	0h: Normal (Initial value) 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a global shutter function that integrates to the all line collectively by using memory in each pixel. This sensor has a variable electronic shutter function that can control the integration time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal. This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

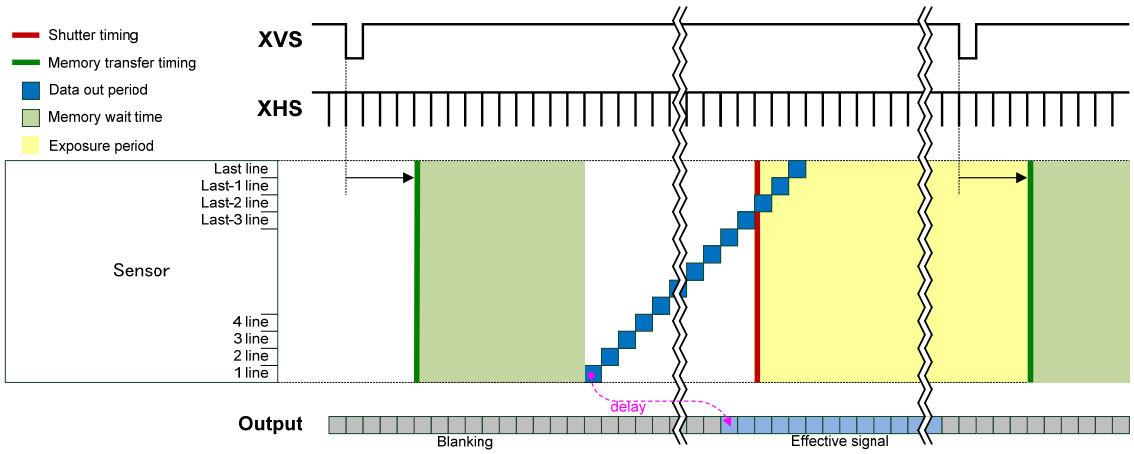


Image Drawing of Global Shutter (Normal mode) Operation

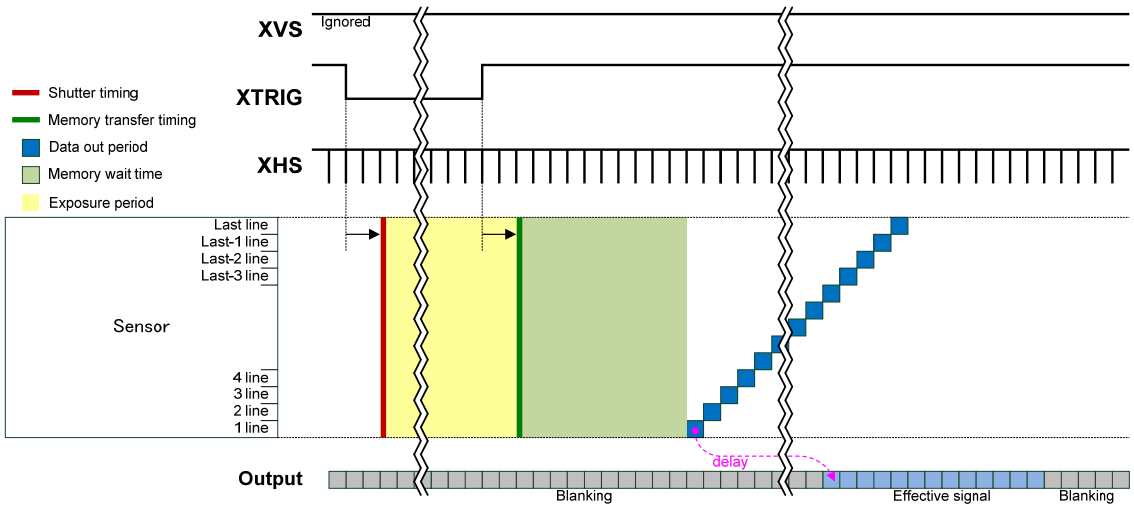


Image Drawing of Global Shutter (Trigger mode) Operation

Global Shutter (Normal Mode) Operation

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS [11:0] register. For setting value of SHS [11:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [11:0] register. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposire time [s] = (1 H period) × (Number of lines per frame - SHS) + 13.73 [μs][*1]

[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
VMAX [11:0]	02h	17h	[7:0]	4E6h	Set the number of lines per frame (only in master mode)
		18h	[3:0]		
SHS [11:0]		9Ah	[7:0]	000h	Sets the shutter sweep time. memory wait time to (Number of lines per frame - 1)
		9Bh	[3:0]		

List of Exposure Setting

Drive mode	memory wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	8 ch LVDS / Maximum frame rate			
					Frame rate [frame/s]		Actually exposure [ms]	
					10 bit	12 bit	10 bit	12 bit
WUXGA UXGA	10	1254	1253	1	164.5	128.2	0.019	0.020
			10	1244			6.045	7.754
1080p-Full HD	6	1125	1124	1	120		0.021	
			6	1119			8.303	
ROI	10	V_{TR} [*1]	V_{TR}-1	1	[*2]		0.019	0.020
			10	V_{TR}-10			[*3]	

[*1] V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + ROIWV4 + 37

[*2] For the frame rate, see the section “ROI mode” in “Readout Drive Mode”.

[*3] Conform to the calculation formura of exposure time. (Number of lines per frame = V_{TR})

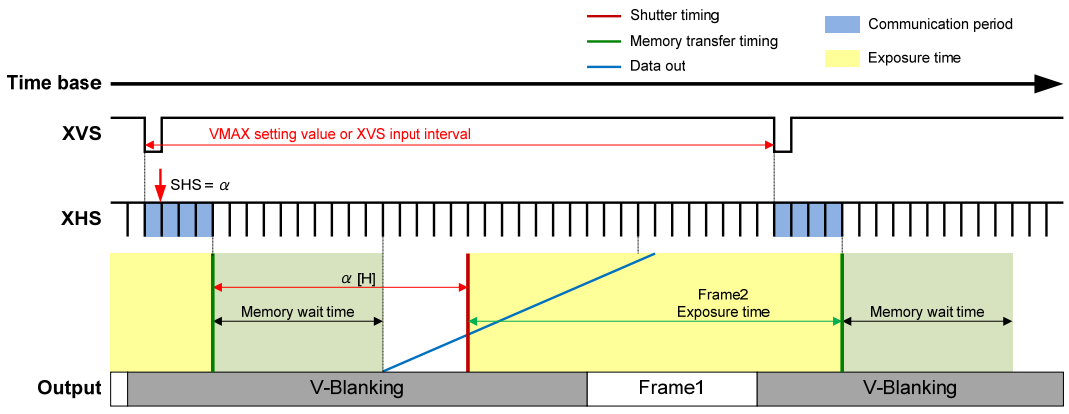


Image Drawing of Global Shutter (Normal Mode)

Global Shutter (Tigger Mode) Operation

The integration time can be controlled by varying the pulse width that is input to XTRIG pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to trigger mode, set 1 to the register TRIGEN. The XVS input signal is ignored during trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{GES}) based on the previous trigger rise.
When the trigger rise is input before the rise input prohibited period (t_{TGPD}), the frame currently being input becomes invalid and storage starts over again. (Interrupt operation)
This fuction is slave mode only. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width) + 13.73 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
TRIGEN	02h	13h	[0]	0h	0h: Global shutter (normal mode) 1h: Global shutter (trigger mode)

Parameter List of Global Shutter (Trigger Mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Integration start delay	t_{TGST}	2	—	3	H
Integration end delay	t_{TGED}	2 + t_{OFFSET}	—	3 + t_{OFFSET}	H
Integration time	t_{TGSE}	1	—	—	H
Next trigger fall prohibited period	t_{TGES}	1	—	—	H
Next trigger rise prohibited period (WUXGA / UXGA)	t_{TGPD}	1254	—	—	H
Next trigger rise prohibited period (1080p Full-HD)		1125	—	—	
Next trigger rise prohibited period (ROI)		V_{TR} [*1]	—	—	
Data output delay (WUXGA / UXGA / ROI)	t_{TGDLY}	—	25	—	H
Data output delay (1080p-Full HD)		—	17	—	

[*1] V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + ROIWV4 + 37

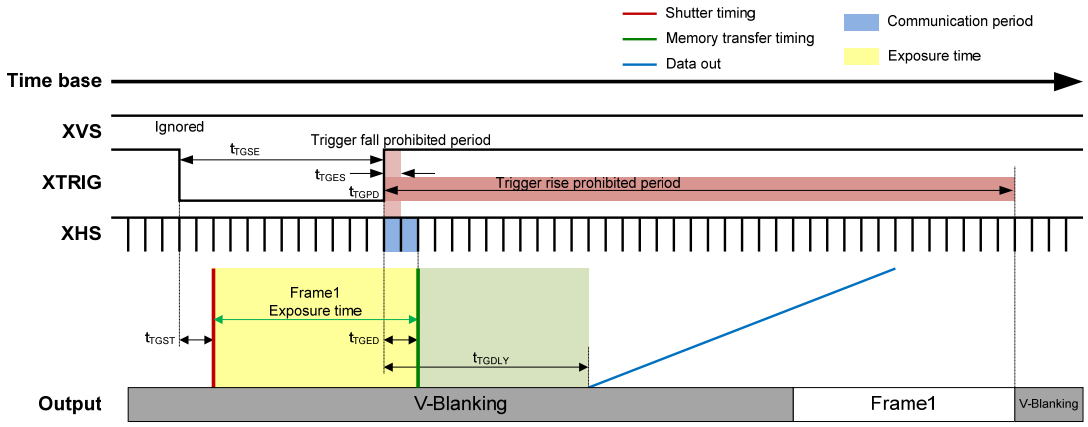


Image Drawing of Global Shutter (Trigger Mode)

Interrupt Operation

The image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame1 in the figure below), Frame1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)

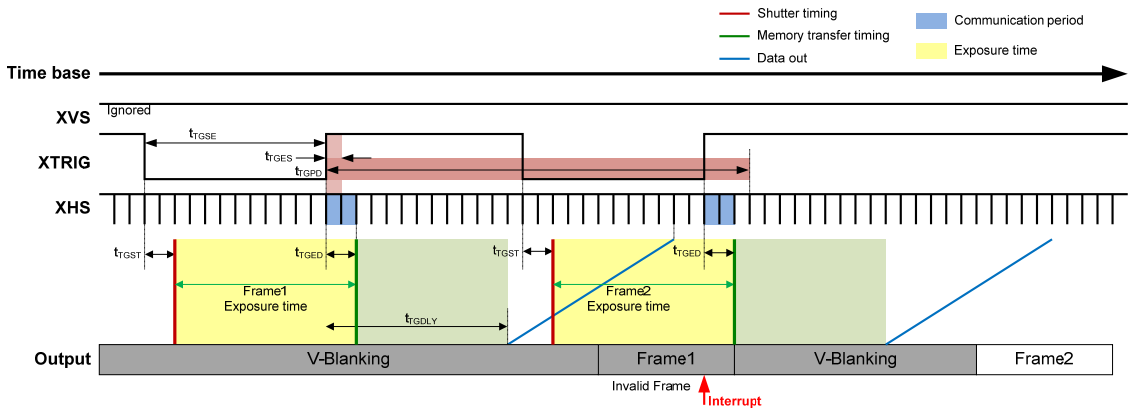


Image Drawing of Interrupt Operation in Global Shutter (Trigger Mode)

Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGEN. The sensor will transition to normal mode or trigger mode 20H after the register TRIGEN is set. (The XVS and XTRIG input during transition are prohibited.)

Transition from Normal Mode to Trigger Mode

The sensor will transition from normal mode to trigger mode after setting 1d to register TRIGEN. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a 20H period after the register TRIGEN is set. When TRIGEN is set during data read, read operation is stopped and that frame becomes an invalid frame.
* The communication is available till 9 H period only when sensor transition to the Trigger mode.

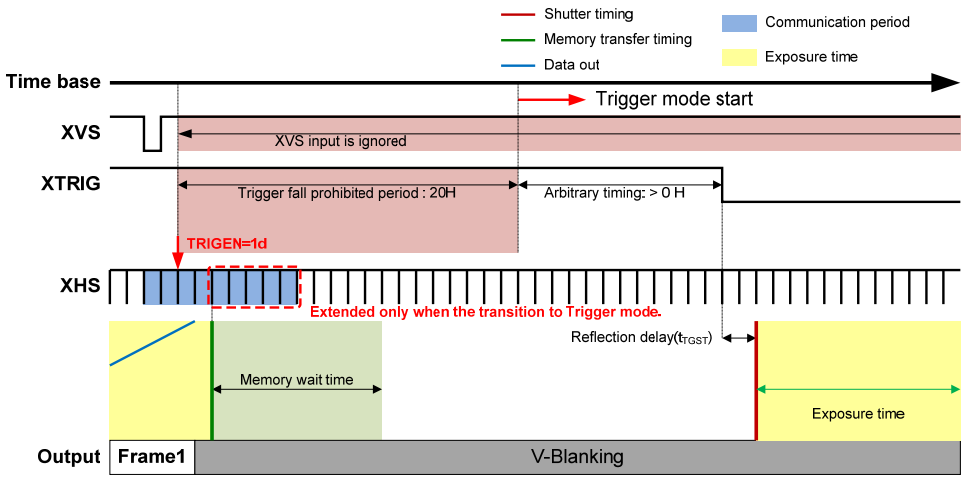


Image Drawing of Transition from Normal Mode to Trigger Mode

Transition from Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting 0d to register TRIGEN. Start XVS input after transition to normal mode. Set TRIGEN after Next trigger rise prohibited period (t_{TGPD}) has passed. When TRIGEN is set before t_{TGPD}, read operation is stopped and that frame becomes an invalid frame.

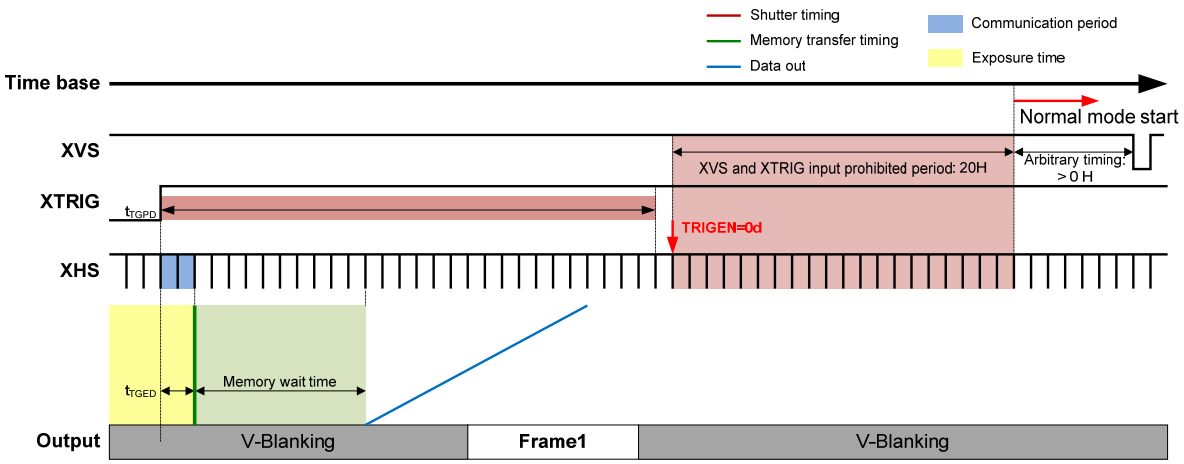


Image Drawing of Transition from Normal Mode to Trigger Mode

Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation. The pulse output from TOUT1 pin and TOUT2 pin. The rise timing and fall timing of pulse are set by Register. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the “List of Reference point".

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
TOUT1SEL [1:0]	02h	2Fh	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [2:0]		32h	[2:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [2:0]			[6:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR		76h	[0]	0	Pulse1 enable in normal mode 0: disable 1: eneble
PULSE1_EN_TRIG			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [15:0]		77h	[7:0]	0000h	Pulse1 active period start timing setting Designated in line units from reference point
		78h	[7:0]		
PULSE1_DN [15:0]		7Ah	[7:0]	0000h	Pulse1 active period end timing setting Designated in line units from reference point
		7Bh	[7:0]		
PULSE2_EN_NOR		7Eh	[0]	0	Pulse2 enable in normal mode 0: disable 1: eneble
PULSE2_EN_TRIG			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
PULSE2_UP [15:0]		7Fh	[7:0]	0000h	Pulse2 active period start timing setting Designated in line units from reference point
		80h	[7:0]		
PULSE2_DN [15:0]		82h	[7:0]	0000h	Pulse2 active period end timing setting Designated in line units from reference point
		83h	[7:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge	Exposure start (shutter) timing
Reference point of Pulse2		Memory transfer timing

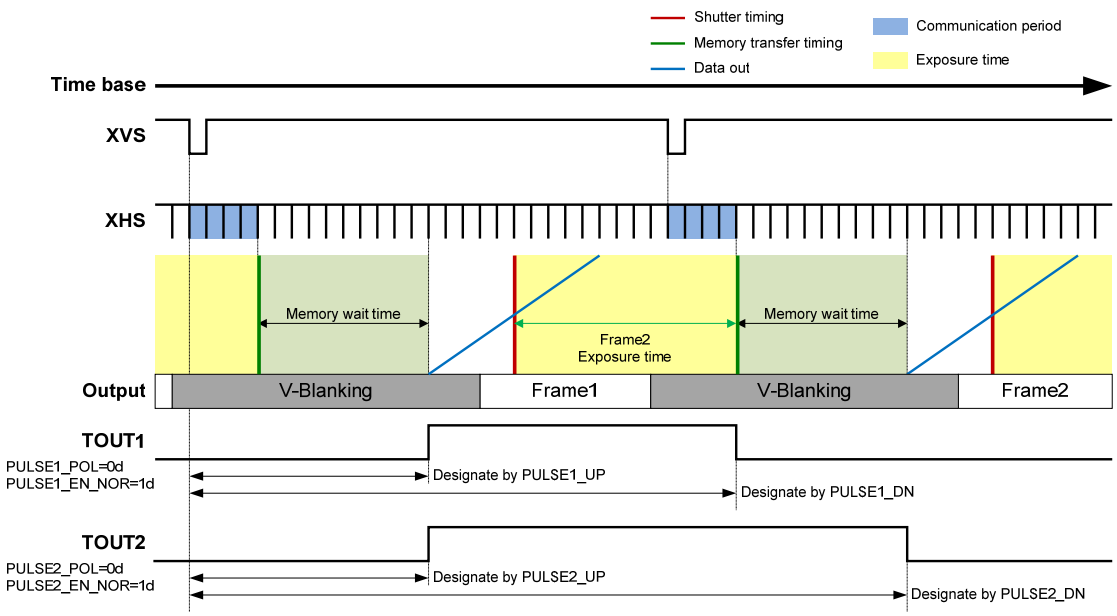


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

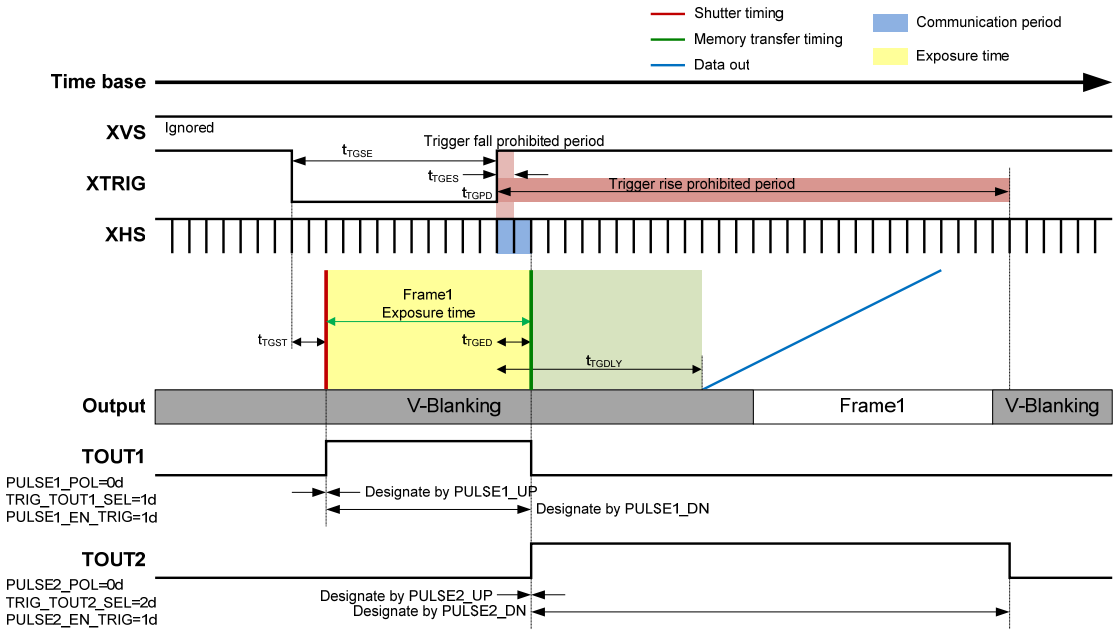


Image Drawing of Pulse Output Function in Global Shutter (Trigger Mode)

Signal Output

Output Pin Settings

This sensor supports Low voltage LVDS serial (2 ch / 4 ch / 8 ch switching) DDR output.
In addition, the data rate per channel is adjustable. The table below shows the output format settings.

Register List of Output Settings

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
STBLVDS	02h	05h	[7:4]	0h	The un-using LVDS channel go into standby
OPORTSEL [2:0]		1Ch	[6:4]	1h	Number of output channel setting (Refer the list of output setting below)
FREQ [1:0]		21h	[1:0]	0h	Frame rate adjust (Refer the list of output setting below)

List of Output Setting

Drive mode	Register setting			Number of LVDS channel	Data rate per channel [Mbps/ch]	Total data rate [Gbps]
	STBLVDS	OPORTSEL	FREQ			
WUXGA UXGA ROI	0h	1h	0h	8 ch	594	4.752
			1h		297	2.376
			2h		148.5	1.188
	1h	3h	0h	4 ch	594	2.376
			1h		297	1.188
	2h	4h	0h	2 ch	594	1.188
1080p-Full HD	0h	1h	0h	8 ch	445.5	3.564
			1h		222.75	1.782
			2h		111.375	0.891
	1h	3h	0h	4 ch	445.5	1.782
			1h		222.75	0.891
	2h	4h	0h	2 ch	445.5	0.891

Each output pin is shown in the table below when setting low-voltage LVDS serial 2 ch / 4 ch / 8 ch output.
In 2 ch and 4 ch output, set the un-using channels to standby.

Output Pins for Low Voltage LVDS Serial

Output pins	Low voltage LVDS serial DDR output		
	2 ch	4 ch	8 ch
DLOPA / DLOMA	Hi-Z	Hi-Z	Ch 7
DLOPB / DLOMB	Hi-Z	Hi-Z	Ch 5
DLOPC / DLOMC	Hi-Z	Ch 3	Ch 3
DLOPD / DLOMD	Ch 1	Ch 1	Ch 1
DLOPE / DLOME	Ch 2	Ch 2	Ch 2
DLOPF / DLOMF	Hi-Z	Ch 4	Ch 4
DLOPG / DLOMG	Hi-Z	Hi-Z	Ch 6
DLOPH / DLOMH	Hi-Z	Hi-Z	Ch 8

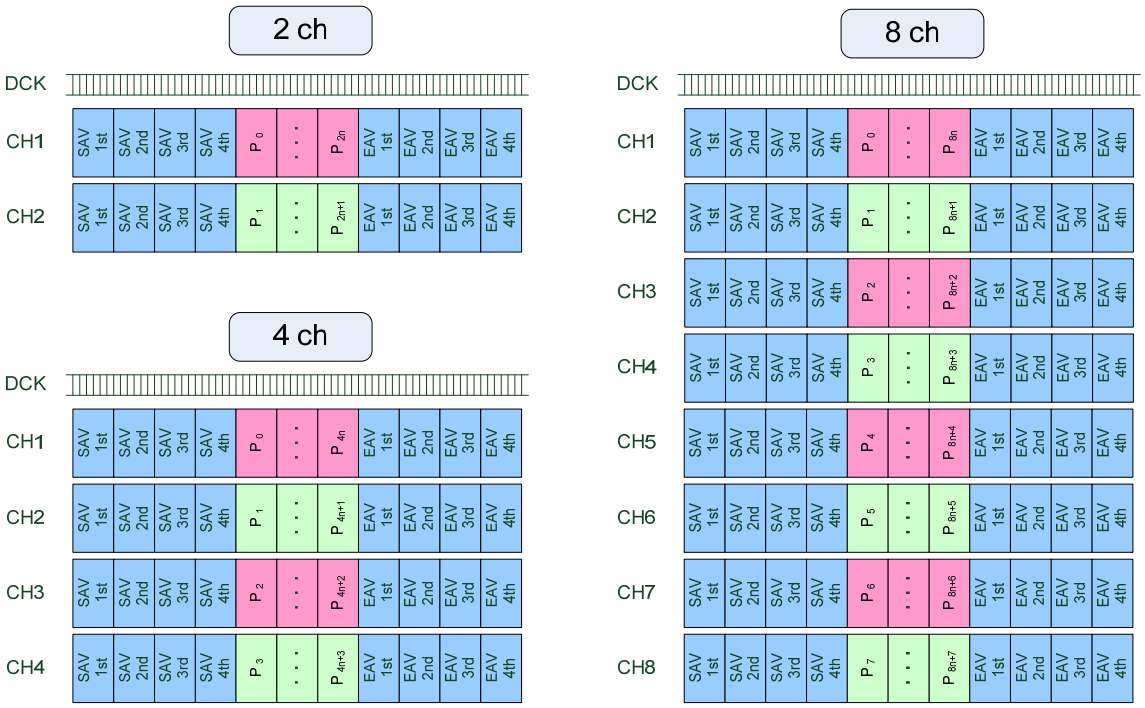
Low-voltage LVDS serial 2 ch / 4 ch / 8 ch output format is shown in the figure below.

When setting 2 ch, after four data of SAV is output in the order of CH1 and CH2 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 and CH2 respectively.

When setting 4 ch, after four data of SAV is output in the order of CH1, CH2, CH3 and CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1, CH2, CH3 and CH4 respectively.

When setting 8 ch, output in a format similar to the 2 ch and 4 ch output as shown below.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Readout Drive Mode".



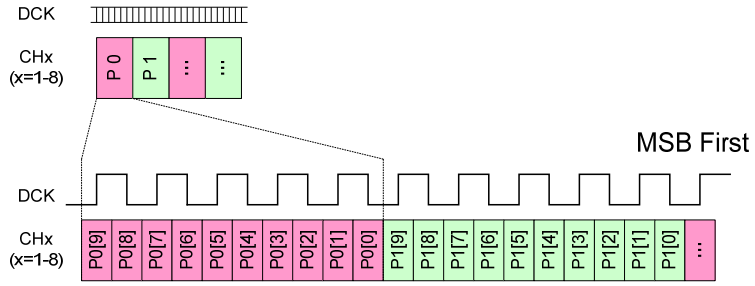
Output Format of Low voltage LVDS Serial 2 ch / 4 ch / 8 ch

Output Pin Bit Width Selection

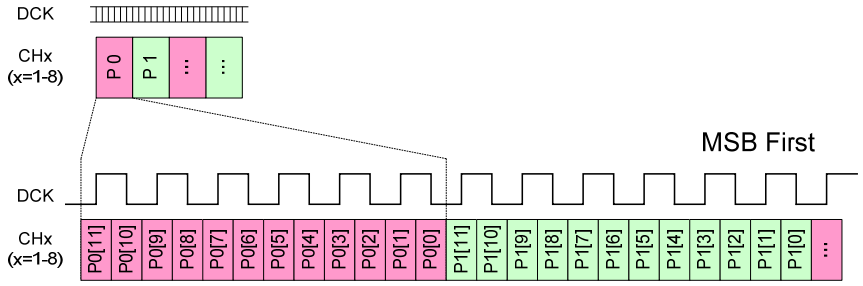
The output pin width can be selected from 10-bit or 12-bit output using register ADBIT, ODBIT. Sync code is output according to bit width setting of these register.

Register List of Bit Width Selection

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address	bit			
ADBIT	02h	14h	[0]	1h	0h: 10 bit 1h: 12 bit	Set same value to both ADBIT and ODBIT
ODBIT		1Ch	[0]	1h	0h: 10 bit 1h: 12 bit	



Example of Data format in low-voltage LVDS serial 10-bit output



Example of Data format in low-voltage LVDS serial 12-bit output

Output Signal Range

The sensor output has either a 10-bit or 12-bit gradation, but output is not performed over the full range, and the maximum output value is the “3FFh - 1” (10-bit output) and the “FFFh - 1” (12-bit output). The minimum value is 001h. The output range for each output gradation is shown in the table below. The maximum level and the mimimum level are output only in the sync code. See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range

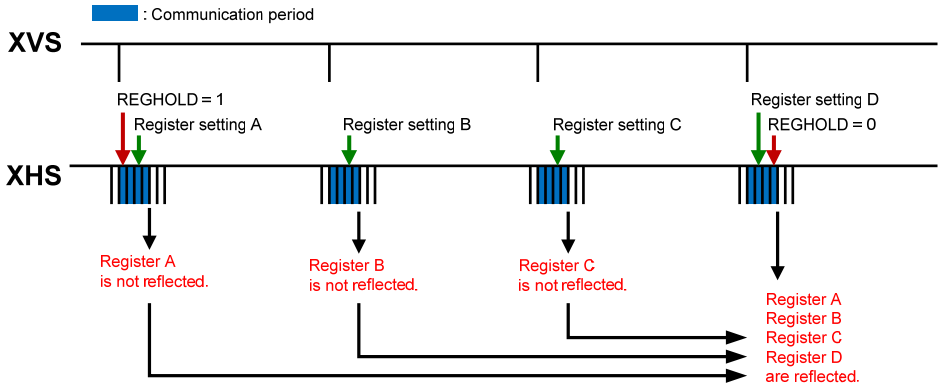
Output gradation	Output value	
	Min.	Max.
10 bit	001h	3FEh
12 bit	001h	FFEh

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address	bit		
REGHOLD	02h	0Ch	[0]	1h	0h: Invalid 1h: Valid (Register hold)



Register Hold Setting

Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
ROI	→	WUXGA	Via the Standby state is unnecessary
	→	UXGA	
WUXGA	→	ROI	
UXGA	→		
- Transition between modes other than the above - Change the input frequency of INCK - Change the data rate (change the register FREQ) - Change the number of output channels (change the register OPORTSEL) - Change the bit width (change the register ADBIT, ODBIT)			Via the standby state is necessary

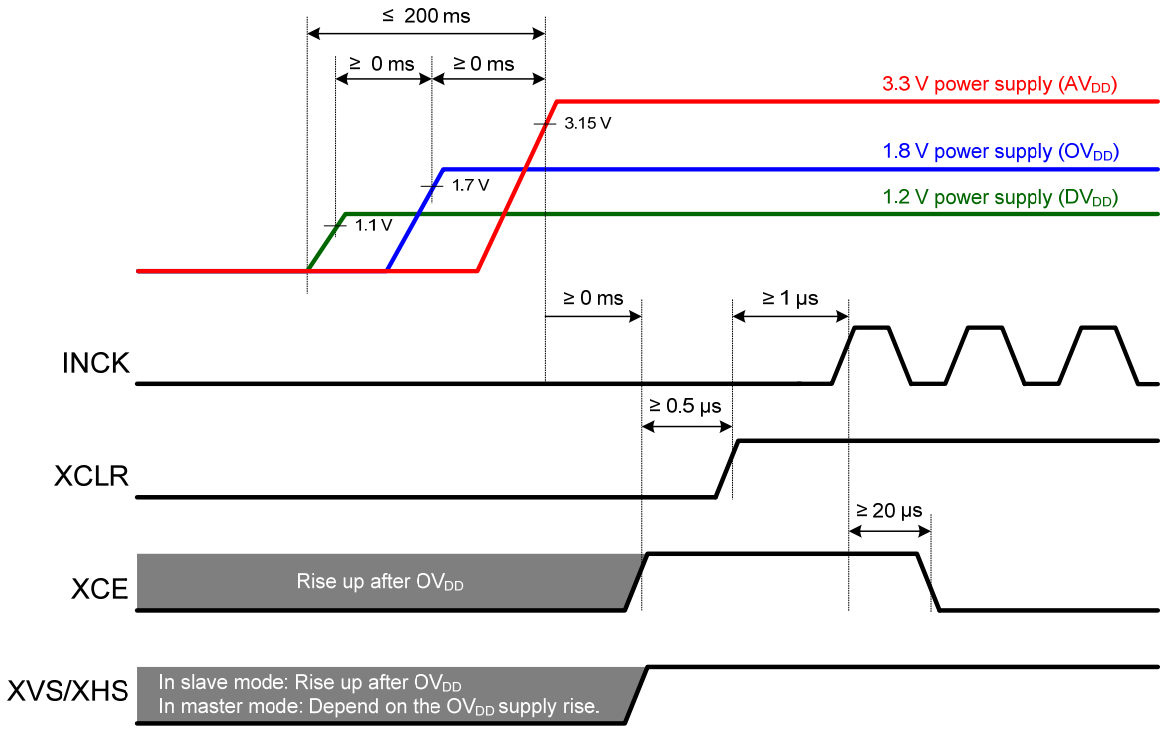
*1 When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Power-on and Power-off Sequence

Power-on sequence

Follow the sequence below to turn On the power supplies.

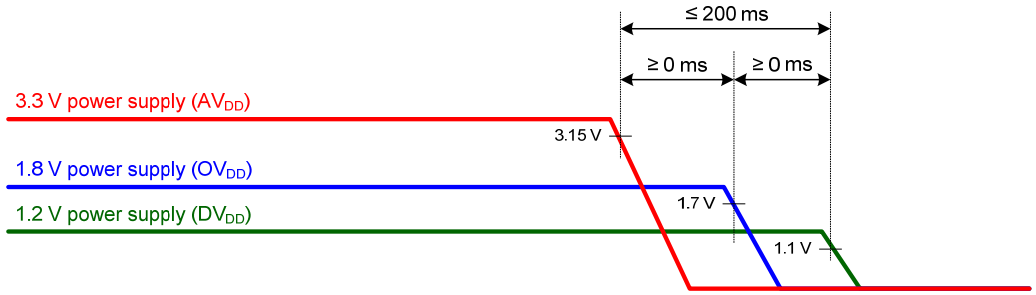
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after the system clear. A period of 0 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE.



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

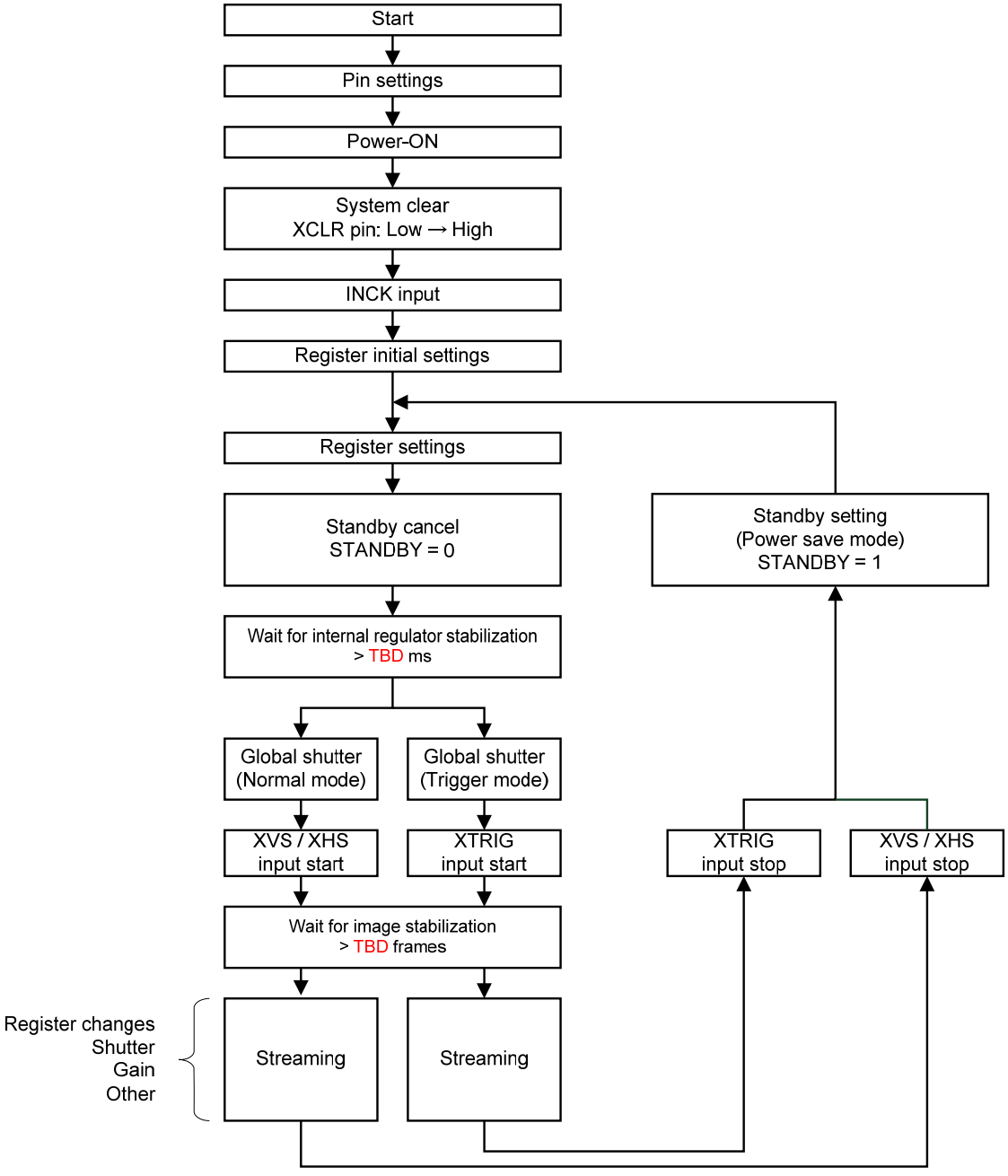


Power-off Sequence

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

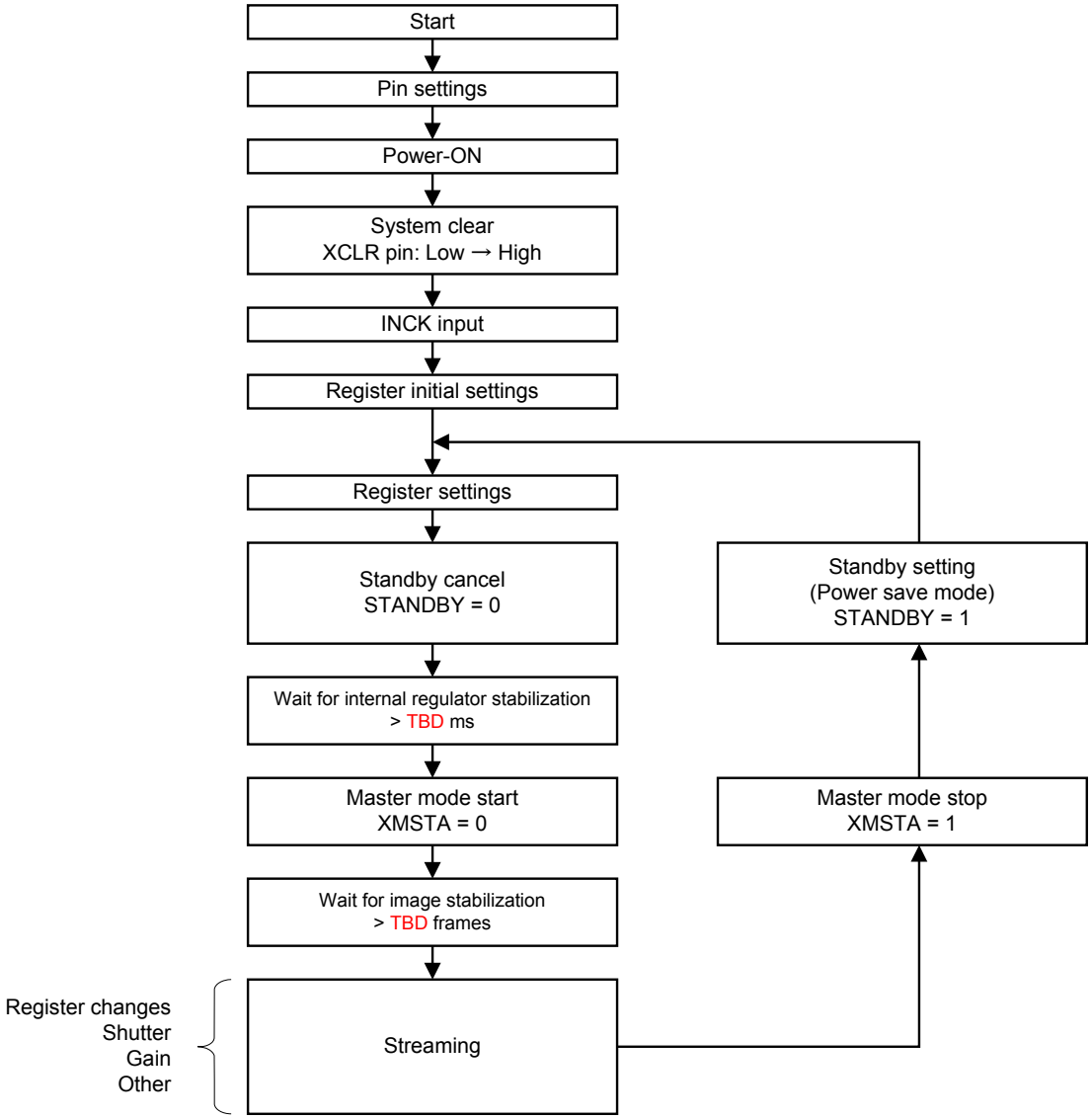
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". “Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Sensor Flow in Sensor Master Mode

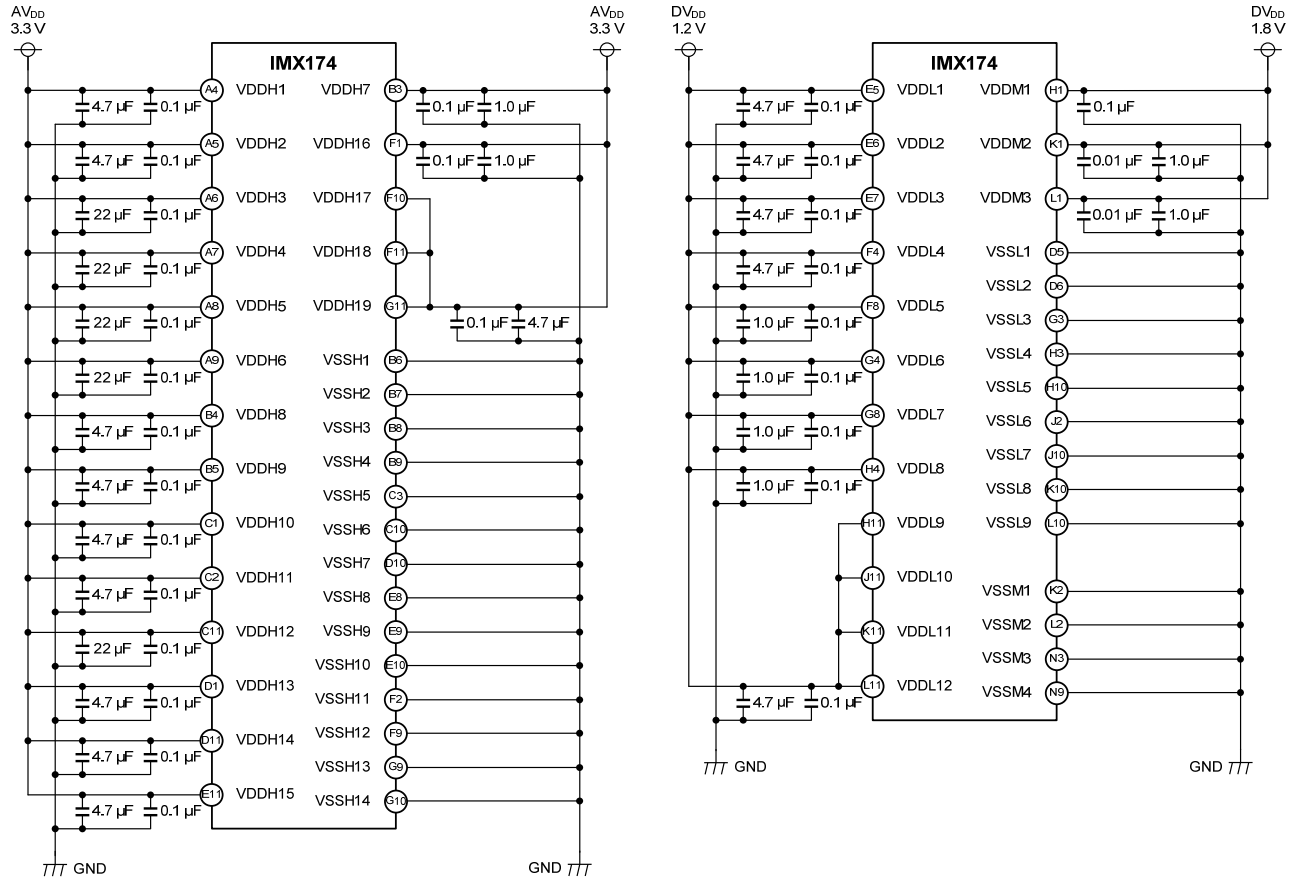
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

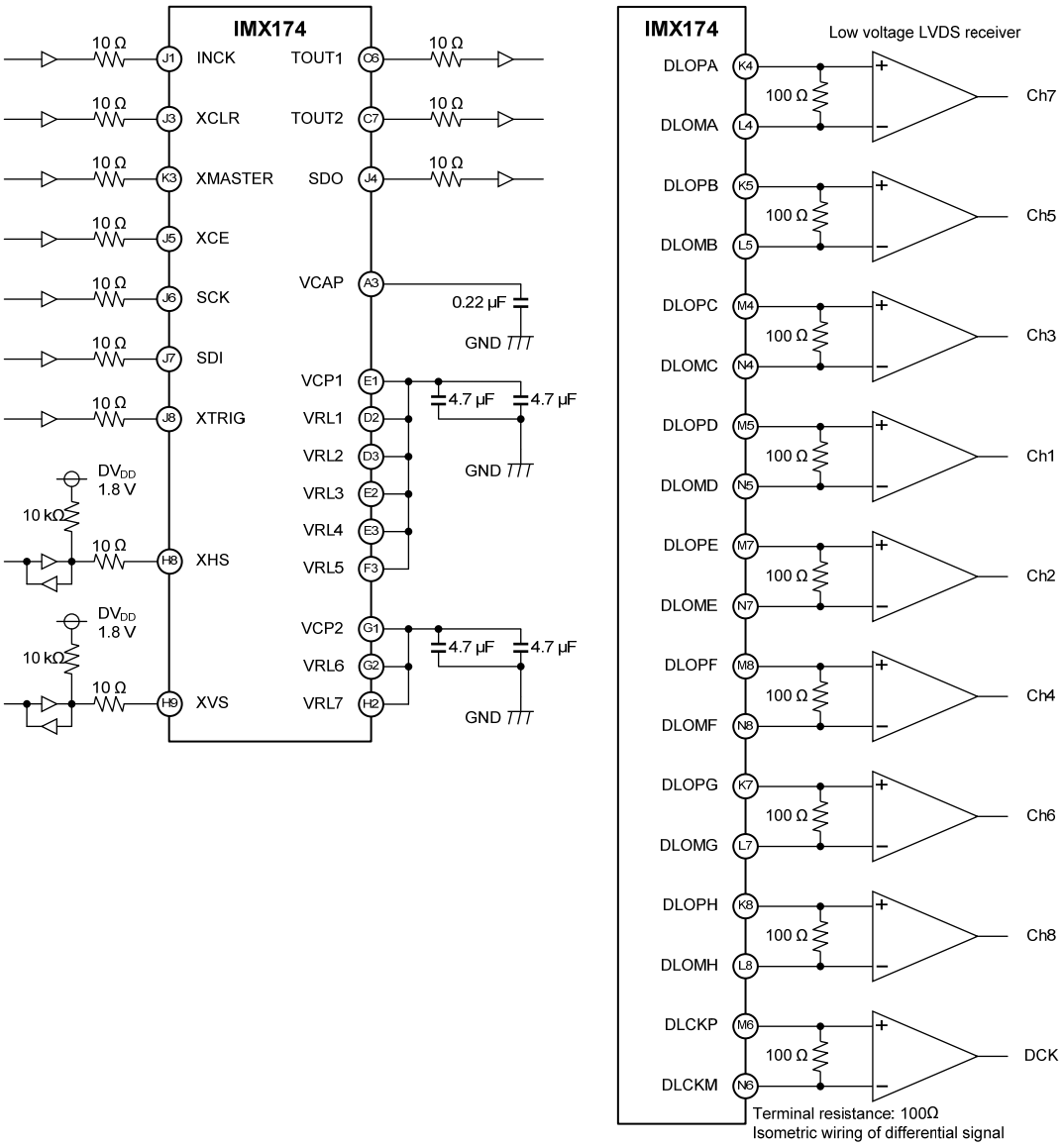
Peripheral Circuit

Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

I/O signal pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

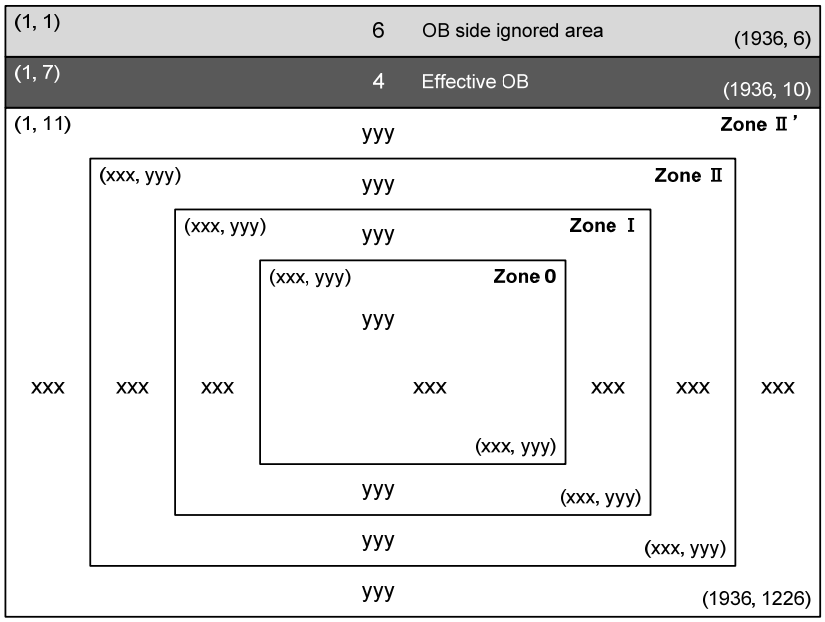
Spot Pixel Specifications

(Tj = 60 ˚C)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	TBD % ≤ D	TBD	No evaluation criteria applied		1	
White pixels in the dark	TBD mV ≤ D	TBD		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ TBD mV	0	No evaluation criteria applied		3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Sport Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	TBD pcs
10.0 mV or higher	TBD pcs
24.0 mV or higher	TBD pcs
50.0 mV or higher	TBD pcs
72.0 mV or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

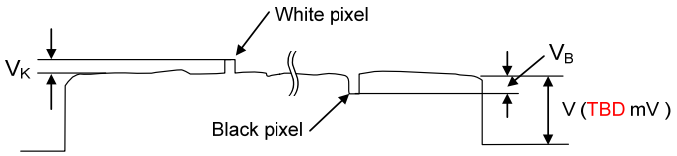
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value V of the Gr signal outputs is TBD mV, measure the local dip point (black pixel at high light, V_B) and peak point (white pixel at high light, V_K) in the signal output V, and substitute the value into the following formula.

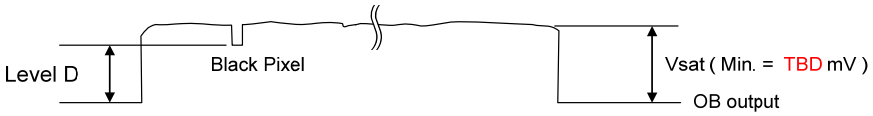
   Spot pixel level D = ((V_B or V_K) / Average value of V) × 100 [%]



Signal output waveform

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.



Signal output waveform

Spot Pixel Pattern Specification

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.
List of White Pixel, Black Pixel and Bright Pixel Pattern

TBD

Marking

TBD

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

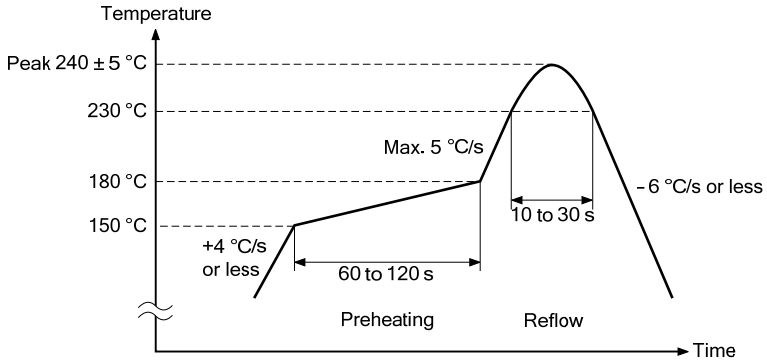
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (– 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

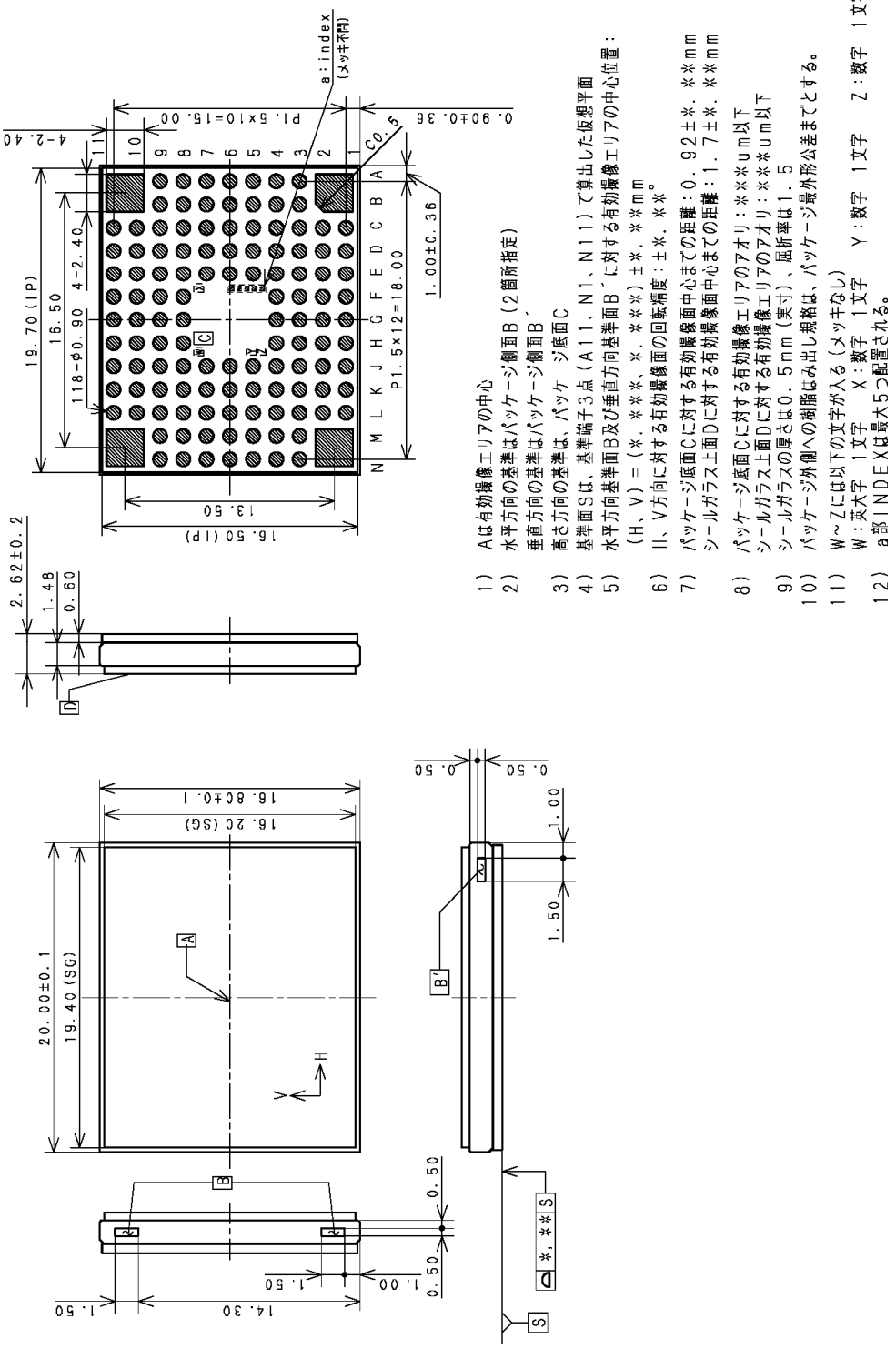
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline (TENTATIVE)

(Unit: mm)



1) Aは有効撮像エリアの中心
2) 水平方向の基準はパッケージ側面B（2箇所指定）
垂直方向の基準はパッケージ側面B´
3) 高さ方向の基準は、パッケージ底面C
4) 基準面Sは、基準端子3点（A11、N1、N11）で算出した仮想平面
5) 水平方向基準面B及び垂直方向基準面B´に対する有効撮像エリアの中心位置：
（H，V）=（*.***，*.***）±*.***mm
6) H、V方向に対する有効撮像面の回転精度：±*.**°
7) パッケージ底面Cに対する有効撮像面中心までの距離：0.92±*.***mm
シールガラス上面Dに対する有効撮像面中心までの距離：1.7±*.***mm
8) パッケージ底面Cに対する有効撮像エリアのアオリ：***μm以下
シールガラス上面Dに対する有効撮像エリアのアオリ：***μm以下
9) シールガラスの厚さは0.5mm（実寸）、屈折率は1.5
10) パッケージ外側への樹脂はみ出し規格は、パッケージ最外形公差までとする。
11) W～Zには以下の文字が入る（メッキなし）
W：英大字 1文字 X：数字 1文字 Y：数字 1文字 Z：数字 1文字
12) a部INDEXは最大5つ配置される。