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S5L33M Chip Datasheet

SUMMARY DESCRIPTION

The S5L33M is an integrated system-on-a-chip (SoC) platform that targets home IP cameras with up to 2Mp30 + 480p30 video performance.

S5L33M chips provide a quad-core 600 MHz Arm® Cortex®-A53 CPU for custom applications, a high-performance digital signal processing (DSP) sub-system with an image sensor pipeline (ISP), and high-performance H.265 / HEVC and H.264 / AVC encoders capable of simultaneous video recording and streaming.

KEY FEATURES

- Embedded Arm quad-core Cortex-A53 600 MHz CPU with L2 cache
- Smart video compression optimized for surveillance scenes, 2Mp30 as low as 512 Kbits/s
- Dual independent sensor inputs
- Up to 320 MPixel/s input pixel rate
- Lens distortion correction for wide-angle lenses
- Advanced dynamic range (WDR and HDR) engine
- 3D motion-compensated noise reduction (MCTF)
- H.264 / H.265 encode performance up to 2Mp30 plus secondary streams
- Simultaneous streaming of H.265 and H.264 encoded streams
- 256-pin, 0.65-mm pitch FC TFBGA package (11 mm x 11 mm)
- 14 nm CMOS low power (LP) technology
- Operating temperature from -20 C to +85 C

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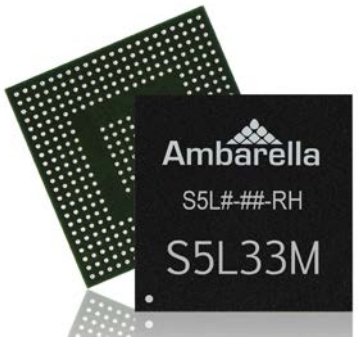


1. OVERVIEW

This preliminary datasheet for the S5L33M processor from Ambarella begins with a brief introduction to the chip (Section 1.1) and a summary of key features (Section 1.2). Chapter 2 describes the S5L33M peripheral interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

Please note that the chip features described in this datasheet are subject to change. Details that have not been entirely finalized (e.g., encoding specifics) are provided using conservative estimates (i.e., final encoding performance is expected to meet or exceed the estimate provided). Please contact an Ambarella representative for additional information.

1.1 Introduction

The S5L33M is an integrated SoC platform that targets low-power IP cameras with 2M - 5M video and HDR support, including service provider applications and cloud storage services for residential-level applications. S5L33M chip provides a quad-core Cortex-A53 Arm CPU for custom applications, a digital signal processing (DSP) subsystem with an image signal processor (ISP), and a high-performance H.265 / HEVC and H.264 / AVC encoding engine capable of simultaneous streaming. A functional block diagram of the S5L33M SoC is provided below.

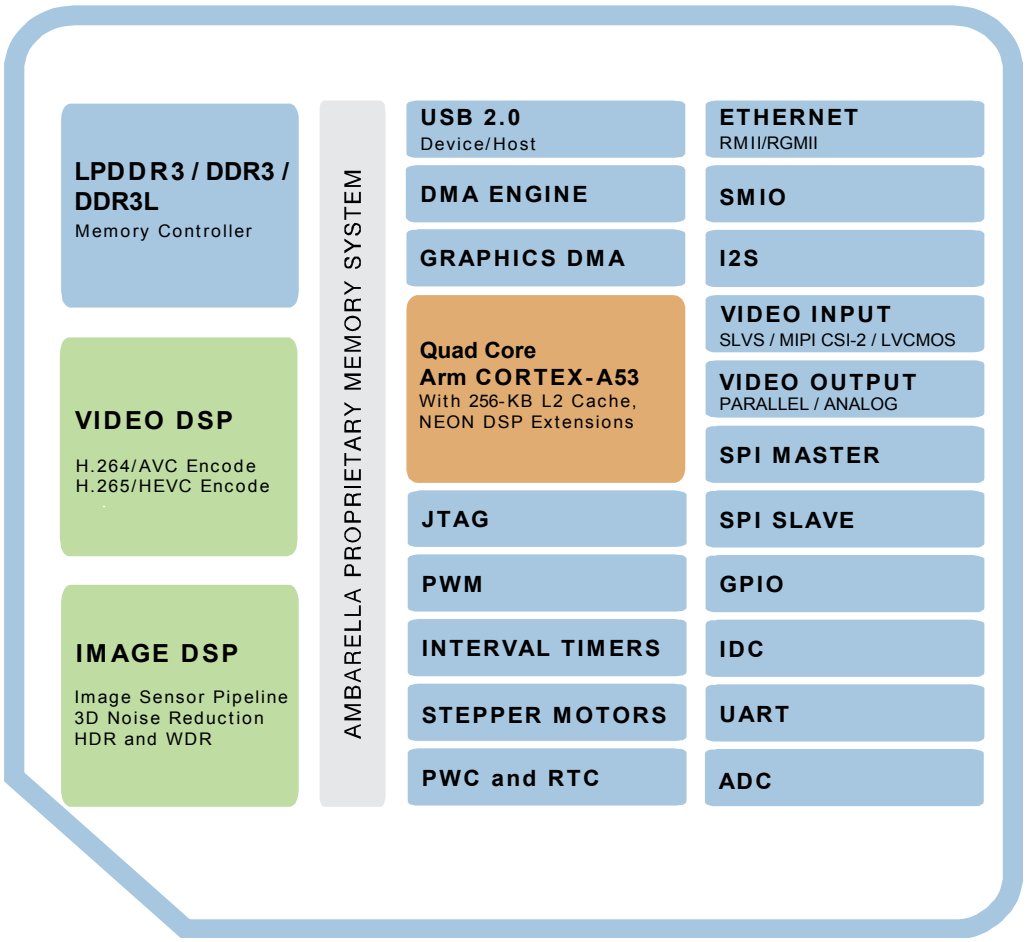


Figure 1-1. S5L33M Overview: Functional Block Diagram of the S5L33M SoC.

The S5L33M SoC provides a glueless interface to serial sub-LVDS, SLVS, HiSPi, and MIPI interfaces, as well as parallel connections to popular CMOS image sensors. The ISP offers advanced image-processing features including improved multi-exposure high dynamic range (HDR) processing, wide dynamic range (WDR) single-exposure tone mapping with local contrast enhancement, 3D motion-compensated noise reduction (MCTF), edge enhancement, and fisheye lens distortion correction with rectilinear and panorama modes for up to 180 degrees .

The H.264/H.265 codec engine delivers versatile encoding up to 2Mp30 + 480p30 + 2Mp1 / 2Mp30 + 480p30 + 2Mp1 total performance, including simultaneous encode streams. The high-efficiency encoder implements full-function H.265/HEVC and H.264/AVC video encoding for the highest-quality and lowest possible bitrate. These functions include bidirectional prediction (B-frames), large motion-estimation search range, and macroblock-level quantization. Ambarella builds in flexibility with a multi-streaming function, allowing on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream.

A 600 MHz quad-core Arm Cortex-A53 CPU with NEON DSP extensions and floating point support is available for implementing full-featured user applications.

The S5LM family is fabricated using low-power 14-nm CMOS technology and integrates advanced power-saving modes, such as utilizing DSP-subsystem memory resources to reduce external memory bandwidth and total camera system power requirements.

1.2 Feature List

Features of the S5L33M chip include:

- Embedded quad-core Arm Cortex-A53 CPU
  - Clock frequency up to 600 MHz
  - 32 KB data / 32 KB instruction cache
  - 256 KB L2 cache
  - NEON SIMD acceleration
- DDR3 and LPDDR3 controller
  - Up to 456 MHz clock rate
  - 16-bit wide data bus
  - Maximum capacity of 4 Gbits (512 Mbytes)
- Sensor / video input (VIN) interfaces
  - Support for popular CMOS sensors: Sony, ON Semiconductor (Aptina), Panasonic, OmniVision
  - Two VIN instances; one VIN (main) and one PIP / VIN (secondary)
    - Single 8-lane sub-LVDS / SLVS / HiSPi™ or up to 4-lane MIPI input
    - Secondary channel supports up to 4-lane SLVS / HiSPi / MIPI input
    - 14-bit parallel and LVCMOS sensors
  - 16-bit CCIR.601 video input with external sync signals
  - 8- / 10- / 12- / 14-bit BT.656 style Bayer RGB input with embedded sync codes
  - 8-bit BT.656 style YUV422 input with embedded sync codes
- Image / video processing
  - Up to 320 MPixel/s input pixel rate

- Fish-eye lens distortion correction
- 3D electronic image stabilization (EIS) with rolling shutter correction
- Black level correction
- Static and dynamic bad pixel correction
- RGB Bayer demosaicing
- Lens shading correction
- Vignetting compensation
- Chromatic aberration correction
- 3D LUT color transform with gamma
- Advanced motion-compensated sharpening
- Advanced dynamic range (WDR and HDR) engine with multi-exposure fusion and motion artifact reduction
- Motion compensated temporal filtering (MCTF) for excellant low-light performance
- Adjustable 3A; exposure, white balance and focus control (AE / AWB / AF)
- RGB and YUV statistics, histogram and AF focus value generation
- Luma sharpen and chroma noise filter
- Crop, mirror, flip, 90°/270° rotation
- Alpha-blending OSD up to full-frame overlay for text, image, and privacy mask
- Flexible APIs and image-tuning tools
- Four resizers (1/8X ~ 16X scaling) with digital pan, tilt and zoom (PTZ)
- HISO still pipeline support

- Video encoding
  - H.265 / HEVC Main Profile Level 5.0 encoding
  - H.264 / AVC MP/HP Level 5.1 encoding
  - JPEG encoding
  - Encode performance up to 2Mp30 + 480p30 + 2Mp1 (H.264) or up to 2Mp30 + 480p30 + 2Mp1 (H.265). System performance may be influenced by image processing features enabled (e.g., oversampling, rotation, HDR, type of noise reduction).
    - Up to six real-time simultaneous encodes with on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream.
  - Advanced compression tools
    - I, IP, IBP modes (M=1,2,3,4…; IP, IBP, IBBP, IBBBP…)
  - Flexible rate control
    - CBR, VBR and Constant QP with max bitrate control
    - Macroblock-level adaptive quantization
- Video output (VOUT) interfaces
  - Two logical channels to drive two video output ports
    - One analog

        - One digital video output
    - RGBA and YUVA OSD
    - Video DAC for 480i / 576i composite PAL / NTSC output
- AHB bus DMA controller
    - Memory-to-memory transfers including support for transfers between memory and peripherals
    - Programmable transfer count up to 4 MB
    - DMA scatter / gather via chained descriptor list in memory with DMA control information source
- Dedicated DMA co-processor for graphics and image operations
    - Linear copy, 2-D copy, composite, and alpha-blend image operations
    - 4- to 32-bit pixel formats
- I2S digital audio interface (stereo)
    - Audio record / playback
- Ethernet MAC controller
    - IEEE 802.3 compliant with full- and half-duplex (IEEE 802.3x flow-control) and jumbo frames
    - IEEE 802.1Q VLAN tag detection
    - Checksum off-load for received IP and TCP / UDP packets
    - Dedicated pins for RMII or RGMII interface
    - FIFO (4 KB / 4 KB) and DMA support
- USB 2.0 interface
    - One port configurable as host or device, with built-in PHY
- Flexible storage media input / output (SMIO) interface
    - NAND flash controller
        - Up to 8 Gb device, and 2 KB page sizes
        - 8-bit flash chip data bus
        - 4-bit and 8-bit SLC with ECC hardware and read-confirm support
        - BCH error correction and increased spare area available
    - Two SD controllers (SD0, SD1)
        - SD0 & SD1:
            - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
            - 1-bit, 4-bit SD mode
        - 32 GB maximum capacity for SDHC SD Card
        - 2 TB maximum capacity for SDXC SD Card
        - CRC7 for command and CRC16 for data integrity
- Multiple boot options
    - NOR-SPI, NAND Flash, USB and eMMC
- Generic interrupt controller including GIC CPU-offload functionality
- SSI / SPI controller interfaces
    - Two SSI / SPI masters with DMA support for up to twelve device enables

  - One dedicated SSI / SPI slave port to connect to an external system master
- Two-wire serial inter-integrated circuit (I2C / IDC) interfaces (x2)
  - Configurable IDC buses
- UART interfaces (x2)
  - DMA support
  - One interface supports flow control
- Up to 94 general purpose input / output (GPIO) pins with individual pull-up / down control
- ADC (two channels) with high / low threshold interrupt generation and 12-bit resolution
- Built-in power controller for power-up / down sequencing
- Real time clock (RTC)
- Interval timing with eight general-purpose timers configurable as external event counters
- Watchdog timer
- Stepper motor interface (five channels)
- Pulse width modulators (PWM) (x3)
- JTAG in-circuit emulator (ICE) interface for debugging
- 256-pin, 0.65-mm pitch FC TFBGA package (11 mm x 11 mm)
- 14-nm CMOS low power (LP) technology
- Operating temperature from -20 C to +85 C

2. INTERFACES

2.1 Overview

This section summarizes the peripheral interfaces for the S5L33M chip as follows:

- (Section 2.2) SDRAM Interface
- (Section 2.3) Video Input (VIN) Interface
- (Section 2.4) Video Output (VOUT) Interfaces
- (Section 2.5) I2S Audio Interface
- (Section 2.6) Digital Microphone Interface (DMIC)
- (Section 2.7) Gigabit Ethernet MAC
- (Section 2.8) USB Interface
- (Section 2.9) Smart Media Input / Output (SMIO) Interface
- (Section 2.10) SSI / SPI Interface
- (Section 2.11) I2C / IDC Interface
- (Section 2.12) UART Interface
- (Section 2.13) General Purpose Input/Output (GPIO) Interface
- (Section 2.14) Analog-to-Digital Converter (ADC) Interface
- (Section 2.15) Real Time Clock (RTC) Interface
- (Section 2.16) Stepper and Pulse Width Modulator (PWM) Interfaces
- (Section 2.17) JTAG Interface

2.2 SDRAM Interface

The S5L33M chip includes a synchronous DRAM interface, enabling high data-access rates in response to pipelined commands. The features of the S5L33M SDRAM interface include:

- Frequencies up to 456 MHz
- Support for the LPDDR3 / DDR3 / DDR3L low-power DDR interface
- Programmable I/O strength
- 16-bit data bus

Please contact an Ambarella representative to select a qualified Ambarella-approved DDR component.

2.3 Video Input (VIN) Interface

The S5L33M chip supports multiple serial and parallel input modes. The features of the S5L33M VIN interface include:

- Two sensor VIN instances - One VIN (Main) and one secondary:
- VIN (Primary, with all secondary units disabled):
    - 1-8 Lane SLVS (up to 3 Gbps per lane)

- 1-4 Lane MIPI CSI-2 (up to 3 Gbps per lane)
- 16-bit Parallel LVCMOS (up to 150 MHz) (YUV422)

◦ Secondary:

- 1-4 Lane SLVS (up to 3 Gbps per lane)
- 1-4 Lane MIPI CSI-2 (up to 3 Gbps per lane)

◦ Example use cases with 2 sensor inputs:

- All 8 lanes are used by VIN
- VIN and Secondary, each uses 4 lanes

Lane	VIN Only	VIN + Secondary
1	1 (VIN)	1 (VIN)
2	2 (VIN)	2 (VIN)
3	3 (VIN)	3 (VIN)
4	4 (VIN)	4 (VIN)
5	5 (VIN)	1 (Secondary)
6	6 (VIN)	2 (Secondary)
7	7 (VIN)	3 (Secondary)
8	8 (VIN)	4 (Secondary)

Table 2-1. Lane Sharing Between VIN and Secondary Inputs.

The S5L33M VIN module is part of the DSP cluster. Like other modules in the DSP cluster it is configured using a set of APIs. Please contact an Ambarella representative for information regarding VIN module configuration and other possible combinations for lane sharing.

2.4 Video Output (VOUT) Interfaces

The S5L33M video output (VOUT) interface supports a total of three output ports using two logical video channels.

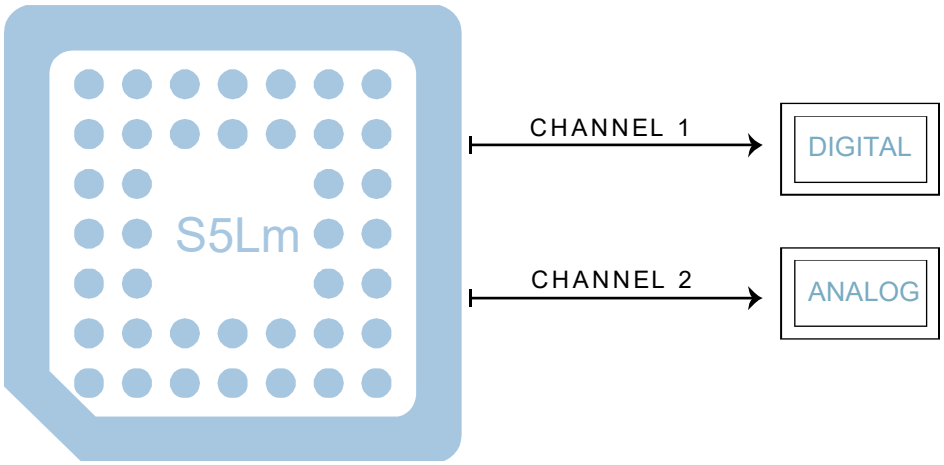


Figure 2-1. S5L33M Video Output Channels and Ports.

2.4.1 Analog Video Output

The S5L33M video digital-to-analog converter (DAC) can drive standard-definition 480i / 576i composite video outputs.

2.4.2 Digital Video Output

The S5L33M chip supports several digital video output modes including 8-bit or 16-bit {CbY, CrY}, LCD-RGB, and CCIR.601 as described in the tables below.

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved R,G,B	**VD0_OUT[7]** is MSB

Table 2-2. Digital RGB Mode (Video Output Modes 0/1/2 for 3-bit Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:11]	Upper 5 bits of the Red channel	**VD0_OUT[15]** is the MSB
VD0_OUT[10:5]	Upper 6 bits of the Green channel	**VD0_OUT[10]** is the MSB
VD0_OUT[4:0]	Upper 5 bits of the Blue channel	**VD0_OUT[4]** is the MSB

Table 2-3. 5:6:5 RGB Mode (Video Output Mode 3 for 16-bit RGB Output to the LCD).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved Cb,Y,Cr,Y . . .	

Table 2-4. 8-bit YCbCr Mode (Video Output Mode 7).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Interleaved Cb,Cr	**VD0_OUT[15]** is the MSB
VD0_OUT[7:0]	Y	**VD0_OUT[7]** is the MSB

Table 2-5. 16-bit 601-YCbCr Mode (Video Output Mode 5).

Table 2-4 and Table 2-5 correspond to 4:2:2 output format.

2.5 I2S Audio Interface

The S5L33M chip provides an integrated interchip sound (I2S) controller for two-channel audio support. Features of the I2S interface include:

- Support for audio using an external audio codec analog-to-digital converter (ADC)
- I2S host interface support
- All data lanes are clocked by the same clock signal

2.6 Digital Microphone Interface (DMIC)

The S5L33M chip provides a digital microphone interface (DMIC).

2.7 Gigabit Ethernet MAC

The S5L33M ethernet controller supports

- 10 / 100 / 1000-Mbps data transfer rates with IEEE 802.3-compliant RGMII / RMII interface and communicates with an external Gigabit / Fast Ethernet PHY
- MDIO master interface (optional) for PHY device configuration and management

2.7.1 Enable / Disable Ethernet

Ethernet functionality is enabled / disabled with power-on configuration bit POC[6], whether the Gigabit function (RGMII) is enabled or Ethernet RMII is used.

2.8 USB Interface

The S5L33M SoC includes one USB 2.0 port configurable as host or device, with a built-in PHY. Features of the S5L33M USB interface include:

- One configurable USB host / device, with a built-in PHY
- USB power-on boot mode
- The USB device can be used to burn firmware to flash or to simulate ethernet for debugging.
- The USB host can be used to connect a USB WiFi module, a USB card reader, or 3G/4G baseband.

2.9 Smart Media Input / Output (SMIO) Interface

The S5L33M chip provides smart media input / output (SMIO) pins as a flexible storage-media interface for NAND flash and SD controllers. Features of the S5L33M SMIO interface include:

- NAND flash controller
  - Up to 8 Gb device and 2 KB page sizes
  - 8-bit flash chip data bus
  - 4-bit and 8-bit single-level cell (SLC) memory with error-correcting code (ECC) hardware and read-confirm support
- Two SD controllers (SD0, SD1)
  - SD0 & SD1:
    - SDIO v3.0, SD, SDHC, SDXC, MMC and eMMC operation with boot support and UHS-I speed
    - Support for 1-bit, 4-bit SD mode
  - 32 GB maximum capacity for SDHC SD Card
  - 2 TB maximum capacity for SDXC SD Card
  - Cyclic redundancy check 7 (CRC-7) for command, and cyclic redundancy check 16 (CRC-16) for data integrity
- Power-on NAND flash and eMMC boot modes
- SD0 may be used to connect to an SD card or an SDIO Wi-Fi module.

2.10 SSI / SPI Interface

The S5L33M chip provides two synchronous serial interface (SSI) / serial peripheral interface (SPI) masters and one dedicated SSI / SPI slave for full-duplex data transmission support. Features of the S5L33M SSI / SPI interface include:

- SSI / SPI master control with DMA support for up to twelve slave devices
- Dedicated SSI / SPI slave port for connection to an external system master
- SPI-NOR, SPI-EEPROM boot support included with DMA support

Master	Number of Device Enables	Device Enable Pins	SSI/SPI Function	Default Polarity[1]
SSI0	4	**SSI0EN0**	ssi0_en0 Device Enable	Active Low
		SSI0EN1	ssi0_en1 Device Enable	Active Low
		SC_E0	ssi0_en2 Device Enable	Active Low
		TIMER2	ssi0_en3 Device Enable	Active Low
SSI1	4	**ENET_RXD_0** or **SC_A3**	ssi1_en0 Device Enable	Active Low
		ENET_RXD_1 or **SC_B0**	ssi1_en1 Device Enable	Active Low
		ENET_RX_ER or **SC_B1**	ssi1_en2 Device Enable	Active Low
		ENET_CRS_DV or **SC_B2**	ssi1_en3 Device Enable	Active Low
-	-	-	-	-
		-	-	-
		-	-	-
		-	-	-

Table 2-6. S5L33M SSI / SPI Master with Device Enable Detail.

Note:

Each SSI / SPI device-enable has programmable polarity; i.e., the polarity can be assigned to meet peripheral requirements without external glue logic.

2.11 I2C / IDC Interface

The S5L33M SoC includes two inter-integrated circuit (I2C / IDC) interfaces to provide bidirectional data communication between the chip and its peripheral devices. Features of the S5L33M I2C / IDC interfaces include:

- Protocol speeds up to 400 Kbps
- Support for single-master mode

2.12 UART Interface

The S5L33M chip includes two universal asynchronous receiver / transmitter (UART) ports. Features of the S5L33M UART interface include:

- Support for direct memory access (DMA) and hardware flow control in UART Port 1
- Debugging support in UART Port 0
- A maximum baud rate of 115.2 Kbps for UART0, based on per-port software settings
- Port 2 (UART2_AHB) is pin muxed with other functions
- UART_AHB can be used to connect to Bluetooth / GPS when other mux functions are not in use

- Benefits of using UART_AHB:
  - Supports hardware flow control
  - Supports DMA

2.13 General Purpose Input/Output (GPIO) Interface

The S5L33M SoC includes 93 CMOS pins which can be programmed for multi-use general purpose input / output (GPIO) functions. Features of the S5L33M GPIO interface include:

- Pins with reduced electrostatic discharge sensitivity, tested to the latest JEDEC standard (*Joint Standard for Component-Level Electrostatic Discharge Sensitivity Testing*)
- Multiplexing support, allowing GPIO pins to be assigned multiple functions that can be independently enabled via software
- Individual pull-up / down control
- Individual drive strength control

2.14 Analog-to-Digital Converter (ADC) Interface

The S5L33M chip provides multiple channels for analog-to-digital conversion (ADC). Features of the S5L33M ADC interface include:

- Two channels
- High / low threshold interrupt generation
- 12-bit resolution

2.15 Real Time Clock (RTC) Interface

To conserve power, the S5L33M system software optimizes clock and PLL frequencies according to operating mode. Peripheral clocks can be further optimized by the user through register programming.

Features of the real-time clock (RTC) interface include:

- 32-bit embedded RTC maintained with one dedicated always-on power supply pin
- RTC provides current time, alarm set, and power-on and power-off sequence generation

2.16 Stepper and Pulse Width Modulator (PWM) Interfaces

2.16.1 Stepper Controllers

The S5L33M chip supports five stepper motor controller channels, each of which can be used for independent motor control.

2.16.2 Pulse Width Modulator (PWM)

The S5L33M chip provides three pulse width modulation interfaces (PWMB0/B1/C0):

- The three PWM outputs are referred to as pwm_[0:2]. Functionally:
  - PWMB0 is associated with pwm_0
  - PWMB1 is associated with pwm_1
  - PWMC0 is associated with pwm_2
- Note that in addition to the PWM controller embedded in the stepper motor controller, the S5L33M external pin **VD_PWM** can also serve as a PWM controller.
- Selection of PWM functions is executed via software.

2.17 JTAG Interface

The S5L33M chip provides an interface for JTAG in-circuit emulator (ICE) debugging. Contact an Ambarella representative for more information regarding the JTAG interface.

3. PINS

3.1 Pins: Overview

The S5L33M SoC is equipped with 256 external physical pins including power balls, ground balls, and signal balls. This section provides pin details for the primary chip interfaces and functions.

- Refer to Section 4.4 for a list of fail-safe CMOS pins and their corresponding voltage thresholds.
- Refer to Chapter 7 for a complete list of pins sorted by their location on the S5L33M ball map.

3.2 Pins: Tables

This section lists the pins for each interface as follows:

For each pin listed, the following information is provided:

- Pin direction: (I) input, (O) output, (S) supply, (G) ground
- Pad type
- A brief description
- For complete multiplexing information, please refer to Section 3.2.12 and Chapter 7.

3.2.1 Pins: DRAM

Name	Location	Dir	Type	Description
DDR_CALIBR	A4	I/O	Analog	ZQ calibration
DDR_CAS	G1	O	SSTL	Column address strobe (active low)
DDR_BA_[2:0]	F3, D1, E3	O	SSTL	Bank address
DDR_ADDR_[14:0]	C2, B4, E2, C1, E1, A3, A1, B3, B2, C3, B1, D3, A2, D2, D4	O	SSTL	Address for row address strobe (RAS) and column address strobe (CAS)
DDR_CK, DDR_CK_BAR	H2, G2	O	SSTL	DRAM clock per SDRAM. **DDR_CK** and **DDR_CK_BAR** are differential clocks
DDR_CKE	F2	O	SSTL	Clock enable
DDR_RAS	F1	O	SSTL	Row address strobe (active low)
DDR_VREF_1	H1	I/O	SSTL	Reference Voltage for SSTL18 pad
DDR_WE	G3	O	SSTL	Write enable (active low)
DDR_ODT	H3	O	SSTL	SDRAM on-die termination control signal
DDR_DM_[1:0]	L2, P2	O	SSTL	Data write mask (1 bit per 8 data bits)
DDR_DQ_[15:0]	K3, J2, J3, L3, M1, J1, M3, K2, N2, T2, M2, T1, N1, R2, P1, R1	I/O	SSTL	Bi-directional data bus
DDR_DQS_[1:0]	K1, N3	I/O	SSTL	Data strobe (1 bit per 8 data bits) Output with write data, center-aligned Input with read data, edge-aligned
DDR_DQS_BAR_[1:0]	L1, P3	I/O	SSTL	**DDR_DQS_[N]** and **DDR_DQS_BAR_[N]** are differential signals
DDR_RESET	C4	O	SSTL	DDR3 - Asynchronous reset
DDR_VDDQ_CKE	D5	S	Digital Supply	Power for DDR_CKE and DDR_RESET pins
DDR_VDDQ	E4, F4, G4, H4, J4, K4, L4, M4	S	Digital Supply	DDR digital I/O power supply

Table 3-1. DRAM Pins.

3.2.2 Pins: Sensor / Video Input

Name	Location	Dir	Type	Description
CLK_SI	D9	I/O	CMOS	Sensor master clock output
SD_LVDS_N_[0:7]	B11, B12, B13, B14, B6, B7, B8, B9	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor data Differential for sub-LVDS / SLVS / MIPI Single-ended for LVCMOS mode Termination resistor built in for sub-LVDS / SLVS mode Both single and double data rates supported.
SD_LVDS_P_[0:7]	A11, A12, A13, A14, A6, A7, A8, A9	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SHSYNC	D8	O	CMOS	H-Sync / H-Valid with Master mode configuration

Name	Location	Dir	Type	Description
SPCLK_LVDS_N_[0:1]	B10, B5	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	Sensor pixel clock Differential pairs for sub-LVDS / SLVS / MIPI mode. **SPCLK_LVDS_P_0** is used for single-ended pixel clock with LVCMOS mode
SPCLK_LVDS_P_[0:1]	A10, A5	I	Sub-LVDS/ SLVS/ LVCMOS /MIPI	
SVSYNC	D7	I/O	CMOS	V-Sync / V-Valid with Master mode configuration

Table 3-2. VIN Sensor Interface Pins.

Note:

Refer to the Video Input chapter of the *System Hardware* document for the MIPI CSI-2 pin map.

3.2.3 Pins: Video Output

This section covers video output interface pins for Digital-to-Analog Conversion, and Digital Video Output.

3.2.3.1 VOUT Pins: Video Digital-to-Analog Conversion (DAC)

Name	Location	Dir	Type	Description
DAC_COMP	E8	I/O	Analog	Compensation pin
DAC_IO	E6	I/O	Analog	Composite CVBS output
DAC_RSET	D6	I/O	Analog	Reference resistor
DAC_VREFIN	E7	I/O	Analog	Voltage reference input

Table 3-3. Video DAC Pins.

3.2.3.2 VOUT Pins: Digital Video Output

Name	Location	Dir	Type	Description [1]
VD0_CLK	M8	I/O	CMOS	Video output clock
VD0_HSYNC	T7	I/O	CMOS	Video output HSync signal
VD0_HVLD	R8	I/O	CMOS	Video output data
VD0_OUT_0	T5	I/O	CMOS	Video output data
VD0_OUT_1	R5	I/O	CMOS	Video output data
VD0_OUT_2	N5	I/O	CMOS	Video output data
VD0_OUT_3	N4	I/O	CMOS	Video output data
VD0_OUT_4	P4	I/O	CMOS	Video output data
VD0_OUT_5	R4	I/O	CMOS	Video output data
VD0_OUT_6	T4	I/O	CMOS	Video output data
VD0_OUT_7	T3	I/O	CMOS	Video output data
VD0_OUT_8	N8	I/O	CMOS	Video output data
VD0_OUT_9	R7	I/O	CMOS	Video output data
VD0_OUT_10	P7	I/O	CMOS	Video output data
VD0_OUT_11	N7	I/O	CMOS	Video output data
VD0_OUT_12	N6	I/O	CMOS	Video output data
VD0_OUT_13	P6	I/O	CMOS	Video output data
VD0_OUT_14	R6	I/O	CMOS	Video output data
VD0_OUT_15	T6	I/O	CMOS	Video output data
VD0_VSYNC	T8	I/O	CMOS	Video output VSync signal

Table 3-4. Digital Video Output Pins.

Note:

- S5L33M digital video output pins are used for power-on configuration (POC).

3.2.4 Pins: I2S Digital Audio

Name	Location	Dir	Type	Description
CLK_AU	M11	O	CMOS	Master clock for external audio codec
I2S_CLK	T16	I/O	CMOS	I2S Controller audio bit clock
I2S_SI	T14	I	CMOS	I2S Controller serial data in
I2S_SO	T13	O	CMOS	I2S Controller serial data out
I2S_WS	T15	I/O	CMOS	I2S Controller word select

Table 3-5. I2S Controller Pins.

3.2.5 Pins: Ethernet Interface

Name	Location	Dir	Type	Description
ENET_MDC	N9	I/O	CMOS	MII clock
ENET_CLK_RX	R12	I/O	CMOS	Reference clock
ENET_RXD_[3:0]	P11, R11, T11, T12	I/O	CMOS	Receive data

Name	Location	Dir	Type	Description
ENET_MDIO	M9	I/O	CMOS	MII data bus
ENET_CLK_TX	N11	I/O	CMOS	Transmit clock
ENET_GTX_CLK	R9	I/O	CMOS	Ethernet clock
ENET_RXDV	N12	I/O	CMOS	Receive data
ENET_TXD_[3:0]	N10, P10, R10, T10	I/O	CMOS	Transmit data
ENET_TXEN	T9	I/O	CMOS	Transmit ready
ENET_EXT_OSC_CLK	P12	I/O	CMOS	Ethernet external oscillator clock

Table 3-6. Ethernet Pins.

3.2.6 Pins: USB

Name	Location	Dir	Type	Description
GPIO_1	M13	I/O	CMOS	USB EHCI overcurrent detect input
GPIO_3	N16	I/O	CMOS	USB EHCI port power enable out
DETECT_VBUS	C13	I/O	CMOS	USB slave bus detect
USB_DM	B16	I/O	Analog	USB data. DP/DM are differential signals.
USB_DP	A16	I/O	Analog	
USB_REXT	A15	I/O	Analog	USB resistor

Table 3-7. USB Interface Pins.

3.2.7 Pins: Smart Media Input/Output (SMIO)

- The Smart Media Input/Output (SMIO) pins are CMOS type and programmable input/output.
- SMIO pins are shared by controllers for NAND Flash (NAND) and SD / SDIO / SDHC / SDXC / MMC / eMMC (SD).
- SMIO pins use **SMIO_[N]** for the primary function name.

Name	Location	NAND		SD		Description
		Function	Dir	Function	Dir	
SMIO_0	K13	nand_ce	O			NAND chip enable
SMIO_1	H11	nand_rb	I/O			NAND ready / busy
SMIO_2	F16			sd_clk	O	SD0 clock
SMIO_3	F15			sd_cmd	I/O	SD0 command
SMIO_4	F14			sd_cd	I	SD0 card detect
SMIO_6	K15	nand_re	O			NAND read enable
SMIO_7	K16	nand_we	O			NAND write enable
SMIO_8	J12	nand_ale	O			NAND address latch enable
SMIO_9	J13	nand_d[0]	I/O			NAND data
SMIO_10	J14	nand_d[1]	I/O			NAND data
SMIO_11	J15	nand_d[2]	I/O			NAND data

Name	Location	NAND		SD		Description
		Function	Dir	Function	Dir	
SMIO_12	J16	nand_d[3]	I/O			NAND data
SMIO_13	H12	nand_d[4]	I/O			NAND data
SMIO_14	G12	nand_d[5]	I/O			NAND data
SMIO_15	H14	nand_d[6]	I/O			NAND data
SMIO_16	H15	nand_d[7]	I/O			NAND data
SMIO_17	H16	nand_cle	O			NAND command latch enable
SMIO_18	F13			sd_d[0]	I/O	SD0 data
SMIO_19	G16			sd_d[1]	I/O	SD0 data
SMIO_20	G15			sd_d[2]	I/O	SD0 data
SMIO_21	E12			sd_d[3]	I/O	SD0 data
SMIO_26	E13			sdxc_clk	O	SD1 clock
SMIO_27	E14			sdxc_cmd	I/O	SD1 command
SMIO_28	E15			sdxc_d[0]	I/O	SD1 data
SMIO_29	E16			sdxc_d[1]	I/O	SD1 data
SMIO_30	D15			sdxc_d[2]	I/O	SD1 data
SMIO_31	D16			sdxc_d[3]	I/O	SD1 data
SMIO_38	G13			sd_reser	O	SD0 reser
WP	K12	nand_wp	O			NAND write protect

Table 3-8. Storage Media Interface Pins (SMIO) in NAND Flash and SD Modes.

3.2.8 Pins: SSI / SPI

Name	Location	Dir	Pad Type	Description
SSI0CLK	L16	I/O	CMOS	ssi0 master port bit clock
SSI0EN0	L13	O	CMOS	ssi0_en0 device enable
SSI0EN1	L12	O	CMOS	ssi0_en1 device enable
TIMER2	D13	I/O	CMOS	ssi0_en3 device enable
ENET_RXD_0	T12	I/O	CMOS	ssi1_en0 device enable
ENET_RXD_1	T11	I/O	CMOS	ssi1_en1 device enable
SSI0MISO	L15	I	CMOS	ssi0 master port data in
SSI0MOSI	L14	O	CMOS	ssi0 master port data out

Table 3-9. SSI / SPI Interface Pins.

3.2.9 Pins: I2C / IDC

Name	Location	Dir	Pad Type	Description
IDCCLK	N13	I/O	CMOS	First IDC serial port - clock
IDCDATA	P13	I/O	CMOS	First IDC serial port - data
IDC3CLK	P14	I/O	CMOS	Third IDC serial port - clock
IDC3DATA	P15	I/O	CMOS	Third IDC serial port - data

Table 3-10. I2C / IDC Interface Pins.

3.2.10 Pins: UART

Name	Location	Dir	Pad Type	Description
UART0RX	M16	I	CMOS	UART Port 0 receive
UART0TX	M15	O	CMOS	UART Port 0 transmit

Table 3-11. UART Interface Pins.

3.2.11 Pins: InfraRed Remote

Name	Location	Dir	Pad Type	Description
IR_IN	D10	I	CMOS	InfraRed input

Table 3-12. InfraRed Remote Interface Pins.

3.2.12 Pins: General Purpose Input/Output (GPIO)

The table below lists the General-Purpose Input/Output (GPIO) pins on the S5L33M chip. GPIO pins have multi-function capabilities and are CMOS-type programmable input/output. The function name that appears on the chip ball map is indicated in the **Pin Name** column. Refer to Chapter 7 for map locations.

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
0	**GPIO_0**	sd_hs_sel				
1	**GPIO_1**	ehci_app_prt_ovcurr0	uart2_ahb_rx	ssis_sclk	sc_c0	
2	**GPIO_2**	ehci_app_prt_ovcurr1	uart2_ahb_tx	ssis_rxd	sc_c1	
3	**GPIO_3**	ehci_prt_pwr_0	uart2_ahb_cts_n	ssis_txd	sc_c2	
5	**GPIO_5**	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart2_ahb_cts_n
6	**GPIO_6**	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart2_ahb_rts_n
25	**TIMER0**	tm11_clk	ssi2_en2			
26	**TIMER1**	tm12_clk	ssi2_en3	idsp_pip_iopad_master_hsync		
27	**TIMER2**	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync		
28	**IDCCLK**	idc0clk				
29	**IDCDATA**	idc0data				
32	**IDC3CLK**	idc2clk	vin_strig0			
33	**IDC3DATA**	idc2data	vin_strig1			
34	**IR_IN**	ir_in				
35	**SSI0CLK**	ssi0_sclk	norspi_clk	uart2_ahb_rx	ssis_sclk	
36	**SSI0MOSI**	ssi0_txd	norspi_dq[0]	uart2_ahb_tx	ssis_rxd	
37	**SSI0MISO**	ssi0_rxd	norspi_dq[1]	uart2_ahb_cts_n	ssis_txd	

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
38	**SSIOENO**	ssi0_en0	norspi_en[0]	uart2_ahb_rts_n	ssis_en	
39	**SSIOEN1**	ssi0_en1	norspi_en[1]			
45	**UART0RX**	uart0rx	uart2_ahb_rx			
46	**UART0TX**	uart0tx	uart2_ahb_tx			
51	**I2S_CLK**	i2s_clk	dmic_clk			
52	**I2S_SI**	i2s_si	dmic_dat			
53	**I2S_SO**	i2s_so				
54	**I2S_WS**	i2s_ws				
55	**CLK_AU**	clk_au				
56	**ENET_TXEN**	enet_txen	sc_a0	enet_txen	ssi1_txd	norspi_en[0]
57	**ENET_ TXD_0**	enet_txd_0	sc_a1	enet_txd_0	ssi1_en0	norspi_en[1]
58	**ENET_ TXD_1**	enet_txd_1	sc_a2	enet_txd_1	ssi1_en1	norspi_en[2]
59	**ENET_ TXD_2**		sc_a3	enet_txd_2	ssi1_en2	
60	**ENET_ TXD_3**		sc_b0	enet_txd_3	ssi1_en3	
61	**ENET_ RXD_0**	enet_rxd_0	sc_b1	enet_rxd_0	ssi1_rxd	norspi_dq[0]
62	**ENET_ RXD_1**	enet_rxd_1	sc_b2	enet_rxd_1		norspi_dq[1]
63	**ENET_ RXD_2**		sc_b3	enet_rxd_2		norspi_dq[2]
64	**ENET_ RXD_3**			enet_rxd_3		norspi_dq[3]
65	**ENET_RXDV**			enet_rxdv		
66	**ENET_MDC**	enet_mdc		enet_mdc		
67	**ENET_MDIO**	enet_mdio		enet_mdio		
68	**ENET_CLK_ TX**	enet_2nd_ref_ clk				
69	**ENET_CLK_ RX**	enet_ref_clk		enet_clk_rx		
70	**ENET_GTX_ CLK**	enet_gtx_clk		enet_gtx_clk		
71	**ENET_EXT_ OSC_CLK**			enet_ext_osc_ clk		
72	**WP**		nand_wp			
73	**SMIO_0**		nand_ce	norspi_clk		
74	**SMIO_1**		nand_rb	norspi_dq[4]		
75	**SMIO_2**		sd_clk			
76	**SMIO_3**		sd_cmd			
77	**SMIO_4**		sd_cd			
79	**SMIO_6**		nand_re	norspi_dq[5]		
80	**SMIO_7**		nand_we	norspi_dq[6]		
81	**SMIO_8**		nand_ale	norspi_dq[7]		
82	**SMIO_9**		nand_d[0]	norspi_en[0]		
83	**SMIO_10**		nand_d[1]	norspi_en[1]		
84	**SMIO_11**		nand_d[2]	norspi_en[2]		

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
85	**SMIO_12**		nand_d[3]	norspi_en[3]		
86	**SMIO_13**		nand_d[4]	norspi_dq[0]		
87	**SMIO_14**		nand_d[5]	norspi_dq[1]		
88	**SMIO_15**		nand_d[6]	norspi_dq[2]		
89	**SMIO_16**		nand_d[7]	norspi_dq[3]		
90	**SMIO_17**		nand_cle			
91	**SMIO_18**		sd_d[0]			
92	**SMIO_19**		sd_d[1]			
93	**SMIO_20**		sd_d[2]			
94	**SMIO_21**		sd_d[3]			
99	**SMIO_26**		sdxc_clk			
100	**SMIO_27**		sdxc_cmd			
101	**SMIO_28**		sdxc_d[0]			
102	**SMIO_29**		sdxc_d[1]			
103	**SMIO_30**		sdxc_d[2]			
104	**SMIO_31**		sdxc_d[3]			
111	**SMIO_38**		sd_reset			
115	**SVSYNC**	vin_svsync	idsp_pip_iopad_master_hsync			
116	**SHSYNC**	vin_shsync	idsp_pip_iopad_master_vsync			
118	**VD0_OUT_0**	vd0_out[0]				
119	**VD0_OUT_1**	vd0_out[1]				
120	**VD0_OUT_2**	vd0_out[2]				
121	**VD0_OUT_3**	vd0_out[3]				
122	**VD0_OUT_4**	vd0_out[4]				
123	**VD0_OUT_5**	vd0_out[5]				
124	**VD0_OUT_6**	vd0_out[6]				
125	**VD0_OUT_7**	vd0_out[7]				
126	**VD0_OUT_8**	vd0_out[8]				
127	**VD0_OUT_9**	vd0_out[9]				
128	**VD0_OUT_10**	vd0_out[10]				
129	**VD0_OUT_11**	vd0_out[11]				
130	**VD0_OUT_12**	vd0_out[12]				
131	**VD0_OUT_13**	vd0_out[13]				
132	**VD0_OUT_14**	vd0_out[14]				
133	**VD0_OUT_15**	vd0_out[15]				
134	**VD0_CLK**	vd0_clk				
135	**VD0_VSYNC**	vd0_vsync				
136	**VD0_HSYNC**	vd0_hsync				
137	**VD0_HVLD**	vd0_hvld				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
138	**VD_PWM**	pwm_0				

Table 3-13. General Purpose Input Output (GPIO) Multifunction-Capable Pins.

3.2.13 Pins: Analog to Digital Conversion (ADC)

Name	Location	Dir	Type	Description
ADC_CH_[1:2]	C5, C6	I	Analog	ADC analog input (2 channels)

Table 3-14. ADC Interface Pins.

3.2.14 Pins: Real Time Clock (RTC)

Name	Location	Dir	Type	Description
PWC_AVDD18	C16	P	Power	Power for RTC module and on-chip RTC oscillator. When **RTC_CP** is less than a specified voltage, the power controller will shut down and all registers will reset.
XI_RTC	D12	I	XOSC	Connect to RTC crystal
XO_RTC	C12	O		

Table 3-15. RTC Interface Pins.

3.2.15 Pins: Timer

Name	Location	Dir	Type	Description
TIMER0	C15	I/O	CMOS	Interval Timer 0 external clock source
TIMER1	C14	I/O	CMOS	Interval Timer 1 external clock source
TIMER2	D13	I/O	CMOS	Interval Timer 2 external clock source

Table 3-16. Timer Pins.

3.2.16 Pins: JTAG Control

Name	Location	Dir	Pad Type	Description
JTAG_CLK	R15	I	CMOS	Clock
JTAG_RST_L	R13	I	CMOS	Reset
JTAG_TDI	P16	I	CMOS	Data in
JTAG_TDO	R14	O	CMOS	Data out
JTAG_TMS	R16	I	CMOS	Test mode select

Table 3-17. JTAG Pins.

3.2.17 Pins: Global and Test

Name	Location	Dir	Type	Description
POR_L	B15	I	CMOS	Power-on reset pin (active low)
TEST_MODE	M10	I	CMOS	0 - Normal mode 1 - Test mode
XIN	D11	I	XOSC	24-MHz or 48-MHz crystal or crystal oscillator input
XOUT	C11	O		

Table 3-18. Global and Test Pins.

3.2.18 Pins: Power, Ground and PLL

Name	Location	Dir	Type	Description
AVDD33	C8	S	Analog Supply	Analog power supply
AVSS	E10, H10	G	Analog Ground	ADC analog ground
VDDI	F6, F8, F10, G6, G8, G10, H6, H8, J6, J8, K6, K8, K10, L6, L8, L10, M6	S	Digital Supply	Digital power supply
SD_VDDO	G14	S	Digital Supply	SD controller digital power
VDDO	F11, J11, P5, P9	S	IO Power	IO Power
VDDP	P8	S	IO Power	IO Power
VSSI	E5, E9, E11, F5, F7, F9, G5, G7, G9, G11, H5, H7, H9, J5, J7, J9, J10, K5, K7, K9, K11, L5, L7, L9, L11, M5, M7	G	Digital Ground	Digital ground
AVDD	C10	S	Analog Supply	Analog power supply
AVDD18	C7, D14	S	Analog Supply	Analog power supply
MIPI_ANA_ AVDD18_IO	C9	P	Digital Power	MIPI CMOS IO Power
SDXC_VDDO	K14	O	Digital Power	Digital Power for SDXC
VDDP	H13	S	IO Power	IO Power

Table 3-19. Power, Ground and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical: Overview

This chapter provides details on the electrical characteristics of the S5L33M chip as follows:

- (Section 4.1) Electrical: Overview
- (Section 4.2) Electrical: Absolute Ratings
- (Section 4.3) Electrical: Recommended Operating Conditions
- (Section 4.4) Electrical: Fail-Safe Pins
- (Section 4.5) Electrical: Video Signal Wave Forms and Timing
- (Section 4.6) Electrical: SD Controller Timing
- (Section 4.7) Electrical: eMMC Boot Timing

Note that the electrical details provided in this chapter are preliminary estimates.

4.2 Electrical: Absolute Ratings

The following table provides absolute ratings for the nominal analog / digital voltages of the S5L33M power rails.

Parameter	Minimum	Maximum
Analog supply voltage (3.0 V)	-0.3 V	3.6 V
Digital supply voltage (3.0 V)	-0.3 V	3.6 V
Analog supply voltage (1.8 V)	-0.3 V	1.98 V
Digital supply voltage (1.8 V)	-0.3 V	1.98 V
Analog supply voltage (0.9 V)	-0.3 V	0.95 V
Digital supply voltage (0.8 V)	-0.3 V	0.95 V
Digital I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Analog I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Operating temperature (case) (°C)	-20 °C	85 °C

Table 4-1. Absolute Ratings.

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Electrical: Recommended Operating Conditions

This section continues with recommended operating conditions for:

- (Section 4.3.1) Operating Conditions: Power Rails - DC Characteristics
- (Section 4.3.2) Operating Conditions: Digital I/O
- (Section 4.3.3) Operating Conditions: DRAM I/O
- (Section 4.3.4) Operating Conditions: PWC and RTC Power Supply
- (Section 4.3.5) Operating Conditions: Video Input
- (Section 4.3.6) Operating Conditions: Video DAC
- (Section 4.3.7) Operating Conditions: ADC Electrical Specifications
- (Section 4.3.8) Operating Conditions: Crystal and Reference Clock Requirements

4.3.1 Operating Conditions: Power Rails - DC Characteristics

Parameter [1]	Comments	Minimum	Typical	Maximum	Ripple
DDR[0:1]_VDDQ_CKE / DDR[0:1]_VDDQ	LPDDR2/3 Mode	1.14 V	1.2 V	1.3 V	2%
	DDR3 Mode	1.4 V	1.5 V	1.6 V	2%
	DDR3L Mode	1.28 V	1.35 V	1.45 V	2%
	-	-	-	-	-
AVDD		0.8 V	0.85 V	0.9 V	2%
-		-	-	-	-
AVDD18		1.7 V	1.8 V	1.9 V	2%
-		-	-	-	-
-		-	-		-
-		-	-	-	-
PWC_AVDD18		0.7 V	1.8 V	1.98 V	2%
AVDD33		2.85 V	3.0 V	3.6 V	2%
VDDI		0.68 V	0.7 V	0.75 V	2%
VDDO	3.0-V mode	2.85 V	3.0 V	3.6 V	2%
	1.8-V mode	1.7 V	1.8 V	1.9 V	2%
-	-	-	-	-	-
	-	-	-	-	-
VDDO_SD / VDDO_SDXC	SD / SDIO mode	2.85 V	3.0 V	3.6 V	2%
	SDXC mode	1.7 V	1.8 V	1.9 V	2%
MIPI_AVDD18_IO	LVCMOS	1.7 V	1.8 V	1.9 V	2%
	MIPI	1.06 V	1.1 V	1.3 V	2%
VDDP		1.7 V	1.8 V	1.9 V	2%
-		-	-	-	-
-		-	-	-	-

Table 4-2. Power Rails: DC Characteristics (Preliminary and Subject to Change).

Note:

The electrical details provided in this chapter are preliminary estimates and are subject to change. Please contact an Ambarella representative for current electrical specifications.

4.3.2 Operating Conditions: Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.7 V
VIH	Input High Voltage	2.0 V		3.6 V (for 3.3 V-tolerant pins)
VOL	Output Low Voltage			0.4 V
VOH	Output High Voltage	2.4 V		

Table 4-3. Digital I/O Characteristics @ VDDO 3.0V (Preliminary).

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.54 V
VIH	Input High Voltage	1.2 V		2.0V
VOL	Output Low Voltage			0.36V
VOH	Output High Voltage	1.44 V		

Table 4-4. Digital I/O Characteristics @ VDDO 1.8V

4.3.3 Operating Conditions: DRAM I/O

4.3.3.1 DRAM: DC Supply Voltage Levels

Parameter	Comments	Minimum	Typical	Maximum
DDR_VDDQ		See Section 4.3.1		
DDR_VDDQ_CKE		See Section 4.3.1		
-		-		
-		-		
VTT	Termination voltage	DDR_VREF - 0.04 V	DDR_VREF	DDR_VREF + 0.04 V
DDR_VREF_1	Input reference level	0.49 * DDR_VDDQ	0.5 * VDDQ	0.51 * DDR_VDDQ

Table 4-5. DRAM I/O Characteristics - DC Supply Voltage Levels (Preliminary).

4.3.3.2 DRAM: SSTL I/O DC Specifications

Parameter	Comments	Minimum	Typical	Maximum
VIHT	DC input logic threshold high			DDR_VREF + 0.05 V
VILT	DC input logic threshold low	DDR_VREF - 0.05 V		
VIH	DC input voltage high	DDR_VREF + 100 mV		VDDQ + 0.3 V
VIL	DC input voltage low	-0.3 V		DDR_VREF - 100 mV
VOH	DC output logic high	DDR_VDDQ		
VOL	DC output logic low			0 V
RTT1	RTT effective impedance	60 Ohms	75 Ohms	90 Ohms
RTT2	RTT effective impedance	120 Ohms	150 Ohms	180 Ohms

Table 4-6. DRAM I/O Characteristics - SSTL I/O DC Specifications (Preliminary).

4.3.4 Operating Conditions: PWC and RTC Power Supply

Parameter	Comments	Minimum	Typical	Maximum
PWC_AVDD18	RTC module supply	0.7 V	1.8 V	1.98 V
-	-	-	-	-
VIH	-	1.7 V		
VIL	-			1.0 V
VOH	PWC_RSTOB VOH(min)=1.5V at 10uA loading; need to add buffer for higher loadings.	1.5 V		
VOL				0.5 V
VIH	For XI_RTC	0.4 V		1.0 V
VIL	For XI_RTC			0.2 V

Table 4-7. PWC and RTC Supply.

4.3.5 Operating Conditions: Video Input

4.3.5.1 VIN: SLVS / LVCMOS I/O

Parameter	Symbol	Comment	Min	Typ.	Max.
Digital Input Voltage	VIL	LVCMOS 1.2 V			0.5 V
		LVCMOS 1.8 V			0.6 V
	VIH	LVCMOS 1.2 V	0.8 V		
		LVCMOS 1.8 V	1.2 V		
Differential Input for SLVS	V_{CM}		0.2 V		1.0 V
	V_{DIFF}		70 mV		400 mV

Table 4-8. DC Characteristics: SLVS Interface.

4.3.6 Operating Conditions: Video DAC

Parameter	Comments	Minimum	Typical	Maximum
IO_{FS}	IO out current		34.6 mA	
I_{OP}	Operating current		36 mA	
V(IO)	Out voltage full scale	1.17 V	1.28 V	1.43 V
Resolution	DAC resolution			10 bits
DNL	Differential non-linearity error			±2 LSB
INL	Integral non-linearity error			±4 LSB
VREF	Reference voltage			1.22 V

Table 4-9. Video DAC Electrical Specification.

4.3.7 Operating Conditions: ADC Electrical Specifications

4.3.7.1 ADC Electrical: DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VREF	Reference voltage (Top) (Low reference is ADC_AVSS)	ADC_AVDD	ADC_AVDD	ADC_AVDD
VIN	Analog input voltage	ADC_AVSS		VREF
N	Resolution		12 bits	
INL	INL			±4 LSB
DNL	DNL			±2 LSB

Table 4-10. ADC DC Specification.

4.3.7.2 ADC Electrical: AC Specification

Parameter	Comments	Minimum	Typical	Maximum
Fs	Sampling rate	50 K		1 MS/s
FCLK	Sampling clock		12 MHz	
SNDR	Signal-to-noise and distortion ratio (Fclk = 5 MHz and AIN = 50 KHz*)	54 dB	60 dB	

Table 4-11. ADC AC Specification.

4.3.8 Operating Conditions: Crystal and Reference Clock Requirements

4.3.8.1 Crystal and Reference Clock Requirements: 24 MHz

Description	Minimum	Typical	Maximum
Crystal frequency	N/A	24 MHz only	N/A
Crystal accuracy			± 30 PPM
Cycle-to-cycle jitter			± 200 ps
Long-term jitter			± 500 ps

Table 4-12. Jitter Specifications.

4.3.8.2 Crystal and Reference Clock Requirements: 32.768 KHz

Description	Minimum	Typical	Maximum
Crystal accuracy			± 30 PPM

Table 4-13. Jitter Specifications (32.768 KHz).

4.4 Electrical: Fail-Safe Pins

The S5L33M chip provides a number of fail-safe CMOS pins that can have active signals at or below 3.6 V when the S5L33M is powered down.

Pin Name
TIMER0
TIMER1
TIMER2
IDCCLK
IDCDATA
IDC2CLK
IDC2DATA
IDC3CLK
IDC3DATA
IR_IN

Pin Name
SSI0CLK
SSI0MOSI
SSI0MISO
SSI0ENO
SSI0EN1
SSI2CLK
UART0RX
UART0TX
I2S_CLK
I2S_SI
I2S_SO
I2S_WS
CLK_AU
JTAG_TDO
DETECT_VBUS
WP
SMIO_0
SMIO_2
SMIO_3
SMIO_4
SMIO_18
SMIO_19
SMIO_20
SMIO_21
SMIO_26
SMIO_27
SMIO_28
SMIO_29
SMIO_30
SMIO_31
SVSYNC
SHSYNC
VD0_OUT_8
VD0_OUT_9
VD0_OUT_10
VD0_OUT_11
VD0_OUT_12
VD0_OUT_13
VD0_OUT_14
VD0_OUT_15
VD0_CLK
VD_PWM
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_5
GPIO_6

Table 4-14. Fail-Safe Pins Which Can Have Active Signals At or Below 3.6 V When the S5L33M is Powered Down.

4.5 Electrical: Video Signal Wave Forms and Timing

4.5.1 Video Waveform: Video Input (VIN) LVCMOS Timing

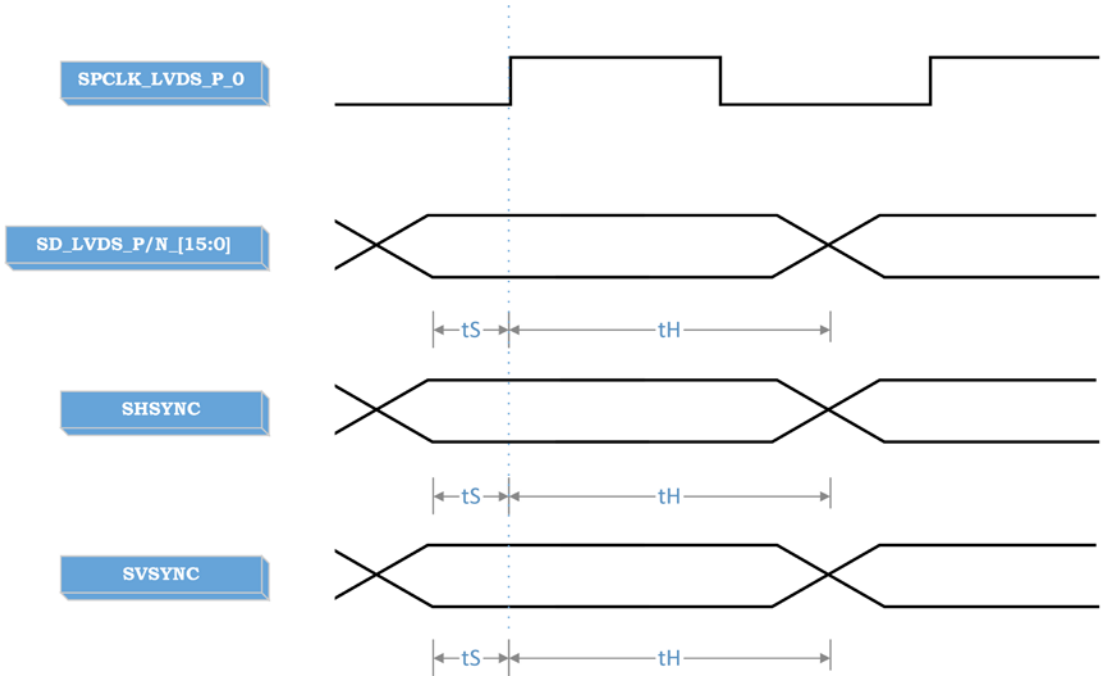


Figure 4-1. Video Input (VIN) LVCMOS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_[16:0]**	2 ns	2 ns	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.
HSync: **SHSYNC**	2 ns	2 ns	
VSync: **SVSYNC**	2 ns	2 ns	
SField: (See Section 2.3)	2 ns	2 ns	

*Table 4-15. LVCMOS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.2 Video Waveform: Video Input (VIN) SLVS Timing

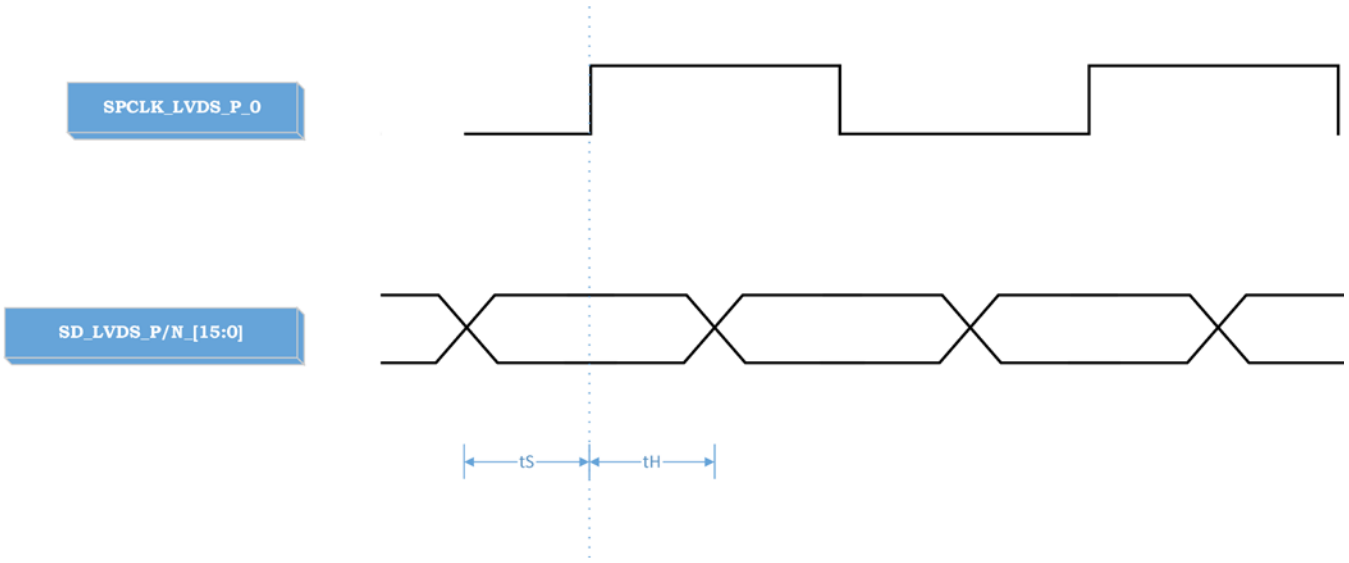


Figure 4-2. Video Input (VIN) SLVS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_[16:0]**	150 ps	150 ps	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.

*Table 4-16. SLVS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.3 Video Waveform: Video Output (VOUT) Timing

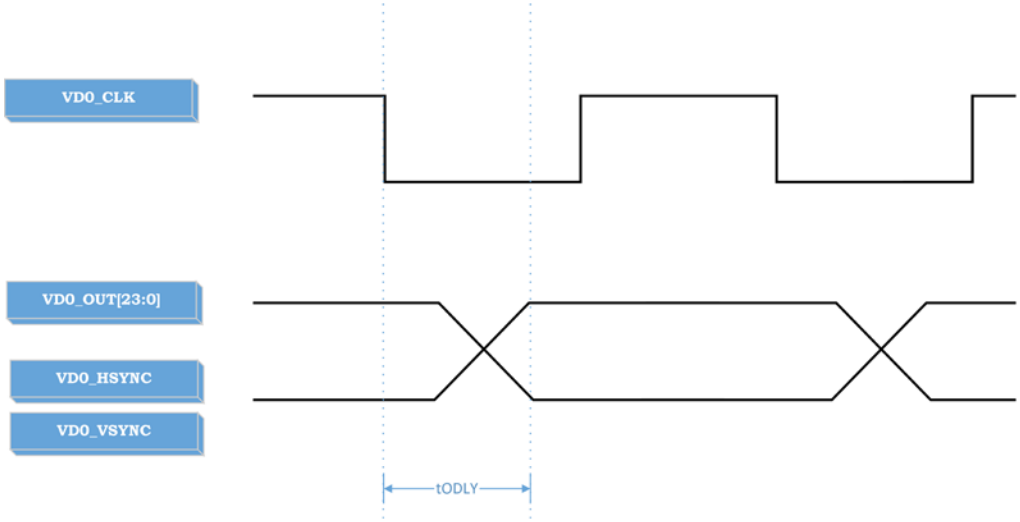


Figure 4-3. Video Output Timing.

Parameter	Minimum	Typical	Maximum	Comment
VD0_CLK frequency		Resolution dependent		Assume the data is latched out at the falling edge of **VD0_CLK**.
VD0_CLK duty	40%	50%	60%	
tODLY output delay	-2 ns		2 ns	

*Table 4-17. Video Output Timing Setup/Hold With Respect to **VD0_CLK**.*

4.6 Electrical: SD Controller Timing

There are two voltages at which the SD card is operated:

- (Section 4.6.1) SD Controller Timing: 3.3 V
- (Section 4.6.2) SD Controller Timing: 1.8 V

4.6.1 SD Controller Timing: 3.3 V

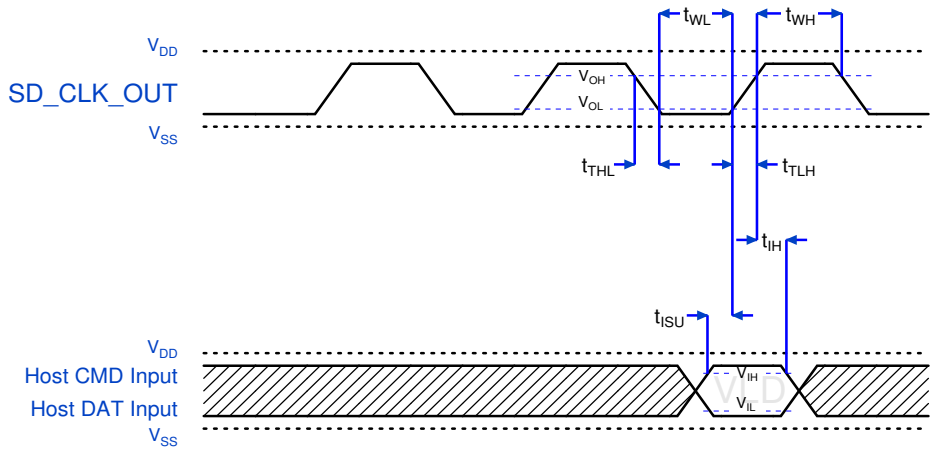


Figure 4-4. SD Host Input Timing.

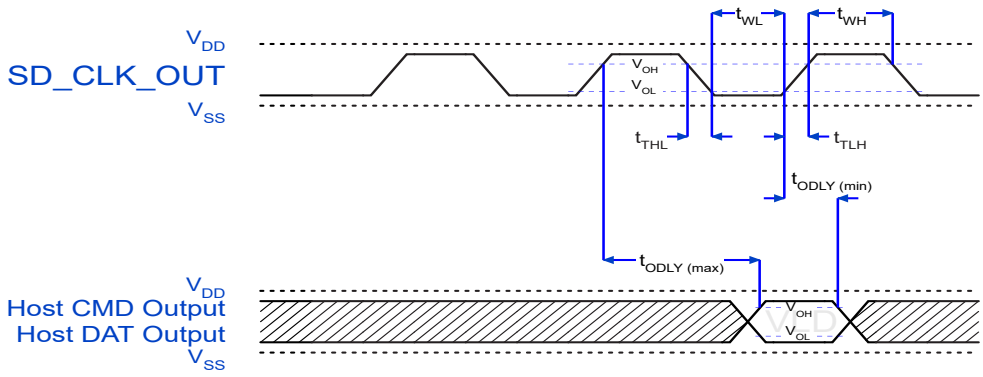


Figure 4-5. SD Host Output Timing.

Parameter	Symbol	Min	Max	Unit	Comment
Clock CLK: All values are referred to as min (VIH) and max (VIL)					
Clock Frequency: Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Frequency: Identification Mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Low Time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock High Time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Rise Time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Fall Time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 Card)
Inputs CMD, DAT: Referenced to CLK					
Input Set-Up Time	t_{ISU}	5.83		ns	C_{CARD} ≤ 10 pF (1 Card)
Input Hold Time	t_{IH}	1.5		ns	C_{CARD} ≤ 10 pF (1 Card)
Outputs CMD, DAT: Referenced to CLK at 50 MHz					
Output Delay Time	t_{ODLY}	8.85	12.16	ns	C_L ≤ 40 pF (1 Card)

Table 4-18. SD Controller Timing Parameters.

Parameter	Symbol	Min	Max	Unit	Comment
Supply Voltage	V_{DD}	2.70	3.60	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	
Output Low Voltage	V_{OL}	-	0.125* V_{DD}	V	
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD} +0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0 V to V_{DD}(min)

Table 4-19. Threshold Level for High Voltage.

4.6.2 SD Controller Timing: 1.8 V

The card input setup time and hold time are measured at V_{IL} (max.) and V_{IH} (min.). The timing parameter, Clock Threshold (V_{CT}), is used to indicate clock reference point and is defined as 0.975V.

Parameter	Symbol	Min	Max	Unit	Comment
Clock CLK: All values are referred to as min (VIH) and max (VIL)					
Clock period	t_{CLK}	10	-	ns	100 MHz (Max). Between rising edge. V_{CT}=0.975 V
Clock rising/failing time	t_{CR}, t_{CF}	-	0x2 * t_{CLK}	ns	C_{CARD} = 10 pF
Clock duty	-	30	70	%	
Card Inputs CMD, DAT: Referenced to CLK					
Input set-up time	t_{IS}	3	-	ns	C_{CARD} = 10 pF, V_{CT}=0.975V
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} = 5 pF, V_{CT}=0.975V
Outputs CMD, DAT: Referenced to CLK at 50 MHz					
Output delay time	t_{ODLY}	-	7.5	ns	C_L = 30 pF
Output hold time	t_{OHLD}	1.5	-	ns	C_L = 15 pF

Table 4-20. SD Controller Timing Parameters in SDR50 Mode.

Parameter	Symbol	Min	Max	Unit	Comment
Supply voltage	V_{DD}	2.70	3.60	V	
Regular voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High voltage	V_{OH}	1.4	-	V	
Output Low voltage	V_{OL}	-	0.45	V	
Input High voltage	V_{IH}	1.27	2.00	V	
Input Low voltage	V_{IL}	V_{SS}-0.30	0.58	V	

Table 4-21. Threshold Level for 1.8V Signaling.

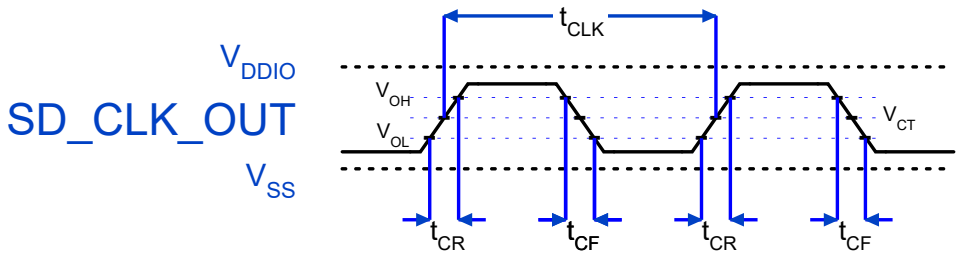


Figure 4-6. Clock Signal Timing.

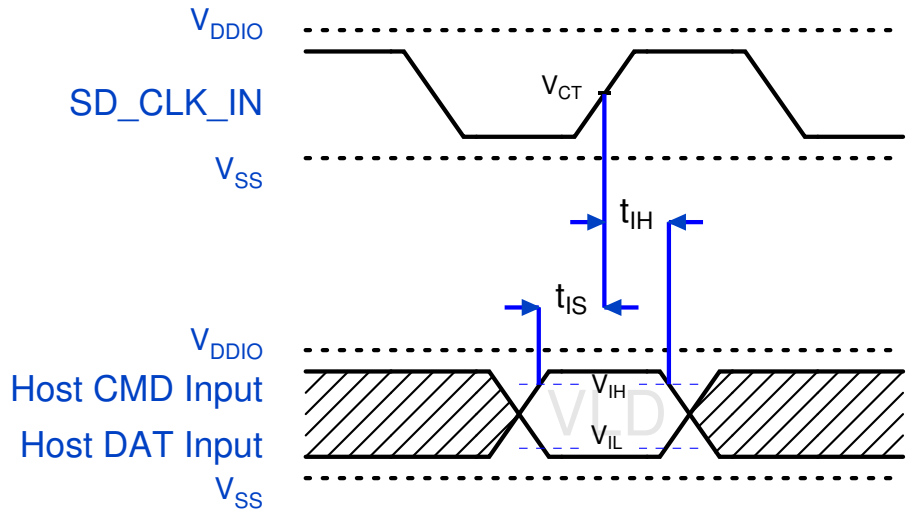


Figure 4-7. SD Host Input Timing.

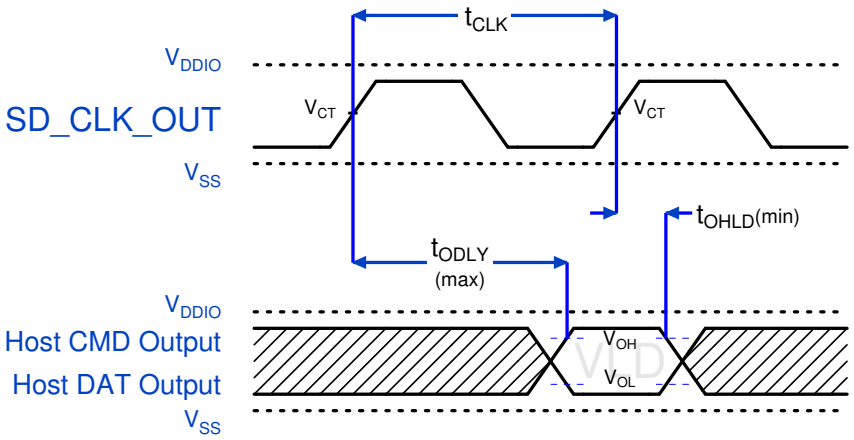


Figure 4-8. SD Host Output Timing.

4.7 Electrical: eMMC Boot Timing

To successfully boot from eMMC, the eMMC device should return boot data with the following timing constraints.

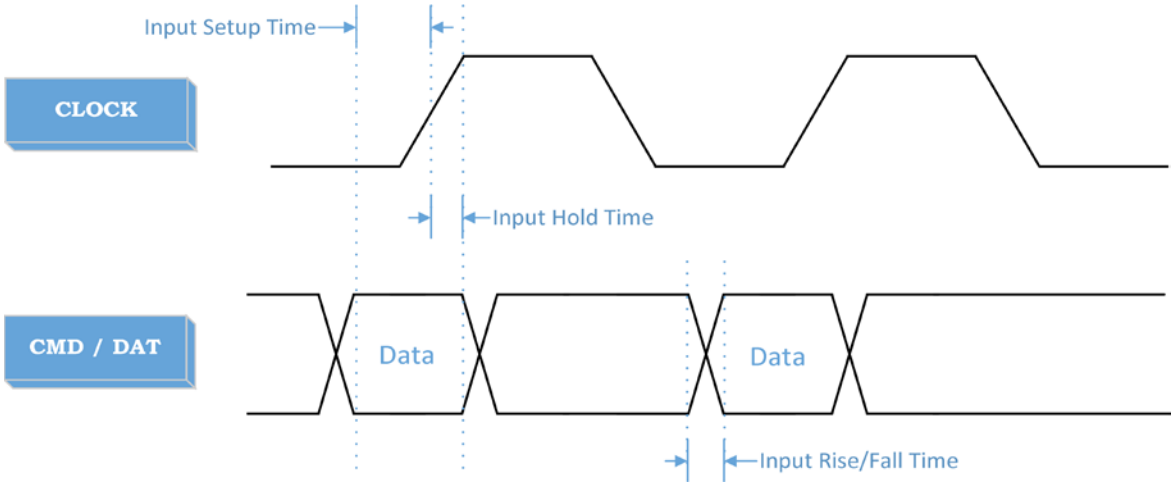


Figure 4-9. eMMC Boot Timing Diagram.

Parameter	Minimum	Maximum
Host CMD / DAT Input Timing		
Input setup time	6 ns	
Input hold time	1.5 ns	
Signal rise time		3 ns
Signal fall time		3 ns

Table 4-22. eMMC Boot Timing.

Note:

CMD / DAT input rise and fall time are measured by VIL and VIH.

5. PACKAGE

The S5L33M chip has a 256-pin FC TFBGA package (11 mm x 11 mm).

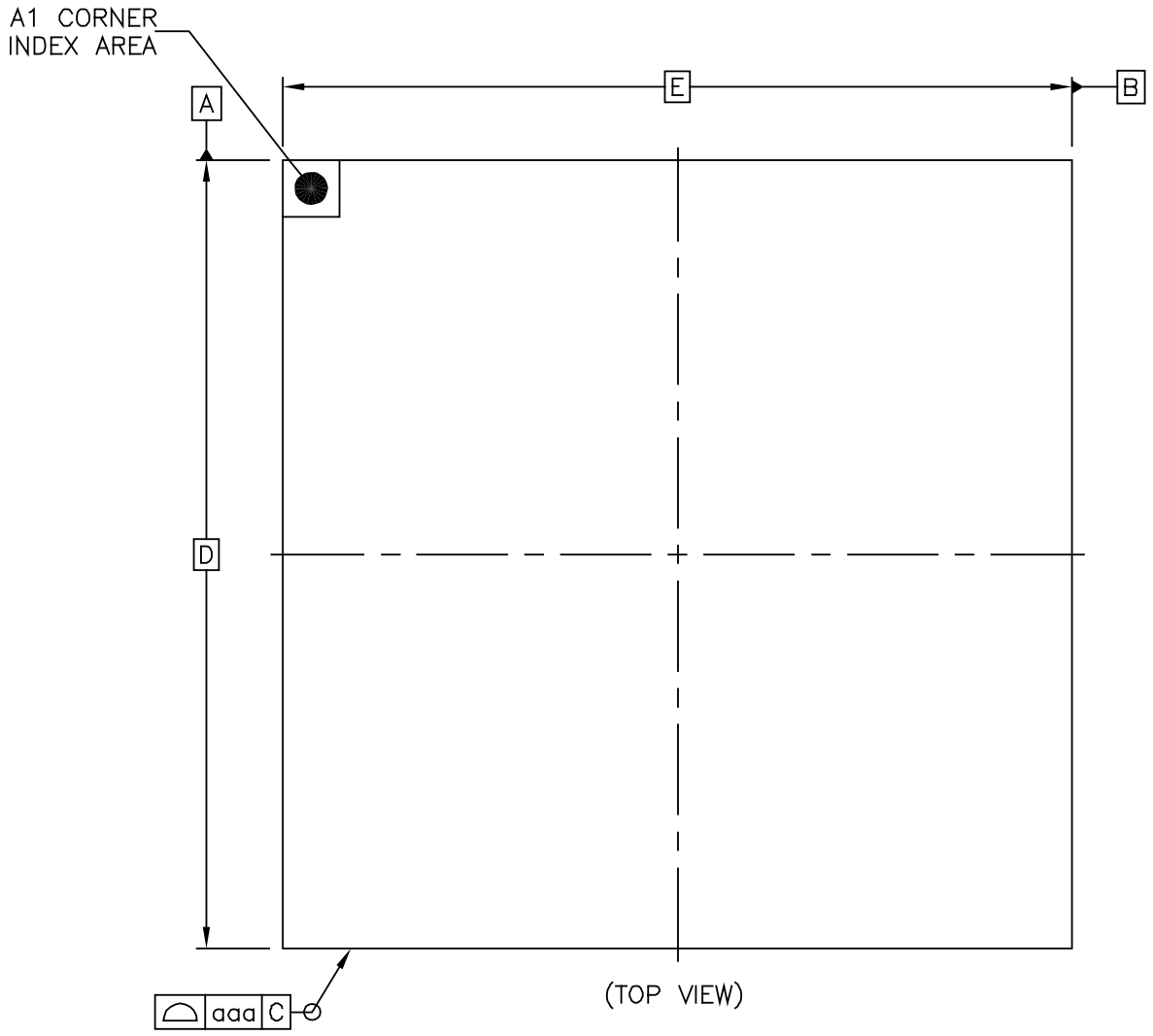


Figure 5-1. Top View of the S5L33M Package.

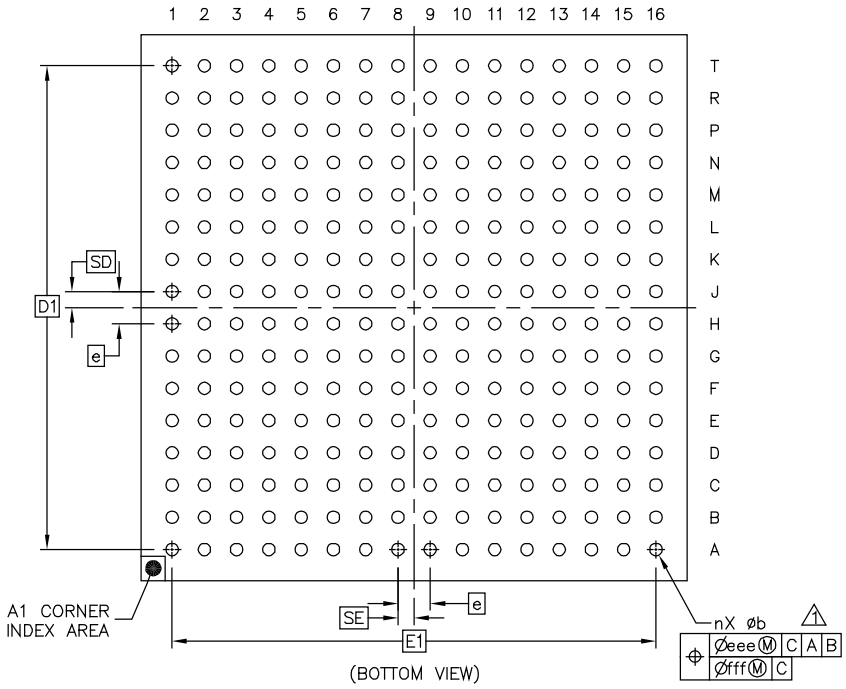


Figure 5-2. Bottom View of the S5L33M Package.

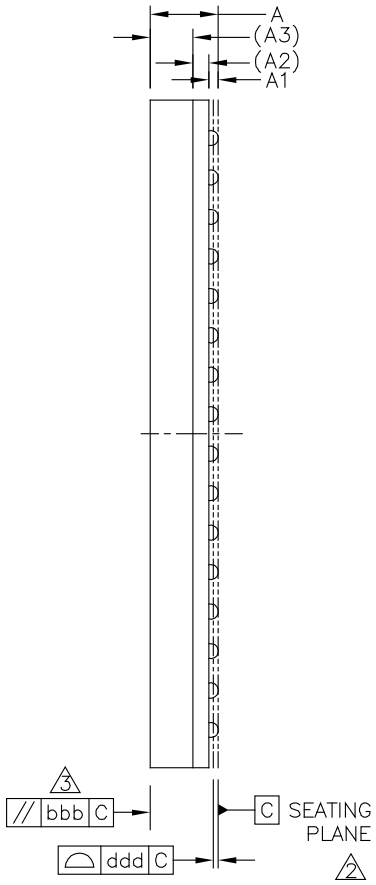


Figure 5-3. Side View of the S5L33M Package.

Description	Symbol	Minimum	Nominal	Maximum
Total Thickness	A			1.2
Stand Off	A1	0.11		0.21
Substrate Thickness	A2		0.26 REF	
Mold Thickness	A3		0.7 REF	
Body Size	D		11 BSC	
	E		11 BSC	
Ball Diameter			0.25	
Ball Opening			0.25	
Ball Width	b	0.2		0.3
Ball Pitch	e		0.65 BSC	
Ball Count	n		256	
Edge Ball Center to Center	D1		9.75 BSC	
	E1		9.75 BSC	
Body Center to Contact Ball	SD		0.325 BSC	
	SE		0.325 BSC	
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

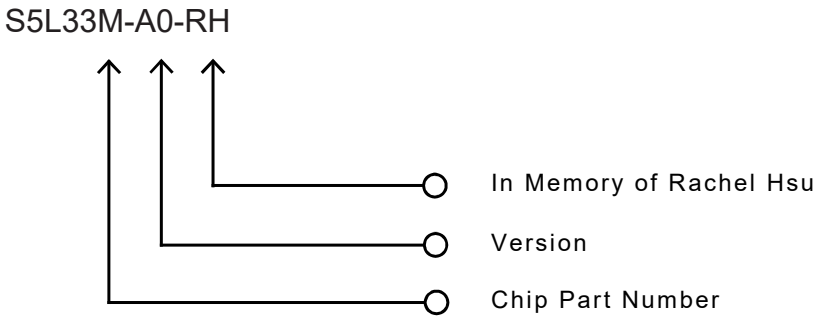
Table 5-1. Dimensions of the S5L33M Package (millimeters).

Notes for table and figures:

- All dimensions are in millimeters.
- Dimension b is measured at the maximum solder ball diameter, parallel to Datum Plane C.
- Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
- Parallelism measurement excludes any effect of mark on top surface of the package.
- Dimension and Tolerances: ASME Y14.5M

6. CONTACT AND ORDER INFORMATION

All chips in the S5LM series are lead-free, halogen-free and RoHS compliant.



For complete Ambarella contact information, please visit www.ambarella.com.

7. PIN LIST AND MAPPING TABLE

This section provides a list of the 256 external pins according to their location on the S5L33M chip. Figure 7-1 below indicates the orientation of the pins by column (numbers) and row (letters).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	ddr_addr_8	ddr_addr_2	ddr_addr_9	ddr_calibr	spclk_lvds_p_1	sd_lvds_p_4	sd_lvds_p_5	sd_lvds_p_6	sd_lvds_p_7	spclk_lvds_p_0	sd_lvds_p_0	sd_lvds_p_1	sd_lvds_p_2	sd_lvds_p_3	usb_rext	usb_dp	A
B	ddr_addr_4	ddr_addr_6	ddr_addr_7	ddr_addr_13	spclk_lvds_n_1	sd_lvds_n_4	sd_lvds_n_5	sd_lvds_n_6	sd_lvds_n_7	spclk_lvds_n_0	sd_lvds_n_0	sd_lvds_n_1	sd_lvds_n_2	sd_lvds_n_3	por_l	usb_dm	B
C	ddr_addr_11	ddr_addr_14	ddr_addr_5	ddr_reset	adc_ch_1	adc_ch_2	avdd18	avdd33	mipi_avdd18_io	avdd	xout	xo_rtc	detect_vbus	timer1	timer0	pwc_avdd18	C
D	ddr_ba_1	ddr_addr_1	ddr_addr_3	ddr_addr_0	ddr_vddq_cke	dac_rset	svsync	shsync	clk_si	ir_in	xin	xi_rtc	timer2	avdd18	smio_30	smio_31	D
E	ddr_addr_10	ddr_addr_12	ddr_ba_0	ddr_vddq	VSSi	dac_io	dac_vrefin	dac_comp	VSSi	avss	VSSi	smio_21	smio_26	smio_27	smio_28	smio_29	E
F	ddr_ras	ddr_cke	ddr_ba_2	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	vddo	hdmi_rext	smio_18	smio_4	smio_3	smio_2	F
G	ddr_cas	ddr_ck_bar	ddr_we	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi	smio_14	smio_38	sd_vddo	smio_20	smio_19	G
H	ddr_vref_1	ddr_ck	ddr_odt	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	avss	smio_1	smio_13	vddp	smio_15	smio_16	smio_17	H
J	ddr_dq_10	ddr_dq_14	ddr_dq_13	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	VSSi	vddo	smio_8	smio_9	smio_10	smio_11	smio_12	J
K	ddr_dqs_1	ddr_dq_8	ddr_dq_15	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi	wp	smio_0	sdxc_vddo	smio_6	smio_7	K
L	ddr_dqs_bar_1	ddr_dm_1	ddr_dq_12	ddr_vddq	VSSi	VDDi	VSSi	VDDi	VSSi	VDDi	VSSi	ssi0en1	ssi0en0	ssi0mosi	ssi0miso	ssi0clk	L
M	ddr_dq_11	ddr_dq_5	ddr_dq_9	ddr_vddq	VSSi	VDDi	VSSi	vd0_clk	enet_mdio	test_mode	clk_au	gpio_2	gpio_1	gpio_0	uart0tx	uart0rx	M
N	ddr_dq_3	ddr_dq_7	ddr_dqs_0	vd0_out_3	vd0_out_2	vd0_out_12	vd0_out_11	vd0_out_8	enet_mdc	enet_txd_3	enet_clk_tx	enet_rxdv	idcclk	gpio_6	gpio_5	gpio_3	N
P	ddr_dq_1	ddr_dm_0	ddr_dqs_bar_0	vd0_out_4	vddo	vd0_out_13	vd0_out_10	vddp	vddo	enet_txd_2	enet_rxd_3	enet_ext_osc_clk	idcdata	idc3clk	idc3data	jtag_tdi	P
R	ddr_dq_0	ddr_dq_2	vd_pwm	vd0_out_5	vd0_out_1	vd0_out_14	vd0_out_9	vd0_hvld	enet_gtx_clk	enet_txd_1	enet_rxd_2	enet_clk_rx	jtag_rst_l	jtag_tdo	jtag_clk	jtag_tms	R
T	ddr_dq_4	ddr_dq_6	vd0_out_7	vd0_out_6	vd0_out_0	vd0_out_15	vd0_hsync	vd0_vsync	enet_txen	enet_txd_0	enet_rxd_1	enet_rxd_0	i2s_so	i2s_si	i2s_ws	i2s_clk	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7-1. Pin Map for the S5L33M Chip.

The table below lists all of the external pins on the S5L33M chip in alphabetic order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A1	**DDR_ADDR_8**	DDR	SSTL						
A2	**DDR_ADDR_2**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A3	**DDR_ ADDR_9**	DDR	SSTL						
A4	**DDR_CAL-IBR**	DDR	SSTL						
A5	**SPCLK_ LVDS_P_1**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A6	**SD_ LVDS_P_4**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A7	**SD_ LVDS_P_5**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A8	**SD_ LVDS_P_6**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A9	**SD_ LVDS_P_7**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A10	**SPCLK_ LVDS_P_0**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A11	**SD_ LVDS_P_0**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A12	**SD_ LVDS_P_1**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A13	**SD_ LVDS_P_2**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A14	**SD_ LVDS_P_3**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
A15	**USB_REXT**	USB	Analog						
A16	**USB_DP**	USB	Analog						
B1	**DDR_ ADDR_4**	DDR	SSTL						
B2	**DDR_ ADDR_6**	DDR	SSTL						
B3	**DDR_ ADDR_7**	DDR	SSTL						
B4	**DDR_ ADDR_13**	DDR	SSTL						
B5	**SPCLK_ LVDS_N_1**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B6	**SD_ LVDS_N_4**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B7	**SD_ LVDS_N_5**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
B8	**SD_ LVDS_N_6**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B9	**SD_ LVDS_N_7**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B10	**SPCLK_ LVDS_N_0**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B11	**SD_ LVDS_N_0**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B12	**SD_ LVDS_N_1**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B13	**SD_ LVDS_N_2**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B14	**SD_ LVDS_N_3**	Sensor	Sub-LVDS / SLVS / LVC-MOS / MIPI						
B15	**POR_L**	Global	CMOS						
B16	**USB_DM**	USB	Analog						
C1	**DDR_ ADDR_11**	DDR	SSTL						
C2	**DDR_ ADDR_14**	DDR	SSTL						
C3	**DDR_ ADDR_5**	DDR	SSTL						
C4	**DDR_RESET**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
C5	**ADC_CH_1**	ADC	Analog						
C6	**ADC_CH_2**	ADC	Analog						
C7	**AVDD18**	Power	Analog Supply						
C8	**AVDD33**	Power	Analog Supply						
C9	**MIPI_ AVDD18_IO**	Power	Analog Supply						
C10	**AVDD**	Power	Analog Supply						
C11	**XOUT**	Global	XOSC						
C12	**XO_RTC**	RTC	Analog						
C13	**DETECT_ VBUS**	USB	CMOS						
C14	**TIMER1**	GPIO	CMOS	tm12_clk	ssi2_en3	idsp_pip_ io_pad_ master_ hsync			26
C15	**TIMER0**	GPIO	CMOS	tm11_clk	ssi2_en2				25
C16	**PWC_ AVDD18**	PWC	Analog Supply						
D1	**DDR_BA_1**	DDR	SSTL						
D2	**DDR_ ADDR_1**	DDR	SSTL						
D3	**DDR_ ADDR_3**	DDR	SSTL						
D4	**DDR_ ADDR_0**	DDR	SSTL						
D5	**DDR_VDDQ_ CKE**	DDR	SSTL						
D6	**DAC_RSET**	DAC	Analog						
D7	**SVSYNC**	Sensor	CMOS	vin_svsync	idsp_pip_ iopad_mas- ter_hsync				115
D8	**SHSYNC**	Sensor	CMOS	vin_shsync	idsp_pip_ iopad_mas- ter_vsync				116
D9	**CLK_SI**	Sensor	CMOS						
D10	**IR_IN**	IR	CMOS	ir_in					34
D11	**XIN**	Global	XOSC						
D12	**XI_RTC**	RTC	Analog						
D13	**TIMER2**	GPIO	CMOS	tm13_clk	ssi0_en3	idsp_ pip_io- pad_mas- ter_vsync			27
D14	**AVDD18**	Power	Analog Supply						
D15	**SMIO_30**	SMIO	CMOS		sdxc_d[2]		sc_d2	ssis_txd	103
D16	**SMIO_31**	SMIO	CMOS		sdxc_d[3]		sc_d3	ssis_en	104

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
E1	**DDR_ ADDR_10**	DDR	SSTL						
E2	**DDR_ ADDR_12**	DDR	SSTL						
E3	**DDR_BA_0**	DDR	SSTL						
E4	**DDR_VDDQ**	Power	DDR HOST Supply						
E5	**VSSI**	Power	Ground						
E6	**DAC_IO**	DAC	Analog						
E7	**DAC_VREFIN**	DAC	Analog						
E8	**DAC_COMP**	DAC	Analog						
E9	**VSSI**	Power	Ground						
E10	**AVSS**	Power	Ground						
E11	**VSSI**	Power	Ground						
E12	**SMIO_21**	SMIO	CMOS		sd_d[3]				94
E13	**SMIO_26**	SMIO	CMOS		sdxc_clk				99
E14	**SMIO_27**	SMIO	CMOS		sdxc_cmd				100
E15	**SMIO_28**	SMIO	CMOS		sdxc_d[0]		sc_d0	ssis_sclk	101
E16	**SMIO_29**	SMIO	CMOS		sdxc_d[1]		sc_d1	ssis_rxd	102
F1	**DDR_RAS**	DDR	SSTL						
F2	**DDR_CKE**	DDR	SSTL						
F3	**DDR_BA_2**	DDR	SSTL						
F4	**DDR_VDDQ**	DDR	SSTL						
F5	**VSSI**	Power	Ground						
F6	**VDDI**	Power	Digital Supply						
F7	**VSSI**	Power	Ground						
F8	**VDDI**	Power	Digital Supply						
F9	**VSSI**	Power	Ground						
F10	**VDDI**	Power	Digital Supply						
F11	**VDDO**	Power	IO Power						
F12	**HDMI_REXT**	HDMI	ANA-LOG						
F13	**SMIO_18**	SMIO	CMOS		sd_d[0]				91
F14	**SMIO_4**	SMIO	CMOS		sd_cd				77
F15	**SMIO_3**	SMIO	CMOS		sd_cmd				76
F16	**SMIO_2**	SMIO	CMOS		sd_clk				75
G1	**DDR_CAS**	DDR	SSTL						
G2	**DDR_CK_ BAR**	DDR	SSTL						
G3	**DDR_WE**	DDR	SSTL						
G4	**DDR_VDDQ**	Power	DDR HOST Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
G5	**VSSI**	Power	Ground						
G6	**VDDI**	Power	IO Power						
G7	**VSSI**	Power	Ground						
G8	**VDDI**	Power	IO Power						
G9	**VSSI**	Power	Ground						
G10	**VDDI**	Power	IO Power						
G11	**VSSI**	Power	Ground						
G12	**SMIO_14**	SMIO	CMOS		nand_d[5]	norspi_ dq[1]			87
G13	**SMIO_38**	SMIO	CMOS		sd_reset				111
G14	**SD_VDDO**	Power	IO Power						
G15	**SMIO_20**	SMIO	CMOS		sd_d[2]				93
G16	**SMIO_19**	SMIO	SMOS		sd_d[1]				92
H1	**DDR_ VREF_1**	DDR	SSTL						
H2	**DDR_CK**	DDR	SSTL						
H3	**DDR_ODT**	DDR	SSTL						
H4	**DDR_VDDQ**	Power	DDR HOST Supply						
H5	**VSSI**	Power	Ground						
H6	**VDDI**	Power	Digital Supply						
H7	**VSSI**	Power	Ground						
H8	**VDDI**	Power	Digital Supply						
H9	**VSSI**	Power	Ground						
H10	**AVSS**	Power	Ground						
H11	**SMIO_1**	SMIO	CMOS		nand_rb	norspi_ dq[4]			74
H12	**SMIO_13**	SMIO	CMOS		nand_d[4]	norspi_ dq[0]			86
H13	**VDDP**	Power	Pre-driver Supply						
H14	**SMIO_15**	SMIO	CMOS		nand_d[6]	norspi_ dq[2]			88
H15	**SMIO_16**	SMIO	CMOS		nand_d[7]	norspi_ dq[3]			89
H16	**SMIO_17**	SMIO	CMOS		nand_cle				90
J1	**DDR_DQ_10**	DDR	SSTL						
J2	**DDR_DQ_14**	DDR	SSTL						
J3	**DDR_DQ_13**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
J4	**DDR_VDDQ**	Power	DDR HOST Supply						
J5	**VSSI**	Power	Ground						
J6	**VDDI**	Power	Digital Supply						
J7	**VSSI**	Power	Ground						
J8	**VDDI**	Power	Digital Supply						
J9	**VSSI**	Power	Ground						
J10	**VSSI**	Power	Ground						
J11	**VDDO**	Power	IO Power						
J12	**SMIO_8**	SMIO	CMOS		nand_ale	norspi_ dq[7]			81
J13	**SMIO_9**	SMIO	CMOS		nand_d[0]	norspi_ en[0]			82
J14	**SMIO_10**	SMIO	CMOS		nand_d[1]	norspi_ en[1]			83
J15	**SMIO_11**	SMIO	CMOS		nand_d[2]	norspi_ en[2]			84
J16	**SMIO_12**	SMIO	CMOS		nand_d[3]	norspi_ en[3]			85
K1	**DDR_DQS_1**	DDR	SSTL						
K2	**DDR_DQ_8**	DDR	SSTL						
K3	**DDR_DQ_15**	DDR	SSTL						
K4	**DDR_VDDQ**	Power	DDR HOST Supply						
K5	**VSSI**	Power	Ground						
K6	**VDDI**	Power	Digital Supply						
K7	**VSSI**	Power	Ground						
K8	**VDDI**	Power	Digital Supply						
K9	**VSSI**	Power	Ground						
K10	**VDDI**	Power	Digital Supply						
K11	**VSSI**	Power	Ground						
K12	**WP**	GPIO	CMOS		nand_wp				72
K13	**SMIO_0**	SMIO	CMOS		nand_ce	norspi_clk			73
K14	**SDXC_VDDO**	Power	IO Power						
K15	**SMIO_6**	SMIO	CMOS		nand_re	norspi_ dq[5]			79
K16	**SMIO_7**	SMIO	CMOS		nand_we	norspi_ dq[6]			80
L1	**DDR_DQS_ BAR_1**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
L2	**DDR_DM1**	DDR	SSTL						
L3	**DDR_DQ_12**	DDR	SSTL						
L4	**DDR_VDDQ**	DDR	SSTL						
L5	**VSSI**	Power	Ground						
L6	**VDDI**	Power	Digital Supply						
L7	**VSSI**	Power	Ground						
L8	**VDDI**	Power	Digital Supply						
L9	**VSSI**	Power	Ground						
L10	**VDDI**	Power	Digital Supply						
L11	**VSSI**	Power	Ground						
L12	**SSI0EN1**	GPIO	CMOS	ssi0_en1	norspi_ en[1]				39
L13	**SSI0EN0**	GPIO	CMOS	ssi0_en0	norspi_ en[0]	uart2_ahb_ rts_n	ssis_en		38
L14	**SSI0MOSI**	GPIO	CMOS	ssi0_txd	norspi_ dq[0]	uart2_ ahb_tx	ssis_rxd		36
L15	**SSI0MISO**	GPIO	CMOS	ssi0_rxd	norspi_ dq[1]	uart2_ahb_ cts_n	ssis_txd		37
L16	**SSI0CLK**	GPIO	CMOS	ssi0clk	norspi_clk	uart2_ ahb_rx	ssis_clk		35
M1	**DDR_DQ_11**	DDR	SSTL						
M2	**DDR_DQ_5**	DDR	SSTL						
M3	**DDR_DQ_9**	DDR	SSTL						
M4	**DDR_VDDQ**	DDR	SSTL						
M5	**VSSI**	Power	Ground						
M6	**VDDI**	Power	Digital Supply						
M7	**VSSI**	Power	Ground						
M8	**VD0_CLK**	VOUT	CMOS	vd0_clk					134
M9	**ENET_MDIO**	ENET	CMOS	enet_mdio		enet_mdio			67
M10	**TEST_MODE**	GLOB-AL	CMOS						
M11	**CLK_AU**	GPI	CMOS	clk_au	clk_au3				55
M12	**GPIO_2**	GPIO	CMOS	ehci_app_ prt_ovcurr1	uart2_ahb_ tx	ssis_rxd	sc_c1		2
M13	**GPIO_1**	GPIO	CMOS	ehci_app_ prt_ovcurr0	uart2_ahb_ rx	ssis_sclk	sc_c0		1
M14	**GPIO_0**	GPIO	CMOS	sd_hs_sel					0
M15	**UART0TX**	GPIO	CMOS	uart0tx	uart2_ahb_ tx				46
M16	**UART0RX**	GPIO	CMOS	uart0rx	uart2_ahb_ rx				45
N1	**DDR_DQ_3**	DDR	SSTL						
N2	**DDR_DQ_7**	DDR	SSTL						
N3	**DDR_DQS_0**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
N4	**VD0_OUT_3**	VOUT	CMOS	vd0_out[3]					121
N5	**VD0_OUT_2**	VOUT	CMOS	vd0_out[2]					120
N6	**VD0_OUT_12**	VOUT	CMOS	vd0_out[12]					130
N7	**VD0_OUT_11**	VOUT	CMOS	vd0_out[11]					129
N8	**VD0_OUT_8**	VOUT	CMOS	vd0_out[8]					126
N9	**ENET_MDC**	ENET	CMOS	enet_mdc		enet_mdc			66
N10	**ENET_TXD_3**	ENET	CMOS		sc_b0	enet_txd_3	ssi1_en3		60
N11	**ENET_CLK_TX**	ENET	CMOS	enet_2nd_ref_clk		enet_clk_tx			68
N12	**ENET_RXDV**	ENET	CMOS	enet_rxdv		enet_rxdv			65
N13	**IDCCLK**	IDC	CMOS	idc0clk					28
N14	**GPIO_6**	GPIO	CMOS	pwm_2	idsp_pip_iopad_master_vsync	vin_strig1	sc_d1	uart2_ahb_rts_n	6
N15	**GPIO_5**	GPIO	CMOS	pwm_1	idsp_pip_iopad_master_hsync	vin_strig0	sc_d0	uart2_ahb_cts_n	5
N16	**GPIO_3**	GPIO	CMOS	ehci_prt_pwr_0	uart2_ahb_cts_n	ssis_txd	sc_c2		3
P1	**DDR_DQ_1**	DDR	SSTL						
P2	**DDR_DM_0**	DDR	SSTL						
P3	**DDR_DQS_BAR_0**	DDR	SSTL						
P4	**VD0_OUT_4**	VOUT	CMOS	vd0_out[4]					122
P5	**VDDO**	Power	IO Power						
P6	**VD0_OUT_13**	VOUT	CMOS	vd0_out[13]					131
P7	**VD0_OUT_10**	VOUT	CMOS	vd0_out[10]					128
P8	**VDDP**	Power	Pre-driver Supply						
P9	**VDDO**	Power	IO Power						
P10	**ENET_TXD_2**	ENET	CMOS		sc_a3	enet_txd_2	ssi1_en2		59
P11	**ENET_RXD_3**	ENET	CMOS			enet_rxd_3		norspi_dq[3]	64
P12	**ENET_EXT_OSC_CLK**	ENET	CMOS			enet_ext_osc_clk			71
P13	**IDCDATA**	IDC	CMOS	idc0data					29
P14	**IDC3CLK**	IDC	CMOS	idc2clk	vin_strig0				32
P15	**IDC3DATA**	IDC	CMOS	idc2data	vin_strg1				33
P16	**JTAG_TDI**	JTAG	CMOS						
R1	**DDR_DQ_0**	DDR	SSTL						
R2	**DDR_DQ_2**	DDR	SSTL						
R3	**VD_PWM**	VOUT	CMOS	pwm_0					138
R4	**VD0_OUT_5**	VOUT	CMOS	vd0_out[5]					123
R5	**VD0_OUT_1**	VOUT	CMOS	vd0_out[1]					119
R6	**VD0_OUT_14**	VOUT	CMOS	vd0_out[14]					132

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
R7	**VD0_OUT_9**	VOUT	CMOS	vd0_out[9]					127
R8	**VD0_HVLD**	IDC	CMOS	vd0_hvld					137
R9	**ENET_GTX_CLK**	ENET	CMOS	enet_gtx_clk		enet_gtx_clk	ssi1_sclk	norspi_clk	70
R10	**ENET_TXD_1**	ENET	CMOS	enet_txd_1	sc_a2	enet_txd_1	ssi1_en1	norspi_en[2]	58
R11	**ENET_RXD_2**	ENET	CMOS		sc_b3	enet_rxd_2		norspi_dq[2]	63
R12	**ENET_CLK_RX**	ENET	CMOS	enet_ref_clk		enet_clk_rx			69
R13	**JTAG_RST_L**	JTAG	CMOS						
R14	**JTAG_TDO**	JTAG	CMOS						
R15	**JTAG_CLK**	JTAG	CMOS						
R16	**JTAG_TMS**	JTAG	CMOS						
T1	**DDR_DQ_4**	DDR	SSTL						
T2	**DDR_DQ_6**	DDR	SSTL						
T3	**VD0_OUT_7**	VOUT	CMOS	vd0_out[7]					125
T4	**VD0_OUT_6**	VOUT	CMOS	vd0_out[6]					124
T5	**VD0_OUT_0**	VOUT	CMOS	vd0_out[0]					118
T6	**VD0_OUT_15**	VOUT	CMOS	vd0_out[15]					133
T7	**VD0_HSYNC**	VOUT	CMOS	vd0_hsync					136
T8	**VD0_VSYNC**	VOUT	CMOS	vd0_vsync					135
T9	**ENET_TXEN**	ENET	CMOS	enet_txen	sc_a0	enet_txen	ssi1_txd	norspi_en[0]	56
T10	**ENET_TXD_0**	ENET	CMOS	enet_txd_0	sc_a1	enet_txd_0	ssi1_en0	norspi_en[1]	57
T11	**ENET_RXD_1**	ENET	CMOS	enet_rxd_1	sc_b2	enet_rxd_1		norspi_dq[1]	62
T12	**ENET_RXD_0**	ENET	CMOS	enet_rxd_0	sc_b1	enet_rxd_0	ssi1_rxd	norspi_dq[0]	61
T13	**I2S_SO**	I2S	CMOS	i2s_so					53
T14	**I2S_SI**	I2S	CMOS	i2s_si	dmic_DAT				52
T15	**I2S_WS**	I2S	CMOS	i2s_ws					54
T16	**I2S_CLK**	I2S	CMOS	i2s_clk	dmic_clk				51

Table 7-1. Pin List and Mapping Table for the S5L33M Chip.

8. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance. Conventions include:

Example	Description
AmbaGuiGen, **DirectUSB** **Save**, **File > Save** **Power**, **Reset**, **Home**	Software names GUI commands and command sequences Computer / hardware buttons
Flash_IO_control **da**, **status**, **enable**	Register names and register fields. For example, **Flash_IO_control** is the register for global control of Flash I/O, and bit 17 (**da)** is used for DMA acknowledgement.
GPIO81, **CLK_AU**	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t **amb_operating_mode_t** **amb_set_operating_mode()**	API details (e.g., functions, structures, and type definitions)
`/usr/local/bin` `success = amb_set_operating_mode (amb_xx_base_address, &operating_mode)`	User entries into software dialogues and GUI windows File names and paths Command line scripting and code

Table 8-1. Typographical Conventions for Technical Documents.

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

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10. REVISION HISTORY

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NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	30 May 2017	New S5LM Part
0.2	7 September 2017	Updated Table 4-2 Power Rails: DC Characteristics : Changed VDDI value to 0.7V Updated Figure 1-1 S5L33M Overview: Functional Block Diagram of the S5L33M SoC. Updated Table 2-6: S5L33M SSI / SPI Master with Device Enable Detail: Removed SSI2 Updated Table 4-13 Fail-Safe Pins: Removed UART1 pins Updated Section 1.2: Modified i2c/idc, uart interface and ADC values Updated 240 MPixel/s input pixel rate to 120 MPixel/s input pixel rate Updated H.264 / H.265 encode performance to 2Mp30
0.3	8 August 2018	Updated Table 4-3 Digital I/O Characteristics @ VDDO 3.0V: Table title modified to VDDO at 3.0V Added Table 4-4: Digital I/O Characteristics @ VDDO 1.8V Deleted Section 3.2.14 PWC and RTC Pins Updated Table 3-15 RTC Interface Pins: Updated PWC_AVDD18 to Power Updated SD1 to support UHS-I Added VIH and VIL for XI_RTC to Table 4-7 PWC and RTC Supply Updated Section 4.4 Fail-Safe Pins Updated DVDD spec
0.4	22 August 2018	Updated to support for only 3 PWM
0.5	12 November 2018	Updated Section 1.2 Feature List: Changed GPIO pins from 93 to 94 Updated Table 3-13 General Purpose Input Output (GPIO) Multifunction-Capable Pins: Added SMIO_31 (GPIO 104) Updated Table 4-9 Video DAC Electrical Specification Updated Table 4-10 ADC DC Specification
0.6	15 May 2019	Updated Chapter 7 Pin List - CLK_AU changed to GPI from GPIO Updated Section 2.11 I2C / IDC Interface to change protocol speed Updated Table 4-18 SD Controller Timing Parameters Updated Section 1.2 Feature List - removed "Two clocking options (PLL-generated gclk _vin or SLVS bit clock)"
0.7	18 July 2019	Updated processing rate to 320 MPixels/s Updated to six encode streams in Section 1.2 Feature List

Version	Date	Comments
0.8	9 September 2019	Updated Table 4-5 DC Supply Voltage Levels (Preliminary) Updated Table 4-6 SSTL I/O DC Specifications (Preliminary) Updated Table 4-2 DC Characteristics to add MIPI_AVDD18_IO Updated Figure 1-1 Functional Block Diagram Deleted Section 3.2.16 PWM Removed references to Micro Stepper Updated Section 1.2 Feature list to reflect correct details on VIN, GPIO, ADC, IDC, SPI devices Updated Chapter 2 Interfaces to reflect correct number of interfaces
0.9	6 April 2021	Updated Section 2.11 I2C / IDC Interface Updated Section 2.15 RTC Interface Updated Section 4.6 Electrical: SD Controller Timing for timing diagrams and tables Removed SPI-EEPROM Updated package type to FC TFBGA

Table 10-1. Revision History.