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This sensor is designed for use in

Consumer use digital still camera

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SONY

Diagonal 28.3 mm (Type 1.8) CMOS Image Sensor with Square Pixel for Color Cameras

IMX571BQR-C

Description

The IMX571BQR-C is a diagonal 28.3 mm (Type 1.8) CMOS active pixel type image sensor with a square pixel array and 26.11 M effective pixels. This sensor incorporates maximum 36 dB PGA circuit and 16-bit A/D converter. 16-bit digital output makes it possible to readout the signals of 26.11 M effective pixels at high-speed of 6.84 frame/s in still picture mode. In addition, it realizes 12-bit digital output for high-speed 4K moving picture by window readout mode. This sensor is designed for use in consumer use digital still camera. When using this for another application, Sony Semiconductor Solutions Corporation does not guarantee the quality and reliability of this product. Therefore, don't use this for applications other than consumer use digital still camera.
In addition, individual specification change cannot be supported because this is a standard product.
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Features

- ◆ APS size CMOS active pixel type dots
- ◆ Input clock frequency 72 MHz
- ◆ All-pixel readout mode
  All-pixel readout mode / 2-parallel ADC readout
  All-pixel readout mode / digital overlap drive
  Vertical 2/2-line and horizontal 2/2-line weighted binning readout mode
  Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/3-line binning, horizontal 3 weighted binning readout mode
  Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode / digital overlap drive
  Vertical 3/3-line binning, horizontal 3 weighted binning readout mode / digital overlap drive
  Vertical 1/5 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/5 subsampling binning, horizontal 3 weighted binning readout mode
  Vertical 1/7 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/7 subsampling binning, horizontal 3 weighted binning readout mode
  Vertical 1/9 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/9 subsampling binning, horizontal 3 weighted binning readout mode
  Vertical 1/13 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/13 subsampling binning, horizontal 3 weighted binning readout mode
  Vertical 1/25 subsampling, horizontal 3 weighted binning readout mode
  Vertical 3/25 subsampling binning, horizontal 3 weighted binning readout mode
- ◆ Rolling shutter function moving picture mode
- ◆ H driver, V driver and serial communication circuit on chip
- ◆ +36dB gain in CDS/PGA on chip (when A/D 16-bit, 14-bit, 12-bit)
- ◆ Built-in 11-bit/12-bit/14-bit/16-bit A/D converter
- ◆ 8 Lane SLVS-EC output
- ◆ R, G, B primary color mosaic filter on chip
- ◆ Back-illuminated type

E18Z05B97

Device Structure

◆ CMOS image sensor	
◆ Image size	Diagonal 28.3 mm (Type 1.8)
◆ Total number of pixels	6280 (H) × 4264 (V)　approx. 26.78 M pixels
◆ Number of effective pixels	6252 (H) × 4176 (V)　approx. 26.11 M pixels
◆ Number of active pixels	6244 (H) × 4168 (V)　approx. 26.02 M pixels
◆ Chip size	27.780 mm (H) × 22.302 mm (V)
◆ Unit cell size	3.76 µm (H) × 3.76 µm (V)
◆ Optical black	Horizontal (H) direction: Front 16 pixels, Rear 0 pixel Vertical (V) direction: Front 22 pixels, Rear 0 pixel
◆ Substrate material	Silicon

Physical Pixel Array and Pixel Address Definition

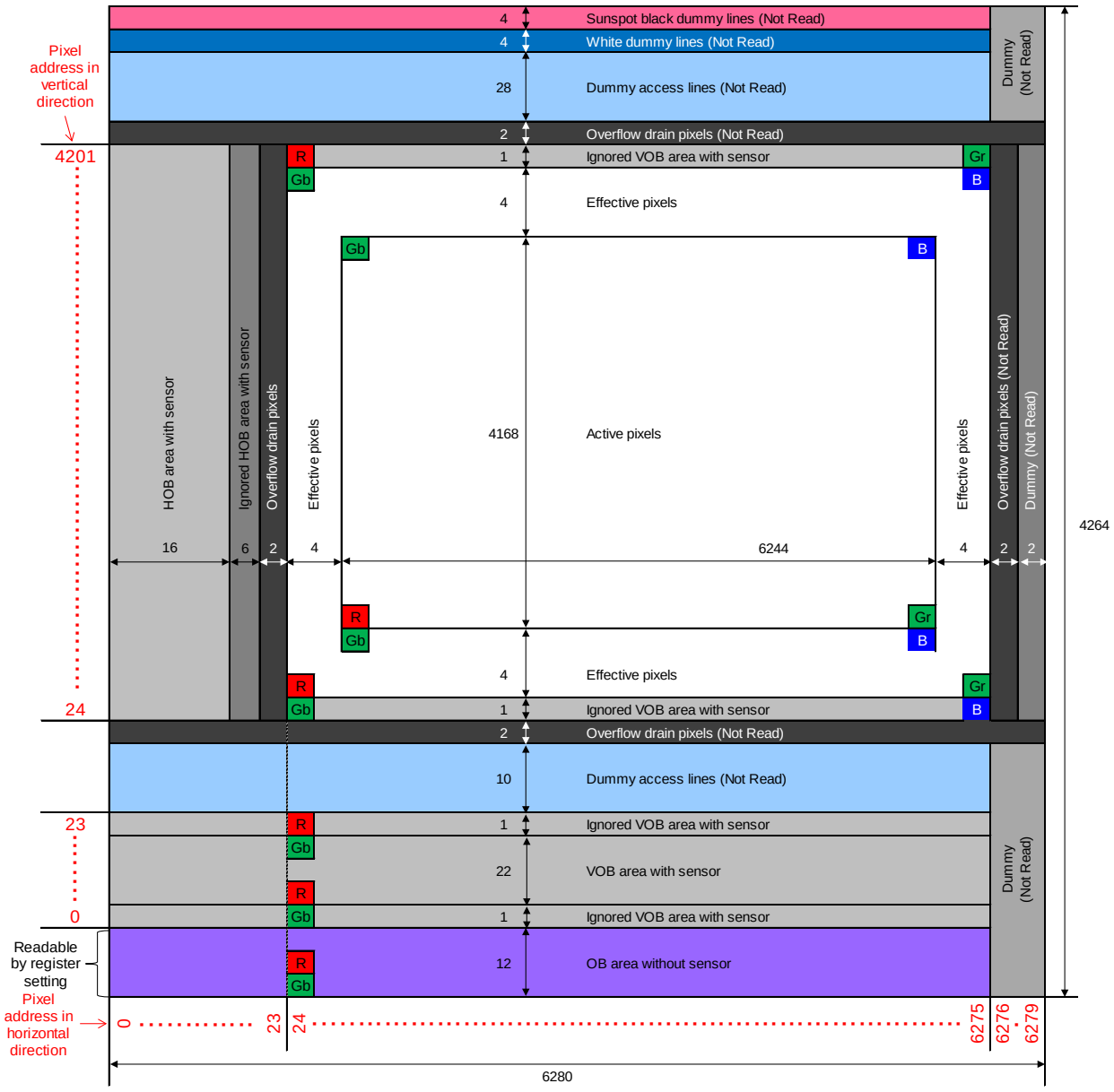

Fig. Physical Pixel Array and Pixel Address Definition (Top View)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}SUB, V_{DD}HPX, V_{DD}HVD	V_{SS}HPX −0.5 to 6.3	V	—
	V_{DD}HVS	V_{SS}HPX −0.5 to 6.3	V	—
	V_{DD}MPX	V_{SS}HPX −0.3 to 2.5	V	—
	V_{DD}LPLA	V_{SS}LPLA −0.3 to 2.0	V	—
	V_{DD}LPLD	V_{SS}LPLD −0.3 to 2.0	V	—
	V_{DD}HCM	V_{SS}HCM −0.5 to 6.3	V	—
	V_{DD}HDA	V_{SS}HDA −0.5 to 6.3	V	—
	V_{DD}HAN	V_{SS}HAN −0.5 to 6.3	V	—
	V_{DD}LCB	V_{SS}LCB −0.3 to 2.0	V	—
	V_{DD}LCN	V_{SS}LCN −0.3 to 2.0	V	—
	V_{DD}MIO	V_{SS}LSC −0.3 to 2.5	V	—
	V_{DD}LSC	V_{SS}LSC −0.3 to 2.0	V	—
	V_{DD}LIF	V_{SS}LIF −0.3 to 2.0	V	—
	VRLT	V_{DD}HVS −6.3 to V_{SS}HPX + 0.5	V	—
	VRLS	V_{DD}HVS −6.3 to V_{SS}HPX + 0.5	V	—
	VRM	V_{SS}HPX −0.5 to 6.3	V	—
	VRML	V_{DD}HVS −6.3 to V_{SS}HPX + 0.5	V	—
Input voltage (digital)	INCK	V_{SS}LPLD −0.3 to V_{DD}MIO + 0.3	V	—
	XCLR, XVS, XHS, XPI, SCK, SDI, XCE	V_{SS}LSC −0.3 to V_{DD}MIO + 0.3	V	—
Output voltage (digital)	SDO	V_{SS}LSC −0.3 to V_{DD}MIO + 0.3	V	—
	DOP0 to DOP7, DOM0 to DOM7	V_{SS}LIF −0.3 to V_{DD}LIF + 0.3	V	SLVS-EC
Analog	TAMON1, TAMON2, TAMON3, TAMON4, VLOADLM1, VLOADLM2 VLOADCMSF1, VLOADCMSF2	V_{SS}HPX −0.3 to V_{DD}HPX + 0.3	V	—
	BIASRESBC1, BIASRESBC2, VBGR1, VBGR2	V_{SS}HAN −0.3 to V_{DD}HAN + 0.3	V	—
	VLOADCM1, VLOADCM2,	V_{SS}HCM −0.3 to V_{DD}HCM + 0.3	V	—
Guaranteed operating temperature		–10 to +75	˚C	—
Storage guarantee temperature		–30 to +80	˚C	—
Performance guarantee temperature		–10 to +60	˚C	—

Recommended Operating Conditions

Item	Symbol	Value	Unit	Remarks
Supply voltage	V_{DD}SUB	4.5	V	Substrate potential
	V_{DD}HPX	4.6	V	Pixel power supply
		1.8	V	Pixel power supply only when using sleep setting during long time exposure mode
	V_{SS}HPX	0.0	V	Pixel GND
	V_{DD}HVD	4.6	V	Pixel power supply
	V_{DD}HVS	4.25	V	Positive power supply for pixel drive
	V_{DD}MPX	1.8	V	Pixel power supply (for long time storage)
	V_{DD}LPLA	1.2	V	PLL power supply (Analog)
	V_{SS}LPLA	0.0	V	PLL GND (Analog)
	V_{DD}LPLD	1.2	V	PLL power supply (Logic)
	V_{SS}LPLD	0.0	V	PLL GND (Logic)
	V_{DD}HCM	4.0	V	Comparator power supply
	V_{SS}HCM	0.0	V	Comparator GND
	V_{DD}HDA	4.2	V	DAC power supply
	V_{SS}HDA	0.0	V	DAC GND
	V_{DD}HAN	4.5	V	DAC power supply
	V_{SS}HAN	0.0	V	DAC GND
	V_{DD}LCB	1.2	V	Comparator buffer power supply
	V_{SS}LCB	0.0	V	Comparator buffer GND
	V_{DD}LCN	1.2	V	Counter power supply
	V_{SS}LCN	0.0	V	Counter GND
	V_{DD}MIO	1.8	V	Digital I/O power supply
	V_{DD}LSC	1.2	V	Digital power supply
	V_{SS}LSC	0.0	V	Digital I/O GND
	V_{DD}LIF	1.2	V	SLVS-EC power supply
	V_{SS}LIF	0.0	V	SLVS-EC GND
	VRLT	-1.2	V	Negative power supply for pixel drive
	VRLS	-1.2	V	Negative power supply for pixel drive
	VRM	2.2	V	Middle voltage supply for pixel drive
	VRML	0.0	V	Middle voltage supply for pixel drive

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Contents

Optical Center

(Unit: mm)

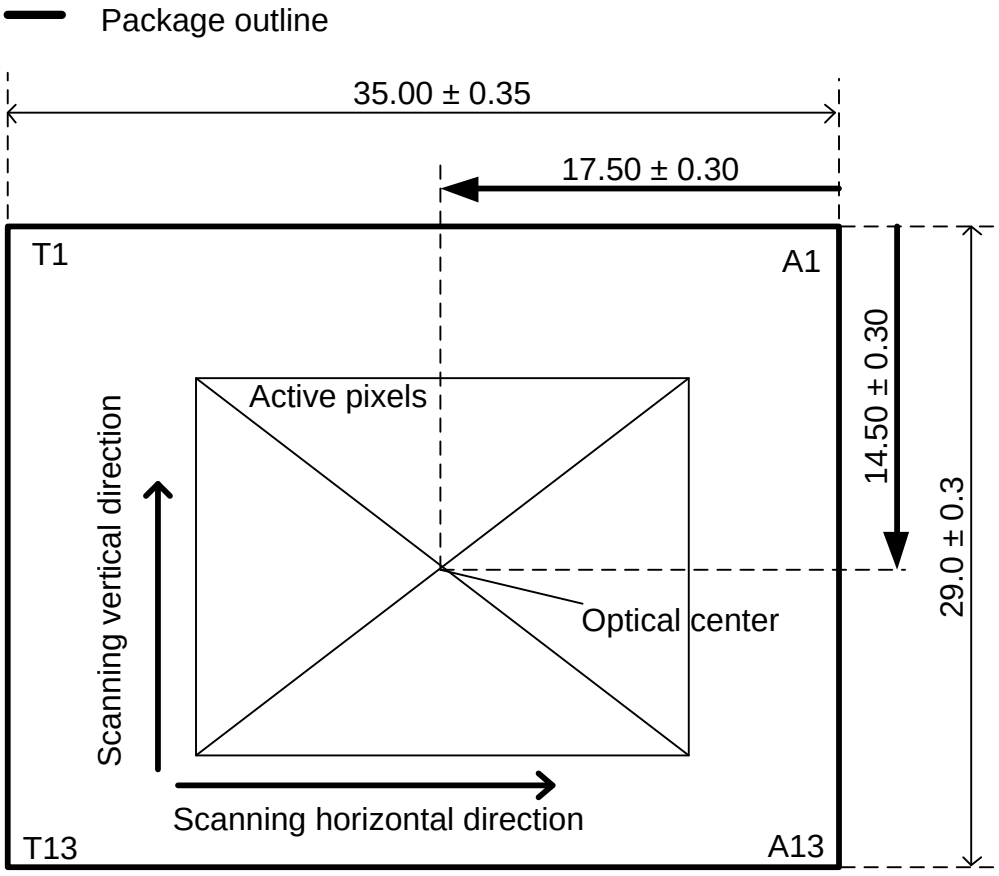


Fig. Optical Center (Top View)

Block Diagram and Pin Configuration

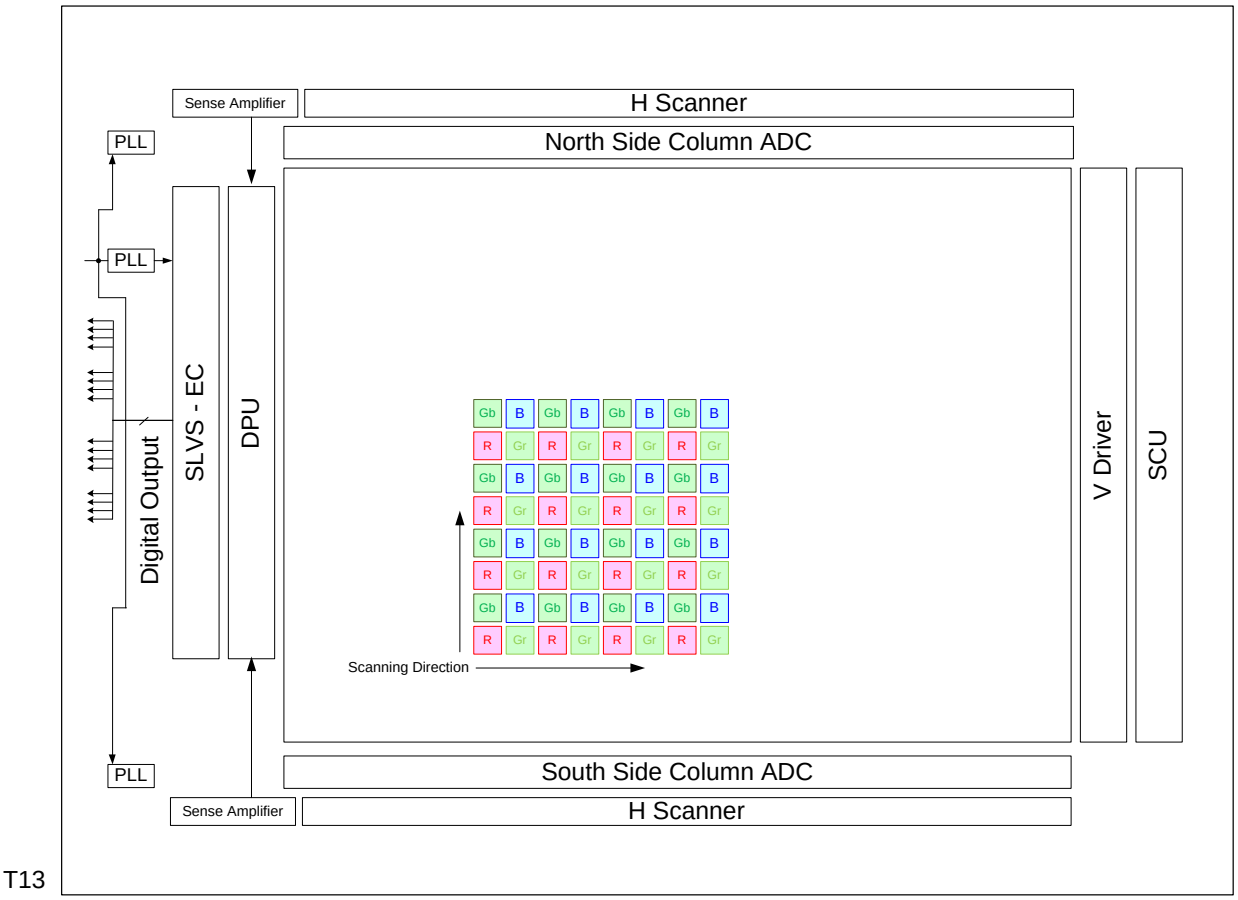


Fig. Block Diagram (Top View)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1		INCK	V_{SS}LSC	V_{DD}LSC	V_{DD}LSC	V_{SS}LSC	V_{DD}LCN_N	V_{SS}LCN_N	TSCANEN	TOUT	V_{SS}LCN_N	V_{DD}LCN_N	V_{DD}LCN_N	V_{SS}LCN_N	V_{DD}MIO1		1
2	V_{DD}LPLA1	V_{SS}LPLA1	V_{SS}LPLD1	NC_K2	NC_K2	NC_K2	NC_K2	NC_J2	TENABLE	NC_D2	NC_D2	NC_D2	NC_D2	XCLR	V_{SS}LSC	V_{DD}LSC	2
3	V_{DD}LIF	V_{SS}LIF	V_{DD}LPLD1	NC_N3	BIASRESBC1	VBGR1	V_{SS}HPX	V_{SS}HPX	V_{SS}LCB_N	V_{SS}HCM_N	V_{SS}LCB_N	V_{SS}HCM_N	V_{DD}HCM_N	NC_C3	VLOADCM1	VLOADLM2	3
4	DOM0	DOP0	V_{DD}LPLD2	NC_N3	TAMON2	TAMON1	V_{DD}HPX	V_{DD}MPX	V_{DD}LCB_N	V_{DD}HCM_N	V_{DD}LCB_N	V_{SS}HPX	V_{DD}HPX	NC_C4	TVDSUN2	TVCDSIND2	4
5	DOM1	DOP1	V_{SS}LPLD2	NC_N3	V_{SS}HAN_N	V_{DD}HAN_N					V_{DD}MPX	V_{SS}HPX	V_{DD}HVD	NC_C4	VLOADCMSF2	SCK	5
6	DOM2	DOP2	V_{DD}MIO2	NC_N3	V_{SS}HDA1	V_{DD}HDA1					NC_C4	V_{SS}HPX	VRLS	NC_C4	XCE	SDI	6
7	DOM3	DOP3	V_{DD}LPLA2	NC_N7	V_{SS}HPX	V_{DD}SUB			Top View		V_{DD}SUB	V_{SS}HPX	VRLT	NC_C7	V_{SS}LSC	SDO	7
8	DOM4	DOP4	V_{SS}LPLA2	NC_N7	V_{SS}HDA2	V_{DD}HDA2					V_{DD}HVS	V_{SS}HPX	VRML	NC_C7	XVS	XHS	8
9	DOM5	DOP5	V_{DD}LPLD3	NC_N7	V_{SS}HAN_S	V_{DD}HAN_S					V_{DD}MPX	V_{SS}HPX	VRM	NC_C7	VLOADCMSF1	XPI	9
10	DOM6	DOP6	V_{SS}LPLD3	NC_N7	TAMON3	TAMON4	V_{DD}HPX	V_{DD}MPX	V_{DD}LCB_S	V_{DD}HCM_S	V_{DD}LCB_S	V_{SS}HPX	V_{DD}HPX	NC_C7	TVDSUN1	TVCDSIND1	10
11	DOM7	DOP7	V_{DD}LPLA3	NC_N7	BIASRESBC2	VBGR2	V_{SS}HPX	V_{SS}HPX	V_{SS}LCB_S	V_{SS}HCM_S	V_{SS}LCB_S	V_{SS}HCM_S	V_{DD}HCM_S	NC_C11	VLOADCM2	VLOADLM1	11
12	V_{DD}LIF	V_{SS}LIF	V_{SS}LPLA3	NC_J12	NC_J12	NC_J12	NC_J12	NC_J12	TI_DGTOP0	NC_C11	NC_C11	NC_C11	NC_C11	NC_C11	V_{SS}LSC	V_{DD}LSC	12
13		NC_R13	V_{SS}LSC	V_{DD}LSC	V_{DD}LSC	V_{SS}LSC	V_{DD}LCN_S	V_{SS}LCN_S	TI_DGTOP1	TOUT_DGTOP	V_{SS}LCN_S	V_{DD}LCN_S	V_{DD}LCN_S	V_{SS}LCN_S	NC_B13		13
	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Fig. Pin Configuration (Top View)

Pin Description

Package Pin No.		Symbol	Input/ Output	Analog/ Digital	Function
A	2	V_{DD}LSC	Power	D	Digital power supply
A	3	VLOADLM2	O	A	Leave open.(No Connection)
A	4	TVCDSIND2	I	A	Leave open.(No Connection)
A	5	SCK	I	D	Serial communication clock input
A	6	SDI	I	D	Serial communication data input
A	7	SDO	O	D	Leave open.(No Connection)
A	8	XHS	I	D	H sync signal
A	9	XPI	I	D	Non-linear electronic shutter timing input
A	10	TVCDSIND1	I	A	Leave open.(No Connection)
A	11	VLOADLM1	O	A	Leave open.(No Connection)
A	12	V_{DD}LSC	Power	D	Digital power supply
B	1	V_{DD}MIO1	Power	D	Digital I/O power supply
B	2	V_{SS}LSC	GND	D	Digital I/O GND
B	3	VLOADCM1	O	A	Leave open.(No Connection)
B	4	TVDSUN2	I	A	Leave open.(No Connection)
B	5	VLOADCMSF2	O	A	Internal circuit decoupling
B	6	XCE	I	D	Serial communication enable
B	7	V_{SS}LSC	GND	D	Digital I/O GND
B	8	XVS	I	D	V sync signal
B	9	VLOADCMSF1	O	A	Internal circuit decoupling
B	10	TVDSUN1	I	A	Leave open.(No Connection)
B	11	VLOADCM2	O	A	Leave open.(No Connection)
B	12	V_{SS}LSC	GND	D	Digital I/O GND
B	13	NC_B13	–	–	N.C.
C	1	V_{SS}LCN_N	GND	D	Counter GND
C	2	XCLR	I	D	Chip reset
C	3	NC_C3	–	–	N.C.
C	4	NC_C4	–	–	N.C.
C	5	NC_C4	–	–	N.C.
C	6	NC_C4	–	–	N.C.
C	7	NC_C7	–	–	N.C.
C	8	NC_C7	–	–	N.C.
C	9	NC_C7	–	–	N.C.

Package Pin No.		Symbol	Input/ Output	Analog/ Digital	Function
C	10	NC_C7	–	–	N.C.
C	11	NC_C11	–	–	N.C.
C	12	NC_C11	–	–	N.C.
C	13	V_{SS}LCN_S	GND	D	Counter GND
D	1	V_{DD}LCN_N	Power	D	Counter power supply
D	2	NC_D2	–	–	N.C.
D	3	V_{DD}HCM_N	Power	A	Comparator power supply
D	4	V_{DD}HPX	Power	A	Pixel power supply
D	5	V_{DD}HVD	Power	A	Pixel power supply
D	6	VRLS	Power	A	Negative power supply for pixel drive
D	7	VRLT	Power	A	Negative power supply for pixel drive
D	8	VRML	GND	A	Middle voltage supply for pixel drive
D	9	VRM	Power	A	Middle voltage supply for pixel drive
D	10	V_{DD}HPX	Power	A	Pixel power supply
D	11	V_{DD}HCM_S	Power	A	Comparator power supply
D	12	NC_C11	–	–	N.C.
D	13	V_{DD}LCN_S	Power	D	Counter power supply
E	1	V_{DD}LCN_N	Power	D	Counter power supply
E	2	NC_D2	–	–	N.C.
E	3	V_{SS}HCM_N	GND	A	Comparator GND
E	4	V_{SS}HPX	GND	A	Pixel GND
E	5	V_{SS}HPX	GND	A	Pixel GND
E	6	V_{SS}HPX	GND	A	Pixel GND
E	7	V_{SS}HPX	GND	A	Pixel GND
E	8	V_{SS}HPX	GND	A	Pixel GND
E	9	V_{SS}HPX	GND	A	Pixel GND
E	10	V_{SS}HPX	GND	A	Pixel GND
E	11	V_{SS}HCM_S	GND	A	Comparator GND
E	12	NC_C11	–	–	N.C.
E	13	V_{DD}LCN_S	Power	D	Counter power supply
F	1	V_{SS}LCN_N	GND	D	Counter GND
F	2	NC_D2	–	–	N.C.
F	3	V_{SS}LCB_N	GND	A	Comparator buffer GND
F	4	V_{DD}LCB_N	Power	A	Comparator buffer power supply
F	5	V_{DD}MPX	Power	A	Pixel power supply (for long time storage)

Package Pin No.		Symbol	Input/ Output	Analog/ Digital	Function
F	6	NC_C4	–	–	N.C.
F	7	V_{DD}SUB	Power	A	Substrate potential
F	8	V_{DD}HVS	Power	A	Positive power supply for pixel drive
F	9	V_{DD}MPX	Power	A	Pixel power supply (for long time storage)
F	10	V_{DD}LCB_S	Power	A	Comparator buffer power supply
F	11	V_{SS}LCB_S	GND	A	Comparator buffer GND
F	12	NC_C11	–	–	N.C.
F	13	V_{SS}LCN_S	GND	D	Counter GND
G	1	TOUT	O	D	Leave open.(No Connection)
G	2	NC_D2	–	–	N.C.
G	3	V_{SS}HCM_N	GND	A	Comparator GND
G	4	V_{DD}HCM_N	Power	A	Comparator power supply
G	10	V_{DD}HCM_S	Power	A	Comparator power supply
G	11	V_{SS}HCM_S	GND	A	Comparator GND
G	12	NC_C11	–	–	N.C.
G	13	TOUT_DGTOP	O	D	Leave open.(No Connection)
H	1	TSCANEN	I	D	Leave open.(No Connection)
H	2	TENABLE	I	D	Leave open.(No Connection)
H	3	V_{SS}LCB_N	GND	A	Comparator buffer GND
H	4	V_{DD}LCB_N	Power	A	Comparator buffer power supply
H	10	V_{DD}LCB_S	Power	A	Comparator buffer power supply
H	11	V_{SS}LCB_S	GND	A	Comparator buffer GND
H	12	TI_DGTOP0	I	D	Leave open.(No Connection)
H	13	TI_DGTOP1	I	D	Leave open.(No Connection)
J	1	V_{SS}LCN_N	GND	D	Counter GND
J	2	NC_J2	–	–	N.C.
J	3	V_{SS}HPX	GND	A	Pixel GND
J	4	V_{DD}MPX	Power	A	Pixel power supply (for long time storage)
J	10	V_{DD}MPX	Power	A	Pixel power supply (for long time storage)
J	11	V_{SS}HPX	GND	A	Pixel GND
J	12	NC_J12	–	–	N.C.
J	13	V_{SS}LCN_S	GND	D	Counter GND
K	1	V_{DD}LCN_N	Power	D	Counter power supply
K	2	NC_K2	–	–	N.C.
K	3	V_{SS}HPX	GND	A	Pixel GND

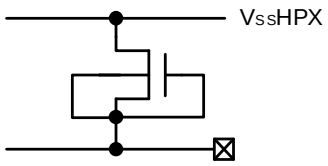
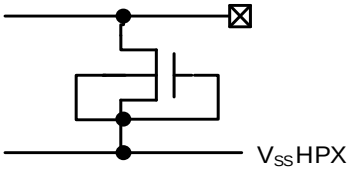
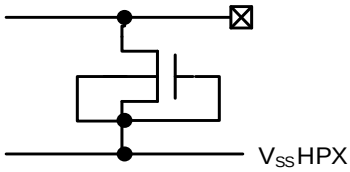
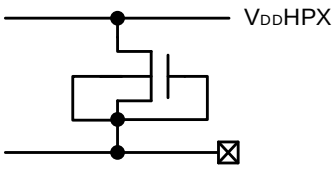
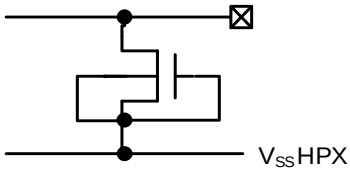
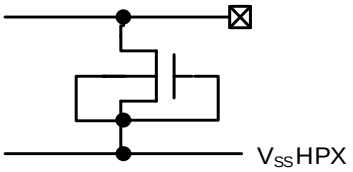
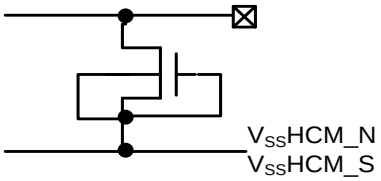
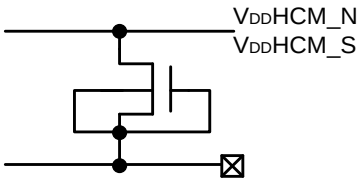
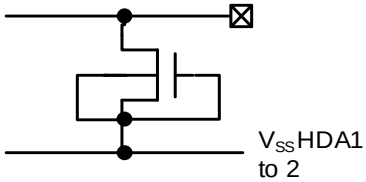
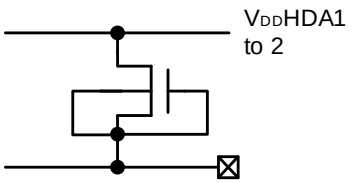
Package Pin No.		Symbol	Input/ Output	Analog/ Digital	Function
K	4	V_{DD}HPX	Power	A	Pixel power supply
K	10	V_{DD}HPX	Power	A	Pixel power supply
K	11	V_{SS}HPX	GND	A	Pixel GND
K	12	NC_J12	–	–	N.C.
K	13	V_{DD}LCN_S	Power	D	Counter power supply
L	1	V_{SS}LSC	GND	D	Digital I/O GND
L	2	NC_K2	–	–	N.C.
L	3	VBGR1	O	A	Internal circuit decoupling
L	4	TAMON1	O	A	Leave open.(No Connection)
L	5	V_{DD}HAN_N	Power	A	DAC power supply
L	6	V_{DD}HDA1	Power	A	DAC power supply
L	7	V_{DD}SUB	Power	A	Substrate potential
L	8	V_{DD}HDA2	Power	A	DAC power supply
L	9	V_{DD}HAN_S	Power	A	DAC power supply
L	10	TAMON4	O	A	Leave open.(No Connection)
L	11	VBGR2	O	A	Internal circuit decoupling
L	12	NC_J12	–	–	N.C.
L	13	V_{SS}LSC	GND	D	Digital I/O GND
M	1	V_{DD}LSC	Power	D	Digital power supply
M	2	NC_K2	–	–	N.C.
M	3	BIASRESBC1	O	A	Reference current input for Column ADC
M	4	TAMON2	O	A	Leave open.(No Connection)
M	5	V_{SS}HAN_N	GND	A	DAC GND
M	6	V_{SS}HDA1	GND	A	DAC GND
M	7	V_{SS}HPX	GND	A	Pixel GND
M	8	V_{SS}HDA2	GND	A	DAC GND
M	9	V_{SS}HAN_S	GND	A	DAC GND
M	10	TAMON3	O	A	Leave open.(No Connection)
M	11	BIASRESBC2	O	A	Reference current input for Column ADC
M	12	NC_J12	–	–	N.C.
M	13	V_{DD}LSC	Power	D	Digital power supply
N	1	V_{DD}LSC	Power	D	Digital power supply
N	2	NC_K2	–	–	N.C.
N	3	NC_N3	–	–	N.C.
N	4	NC_N3	–	–	N.C.

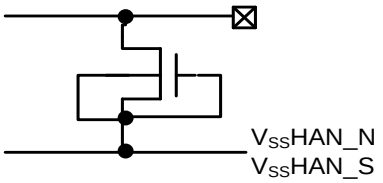
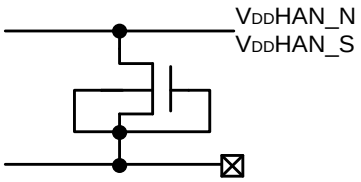
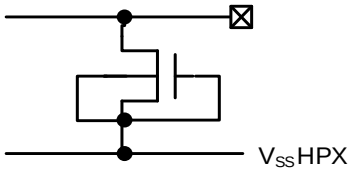
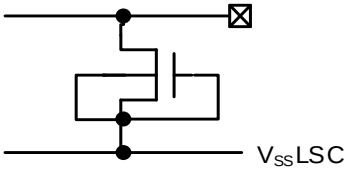
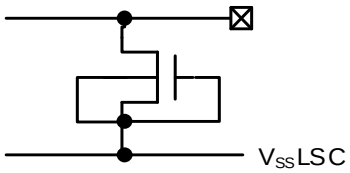
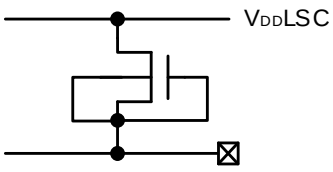
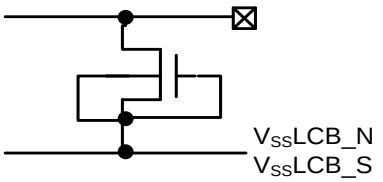
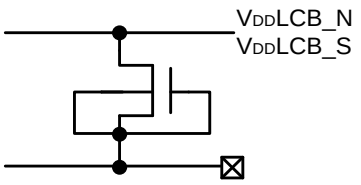
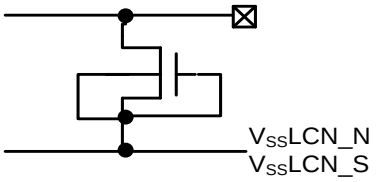
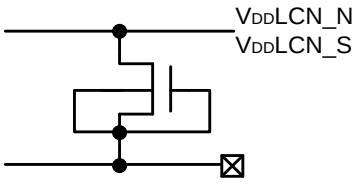
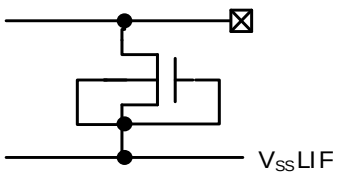
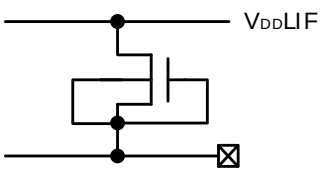
Package Pin No.		Symbol	Input/ Output	Analog/ Digital	Function
N	5	NC_N3	–	–	N.C.
N	6	NC_N3	–	–	N.C.
N	7	NC_N7	–	–	N.C.
N	8	NC_N7	–	–	N.C.
N	9	NC_N7	–	–	N.C.
N	10	NC_N7	–	–	N.C.
N	11	NC_N7	–	–	N.C.
N	12	NC_J12	–	–	N.C.
N	13	V_{DD}LSC	Power	D	Digital power supply
P	1	V_{SS}LSC	GND	D	Digital I/O GND
P	2	V_{SS}LPLD1	GND	D	PLL GND (Logic)
P	3	V_{DD}LPLD1	Power	D	PLL power supply (Logic)
P	4	V_{DD}LPLD2	Power	D	PLL power supply (Logic)
P	5	V_{SS}LPLD2	GND	D	PLL GND (Logic)
P	6	V_{DD}MIO2	Power	D	Digital I/O power supply
P	7	V_{DD}LPLA2	Power	A	PLL power supply (Analog)
P	8	V_{SS}LPLA2	GND	A	PLL GND (Analog)
P	9	V_{DD}LPLD3	Power	D	PLL power supply (Logic)
P	10	V_{SS}LPLD3	GND	D	PLL GND (Logic)
P	11	V_{DD}LPLA3	Power	A	PLL power supply (Analog)
P	12	V_{SS}LPLA3	GND	A	PLL GND (Analog)
P	13	V_{SS}LSC	GND	D	Digital I/O GND
R	1	INCK	I	D	Master clock
R	2	V_{SS}LPLA1	GND	A	PLL GND (Analog)
R	3	V_{SS}LIF	GND	A	SLVS-EC GND
R	4	DOP0	O	D	SLVS-EC output: Plus 0
R	5	DOP1	O	D	SLVS-EC output: Plus 1
R	6	DOP2	O	D	SLVS-EC output: Plus 2
R	7	DOP3	O	D	SLVS-EC output: Plus 3
R	8	DOP4	O	D	SLVS-EC output: Plus 4
R	9	DOP5	O	D	SLVS-EC output: Plus 5
R	10	DOP6	O	D	SLVS-EC output: Plus 6
R	11	DOP7	O	D	SLVS-EC output: Plus 7
R	12	V_{SS}LIF	GND	A	SLVS-EC GND
R	13	NC_R13	–	–	N.C.

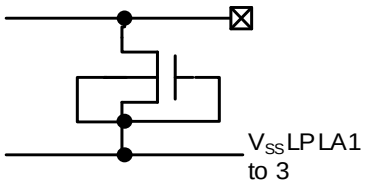
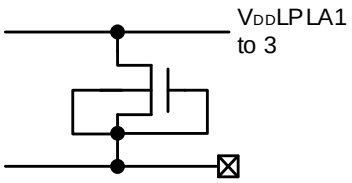
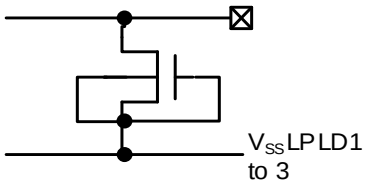
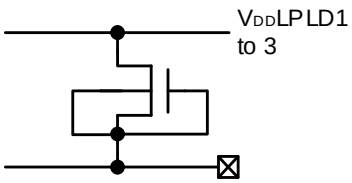
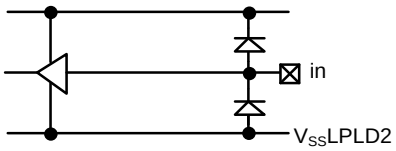
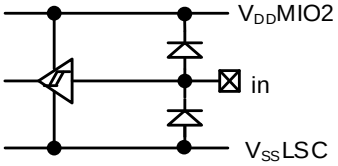
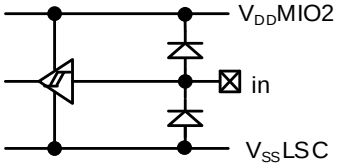
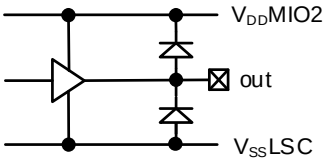
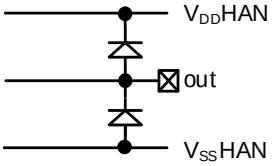
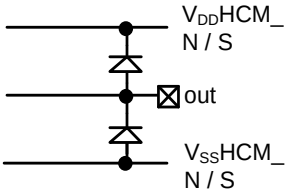
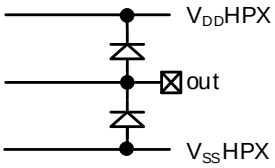
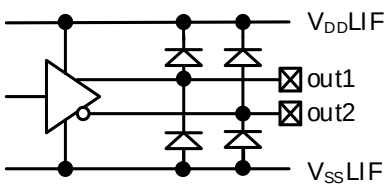
Package	Pin No.	Symbol	Input/ Output	Analog/ Digital	Function
T	2	V_{DD}LPLA1	Power	A	PLL power supply (Analog)
T	3	V_{DD}LIF	Power	A	SLVS-EC power supply
T	4	DOM0	O	D	SLVS-EC output: Minus 0
T	5	DOM1	O	D	SLVS-EC output: Minus 1
T	6	DOM2	O	D	SLVS-EC output: Minus 2
T	7	DOM3	O	D	SLVS-EC output: Minus 3
T	8	DOM4	O	D	SLVS-EC output: Minus 4
T	9	DOM5	O	D	SLVS-EC output: Minus 5
T	10	DOM6	O	D	SLVS-EC output: Minus 6
T	11	DOM7	O	D	SLVS-EC output: Minus 7
T	12	V_{DD}LIF	Power	A	SLVS-EC power supply

I/O Equivalent Circuit Diagram

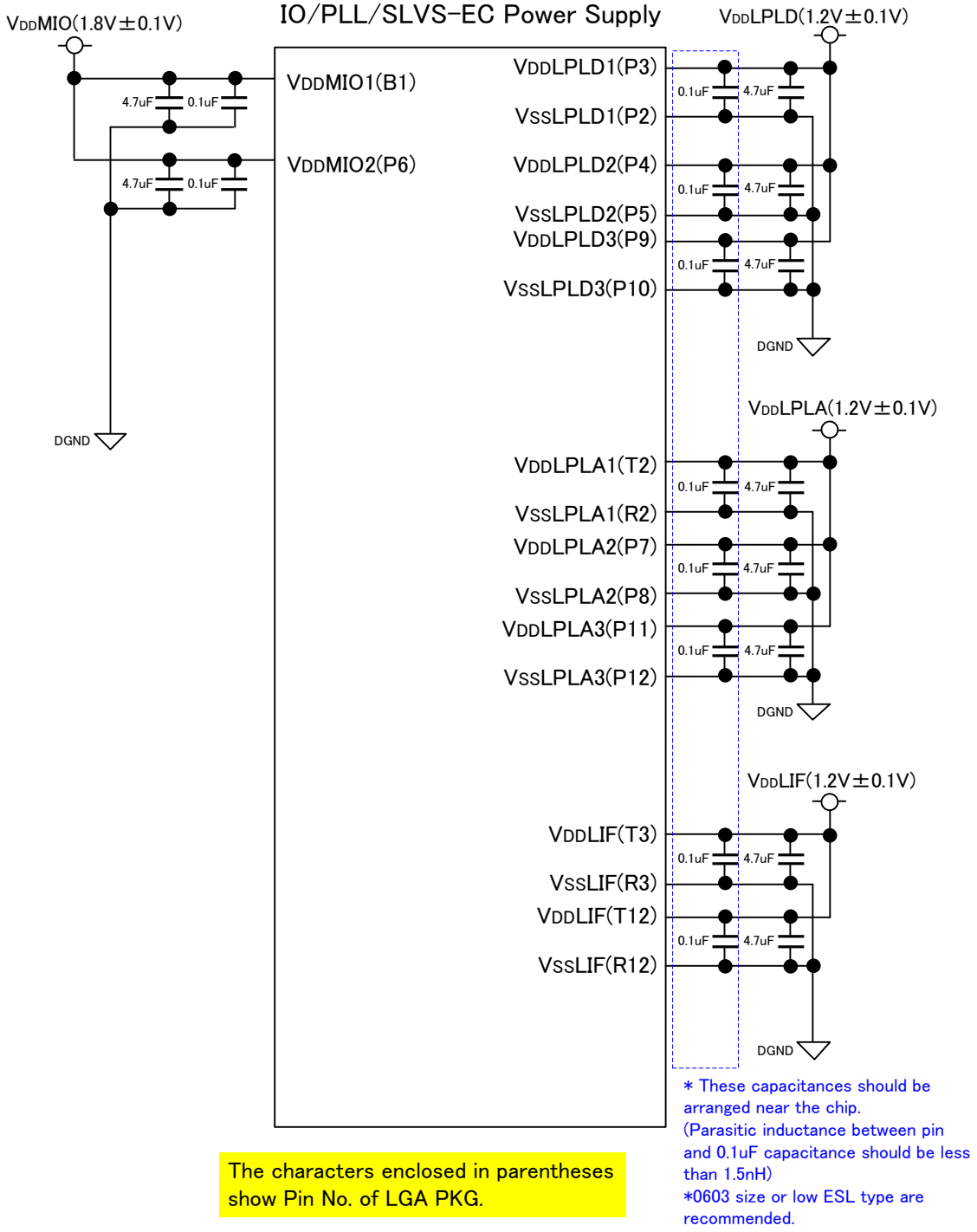
☒ **External pins**

Symbol	Equivalent circuit	Symbol	Equivalent circuit
VRLT VRLS VRML		VRM	
V_{DD}HPX V_{DD}HVD		V_{SS}HPX	
V_{DD}HVS		V_{DD}MPX	
V_{DD}HCM_N V_{DD}HCM_S	 V_{DD}HCM_N and V_{DD}HCM_S are separated. V_{DD}HCM_N pairs with V_{SS}HCM_N. V_{DD}HCM_S pairs with V_{SS}HCM_S.	V_{SS}HCM_N V_{SS}HCM_S	 V_{SS}HCM_N and V_{SS}HCM_S are separated.
V_{DD}HDA1 to 2	 V_{DD}HDA1 and V_{DD}HDA2 are separated. V_{DD}HDA1 pairs with V_{SS}HDA1. V_{DD}HDA2 pairs with V_{SS}HDA2.	V_{SS}HDA1 to 2	 V_{SS}HDA1 and V_{SS}HDA2 are separated.

Symbol	Equivalent circuit	Symbol	Equivalent circuit
V_{DD}HAN_N V_{DD}HAN_S	 V_{DD}HAN_N and V_{DD}HAN_S are separated. V_{DD}HAN_N pairs with V_{SS}HAN_N. V_{DD}HAN_S pairs with V_{SS}HAN_S.	V_{SS}HAN_N V_{SS}HAN_S	 V_{SS}HAN_N and V_{SS}HAN_S are separated.
V_{DD}SUB		V_{DD}MIO1 to 2	 V_{DD}MIO1 and V_{DD}MIO2 are separated.
V_{DD}LSC		V_{SS}LSC	
V_{DD}LCB_N V_{DD}LCB_S	 V_{DD}LCB_N and V_{DD}LCB_S are separated. V_{DD}LCB_N pairs with V_{SS}LCB_N. V_{DD}LCB_S pairs with V_{SS}LCB_S.	V_{SS}LCB_N V_{SS}LCB_S	 V_{SS}LCB_N and V_{SS}LCB_S are separated.
V_{DD}LCN_N V_{DD}LCN_S	 V_{DD}LCN_N and V_{DD}LCN_S are separated. V_{DD}LCN_N pairs with V_{SS}LCN_N. V_{DD}LCN_S pairs with V_{SS}LCN_S.	V_{SS}LCN_N V_{SS}LCN_S	 V_{SS}LCN_N and V_{SS}LCN_S are separated.
V_{DD}LIF		V_{SS}LIF	

Symbol	Equivalent circuit	Symbol	Equivalent circuit
V_{DD}LPLA1 to 3	 V_{DD}LPLA1 to V_{DD}LPLA3 are separated. V_{DD}LPLA1 to V_{DD}LPLA3 pair with V_{SS}LPLA1 to V_{SS}LPLA3.	V_{SS}LPLA1 to 3	 V_{SS}LPLA1 to V_{SS}LPLA3 are separated.
V_{DD}LPLD1 to 3	 V_{DD}LPLD1 to V_{DD}LPLD3 are separated. V_{DD}LPLD1 to V_{DD}LPLD3 pair with V_{SS}LPLD1 to V_{SS}LPLD3.	V_{SS}LPLD1 to 3	 V_{SS}LPLD1 to V_{SS}LPLD3 are separated.
INCK		XCLR	
XVS, XHS, XCE, XPI, SCK, SDI		SDO	
VBGR1 VBGR2 BIASRESBC1 BIASRESBC2		VLOADCM1 VLOADCM2	
VLOADLM1 VLOADLM2 VLOADCMSF1 VLOADCMSF2		DOP0 to 7 DOM0 to 7	

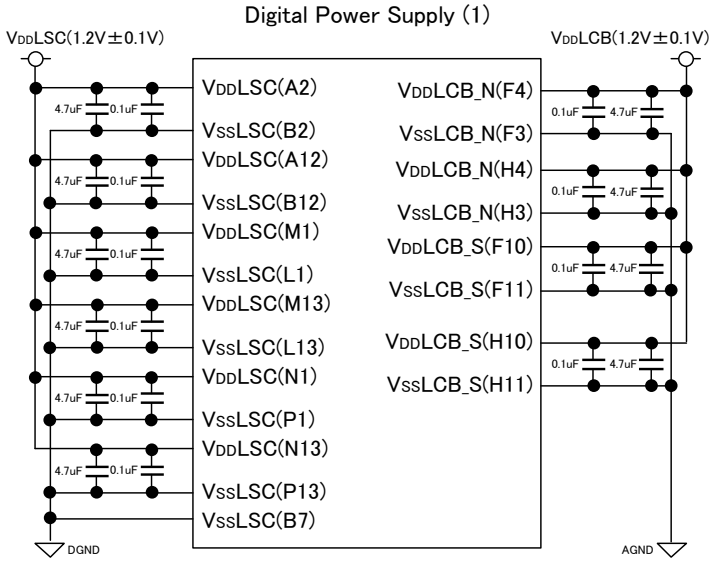
Example of Peripheral Circuit Diagram



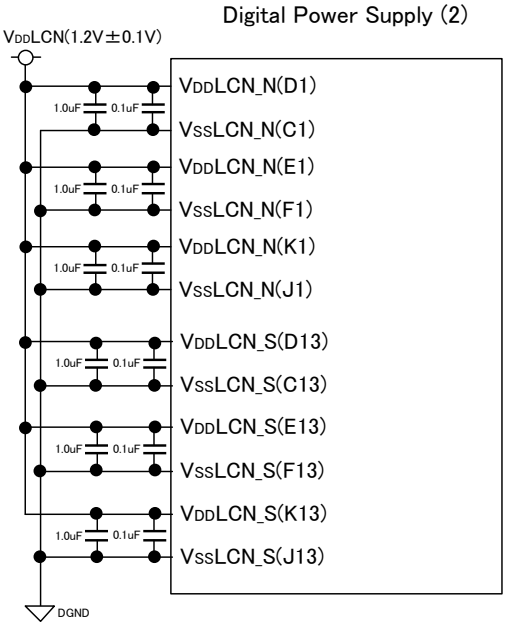
The characters enclosed in parentheses show Pin No. of LGA PKG.

* These capacitances should be arranged near the chip.
(Parasitic inductance between pin and 0.1uF capacitance should be less than 1.5nH)
*0603 size or low ESL type are recommended.

Digital Power Supply (1)

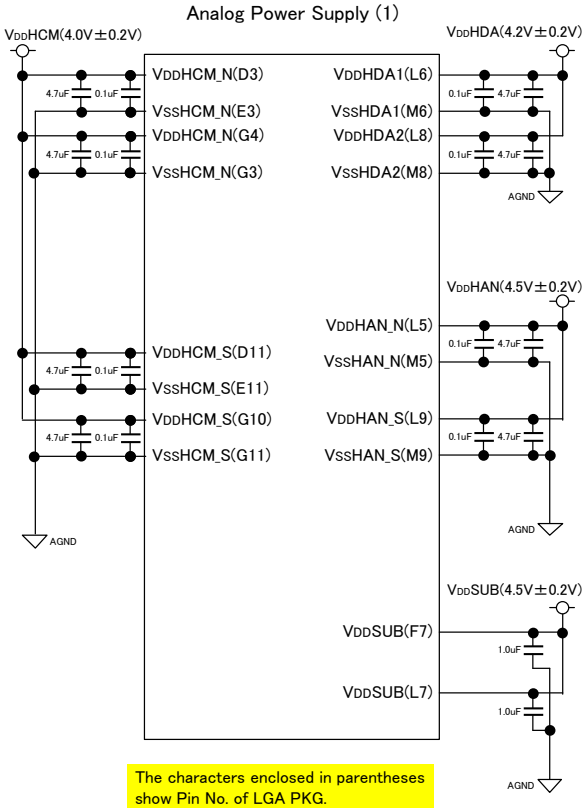


Digital Power Supply (2)

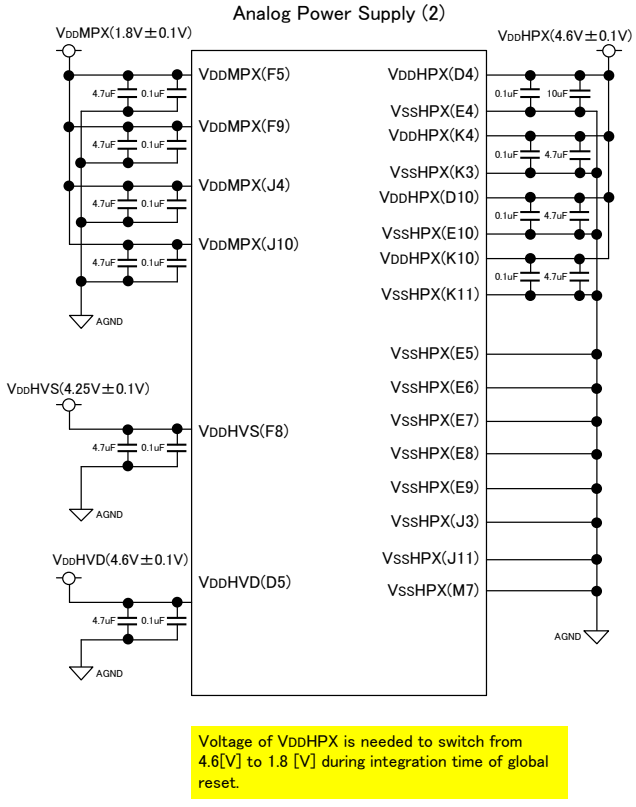


The characters enclosed in parentheses show Pin No. of LGA PKG.

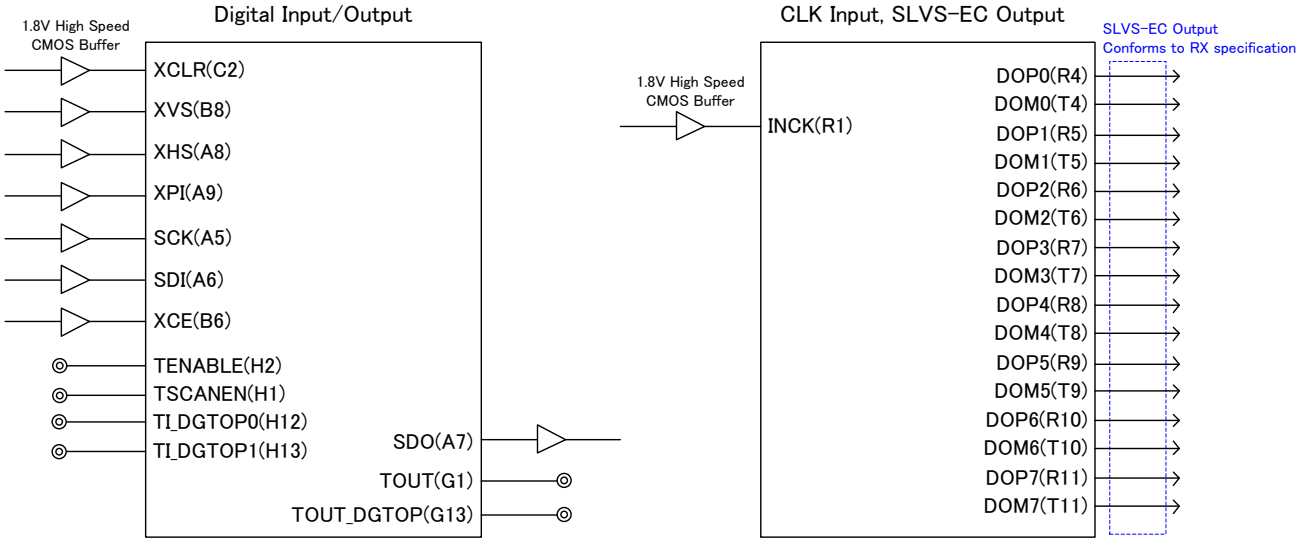
Analog Power Supply (1)



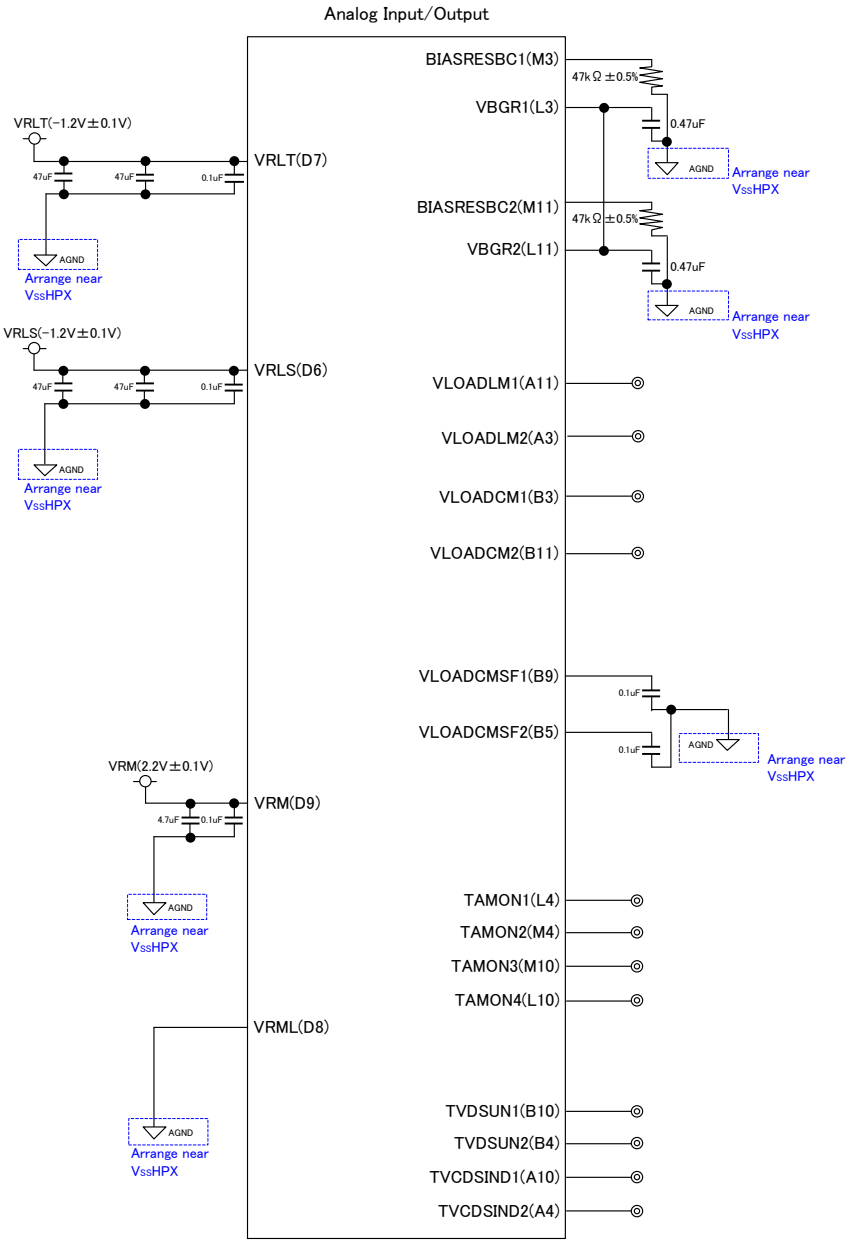
Analog Power Supply (2)



Voltage of VDDHPX is needed to switch from 4.6[V] to 1.8 [V] during integration time of global reset.



The characters enclosed in parentheses show Pin No. of LGA PKG.



The characters enclosed in parentheses show Pin No. of LGA PKG.

Electrical Characteristics

DC Characteristics

Item	Pin name	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}SUB	—	4.3	4.5	4.7	V	Substrate potential
	V_{DD}HPX	—	4.5	4.6	4.7	V	Pixel power supply
			1.7	1.8	1.9	V	Pixel power supply only when using sleep setting during long time exposure mode
	V_{SS}HPX	—	—	0.0	—	V	Pixel GND
	V_{DD}HVD	—	4.5	4.6	4.7	V	DAC power supply
	V_{DD}HVS	—	4.15	4.25	4.35	V	Positive power supply for pixel drive
	V_{DD}MPX	—	1.7	1.8	1.9	V	Pixel power supply (for long time integration)
	V_{DD}LPLA	—	1.1	1.2	1.3	V	PLL power supply (Analog)
	V_{SS}LPLA	—	—	0.0	—	V	PLL GND (Analog)
	V_{DD}LPLD	—	1.1	1.2	1.3	V	PLL power supply (Digital)
	V_{SS}LPLD	—	—	0.0	—	V	PLL GND (Digital)
	V_{DD}HCM	—	3.8	4.0	4.2	V	Comparator power supply
	V_{SS}HCM	—	—	0	—	V	Comparator GND
	V_{DD}HDA	—	4.0	4.2	4.4	V	DAC power supply
	V_{SS}HDA	—	—	0.0	—	V	DAC GND
	V_{DD}HAN	—	4.3	4.5	4.7	V	DAC power supply
	V_{SS}HAN	—	—	0.0	—	V	DAC GND
	V_{DD}LCB	—	1.1	1.2	1.3	V	Comparator buffer power supply
	V_{SS}LCB	—	—	0.0	—	V	Comparator buffer GND
	V_{DD}LCN	—	1.1	1.2	1.3	V	Counter power supply
	V_{SS}LCN	—	—	0.0	—	V	Counter GND
	V_{DD}MIO	—	1.7	1.8	1.9	V	Digital I/O power supply
	V_{DD}LSC	—	1.1	1.2	1.3	V	Digital power supply
	V_{SS}LSC	—	—	0.0	—	V	Digital GND
	V_{DD}LIF	—	1.1	1.2	1.3	V	SLVS-EC power supply
	V_{SS}LIF	—	—	0.0	—	V	SLVS-EC GND
	VRLT	—	-1.3	-1.2	-1.1	V	Negative power supply for pixel drive
	VRLS	—	-1.3	-1.2	-1.1	V	Negative power supply for pixel drive
	VRM	—	2.1	2.2	2.3	V	Power supply for pixel drive
	VRML	—	—	0.0	—	V	Power supply for pixel drive

Item	Pin name	Symbol	Min.	Typ.	Max.	Unit	Remarks
Digital input Voltage	INCK	I_{ILK1}	-30	—	30	μA	Input leakage current
		V_{IL1}	—	—	0.3×V_{DD}MIO	V	“Low” level input voltage
		V_{IH1}	0.7×V_{DD}MIO	—	—	V	“High” level input voltage
	XCE, SCK, SDI,XCLR, XVS, XHS, XPI	I_{ILK2}	–30	—	30	μA	
		V_{IL2}	—	—	0.3×V_{DD}MIO	V	
		V_{IH2}	0.7×V_{DD}MIO	—	—	V	
		V_{IH2}-V_{IL2}	—	0.3	—	V	Hysteresis
Digital output voltage	SDO	V_{OL}	—	—	V_{SS}MIO + 0.2	V	I_{OL} = 1 mA
		V_{OH}	V_{DD}MIO – 0.2	—	—	V	I_{OH} = 1 mA
Analog pin	VBGR1, VBGR2,	—	0.0	1.21	4.5	V	V_{DD}HAN power supply
	BIASRESBC1, BIASRESBC2	—	0.0	1.21	4.5	V	V_{DD}HAN power supply
	VLOADLM1, VLOADLM2	—	0.0	0.6	4.6	V	V_{DD}HPX power supply
	VLOADCM1, VLOADCM2	—	0.0	0.8	4.5	V	V_{DD}HCM power supply
	VLOADCMSF1, VLOADCMSF2	—	0.0	3.7	4.6	V	V_{DD}HPX power supply
	TAMON1, TAMON2, TAMON3, TAMON4	—	0.0	1.53	2.1	V	V_{DD}HPX power supply

SLVS-EC Output DC Characteristics

The characteristics of the TX of SLVS-EC are defined in the characteristic at the output pin of the package as shown in figure below.

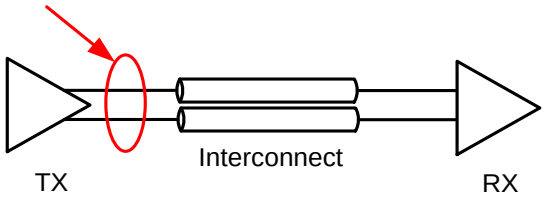


Fig. Definition of the characteristics of SLVS-EC

The details about the SLVS-EC, please refer of the “SLVS-EC Specification Version 1.2”.

Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit
Digital output voltage	DOP0 to DOP7, DOM0 to DOM7	Differential DC Voltage	VDIF_DC_TX	160	—	280	mV
		Common Mode Voltage	VCM_TX	160	—	260	mV
		Single-ended Output Resistance	RSED_TX	30	—	60	Ω

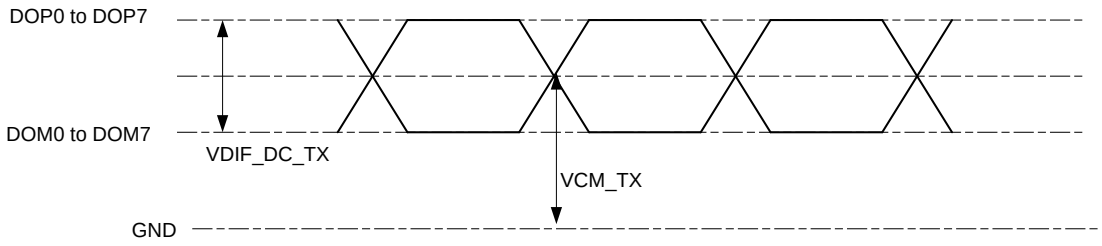
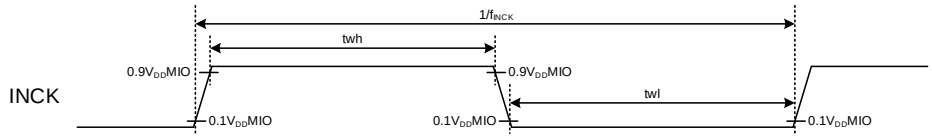


Fig. DC output of TX of SLVS-EC

AC Characteristics

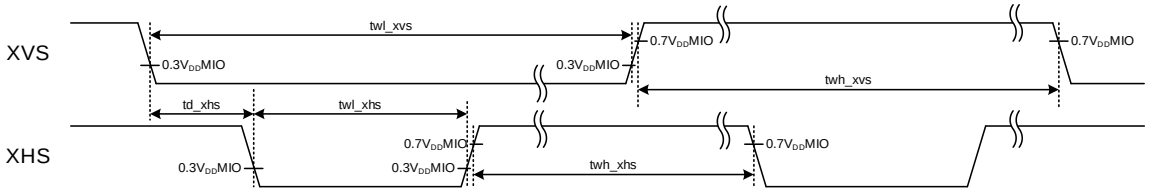
System Clock INCK



(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
f_{INCK}	INCK clock frequency	—	72	—	MHz
FERR	Clock frequency error	-300	—	300	ppm
twl	INCK Low level width	5.0	—	—	ns
twh	INCK High level width	5.0	—	—	ns
twh / (1/f_{INCK}) twl / (1/f_{INCK})	Duty cycle	40	50	60	%
PN100K	Phase noise (100 kHz)	—	—	-135	dBc/Hz
PN1M	Phase noise (1 MHz)	—	—	-140	dBc/Hz

XVS, XHS Load Characteristics



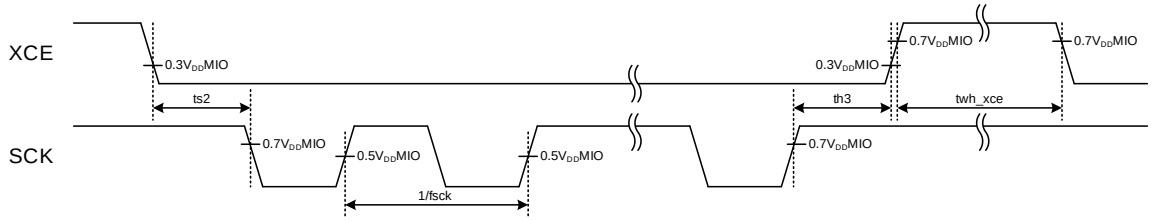
(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
td_xhs	XVS – XHS delay period	3	—	—	t_{INCK}
twl_xhs	XHS Low level period	12	—	—	t_{INCK}
twh_xhs	XHS High level period	12	—	—	t_{INCK}
twl_xvs	XVS Low level period	12	—	—	t_{INCK}
twh_xvs	XVS High level period	12	—	—	t_{INCK}

$t_{INCK} = 1/f_{INCK}$

Serial Communication

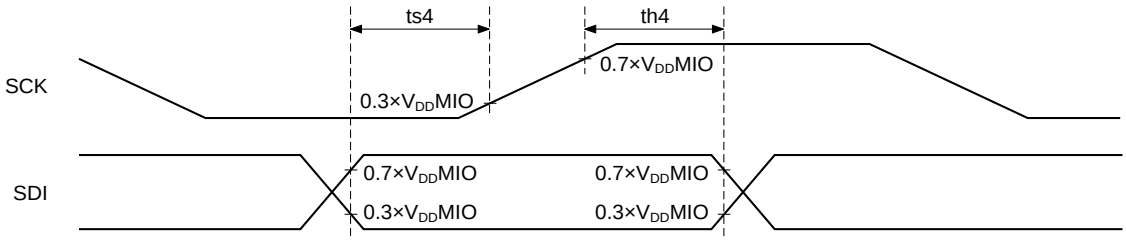
XCE - SCK AC Characteristics



(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts2	XCE setup time for the falling edge of SCK	20	—	—	ns
th3	XCE hold time for the rising edge of SCK	20	—	—	ns
twh_xce	XCE High period (Interval until the next communicating)	50	—	—	ns
f_{SCK}	SCK clock frequency	—	—	28.0	MHz

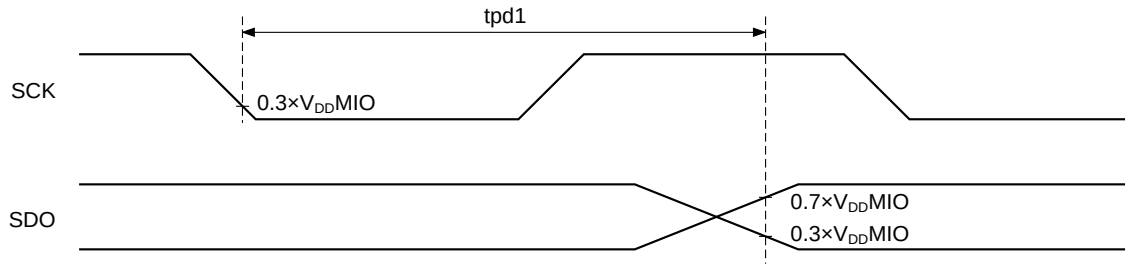
SCK - SDI AC Characteristics



(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts4	SDI setup time for the rising edge of SCK	10.0	—	—	ns
th4	SDI hold time for the rising edge of SCK	5.0	—	—	ns

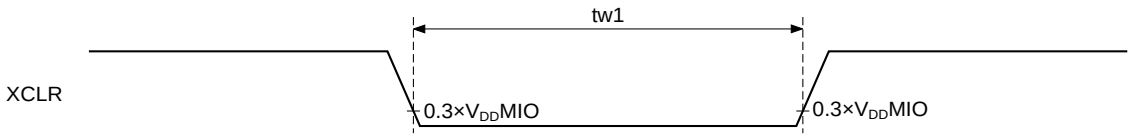
SCK - SDO AC Characteristics



(Within the range of guaranteed operating temperature and DC characteristics current voltage and SDO load capacitance: 10 pF)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	SDO delay for the falling edge of SCK	3	—	30	ns

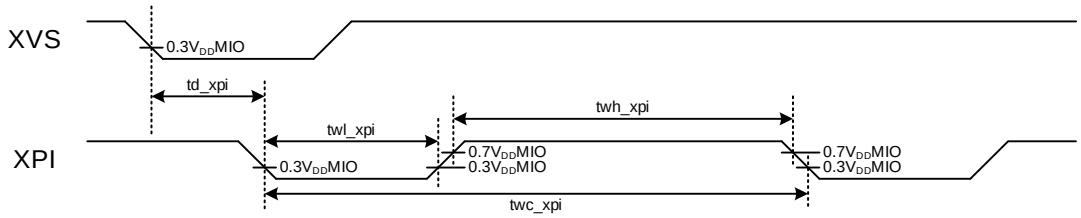
System Reset



(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	XCLR pulse width	10	—	—	μs

XPI (Non-linear electronic curtain shutter timing input)



(Within the range of guaranteed operating temperature and DC characteristics current voltage)

Symbol	Definition	Min.	Typ.	Max.	Unit
td_xpi	XVS-XPI delay time	700	—	—	t_{INCK}
twh_xpi	XPI High period	5	—	—	t_{INCK}
twl_xpi	XPI Low period	5	—	—	t_{INCK}
twc_xpi	XPI pulse cycle	20	—	—	t_{INCK}

SCLVS-EC Output AC Characteristics

The characteristics of the TX of SLVS-EC are defined in the characteristic at the output pin of the package as shown in the figure below.

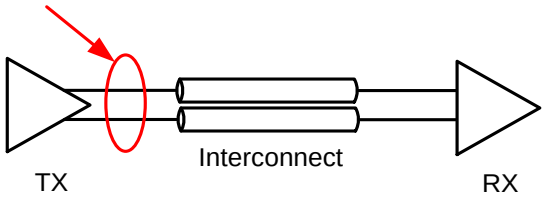
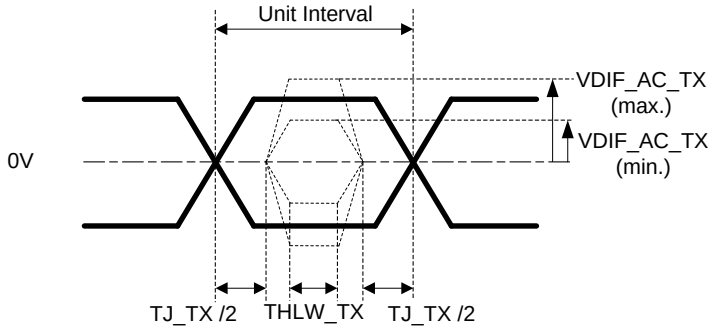


Fig. Define of the characteristics of the SLVS-EC

The details about SLVS-EC, please refer to the “SLVS-EC Specification Version 1.2”.

Item	Symbol	Min.	Typ.	Max.	Unit.	Remarks
Differential AC Voltage	VDIF_AC_TX	140	—	290	mV	100Ω differential connection
Eye High/Low width	THLW_TX	0.2	—	—	UI	100Ω differential connection
Deterministic Jitter	DJ_TX	—	—	0.3	UI	100Ω differential connection
Total Jitter	TJ_TX	—	—	0.4	UI	100Ω differential connection
Skew between the lanes	TLSKEW_TX	—	—	5	SI	Note)

Note) Regarding Input Skew between lanes spec, Rx receiver should be designed for the worst spec of SLVS-EC Ver. 1.2 Rx characteristics: 10SI.



AC output of TX in SLVS-EC

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics)

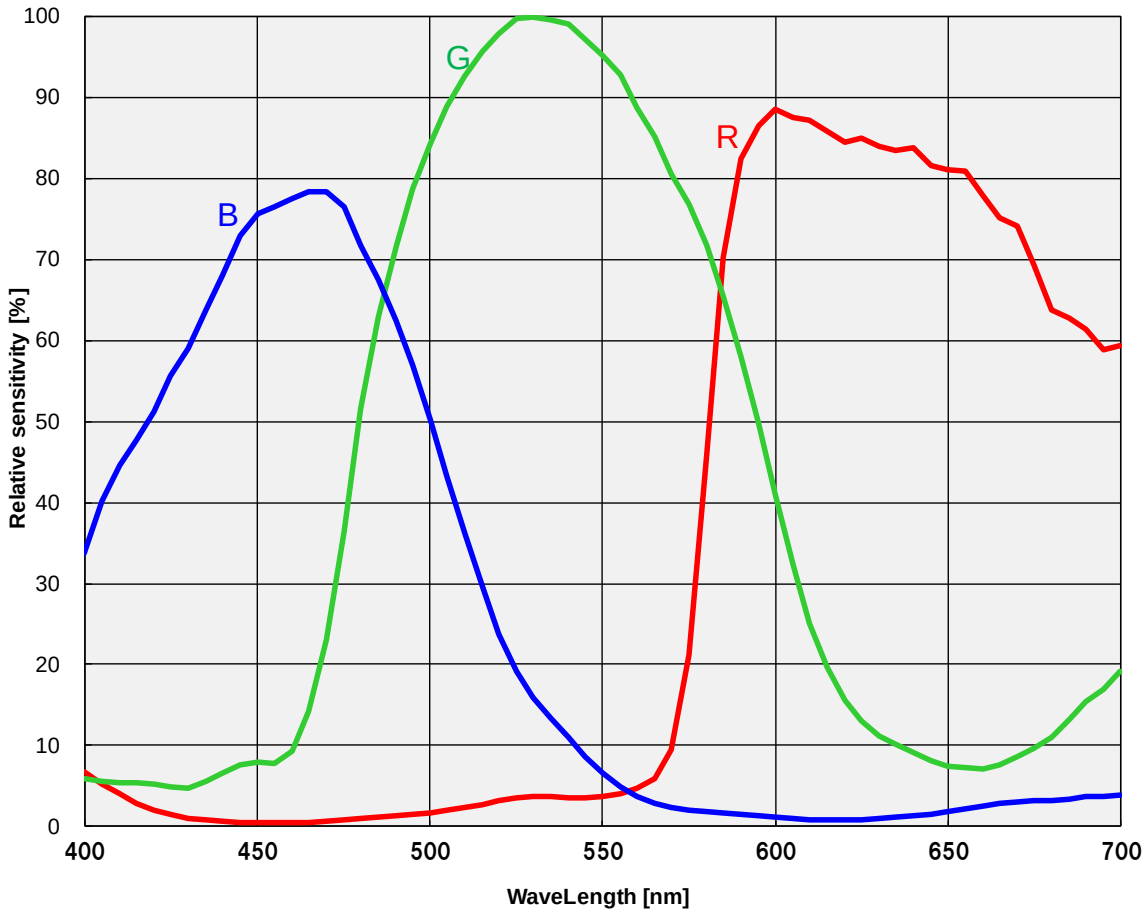


Image Sensor Characteristics

(Sensor signal, Tj = 60 ˚C, Reference gain 0dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measure-ment method	Remarks
Sensitivity	Sg	4786	5630	6475	LSB	1	1/30 s integration Zone 0
Sensitivity ratio	Rr	0.24	0.39	0.54	—	2	—
	Rb	0.30	0.45	0.60			—
Saturation signal	Vsat	14168	—	—	LSB	3	left for 0.4 s Zone 0 to III
		10152	—	—	LSB	3	left for 30 s Zone 0 to III
Video signal shading	SH	—	—	20	%	4	Zone 0, I
		—	—	30			Zone 0 to II’
Horizontal dark shading	ΔVh	—	—	4.5	LSB	5	Zone 0 to III + OB
Vertical stripe fixed pattern	V_{FPN}	—	—	0.76	LSB	6	Zone 0 to III + OB
Vertical stripes by gain	—	—	—	0.75	%	12	Zone 0 to II’
Dark signal	Vdt	—	—	0.76	LSB	7	1/30 s integration
Dark signal shading	ΔVdt	—	—	6.5	LSB	8	—
Line crawl R	Lcr	-3	—	3	%	9	—
Line crawl R uniformity	ΔLcr	—	—	5	%	10	—
Line crawl B	Lcb	-2.5	—	2.5	%	9	—
Line crawl B uniformity	ΔLcb	—	—	3	%	10	—
Lag	Lag	—	—	Below the measure-ment limit	%	11	—

* Shown LSB when 14-bit output.
  Example of LSB conversion: 1 digit ≈ 0.08606 mV when 14-bit output.

Zone Definition of Image Sensor Characteristics

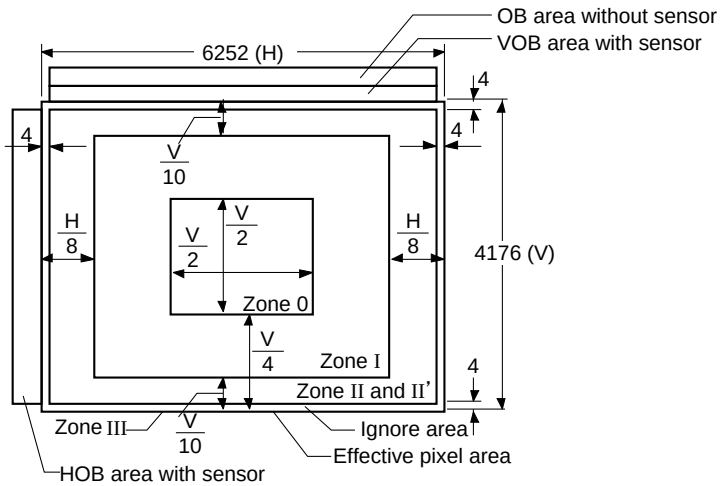


Image Sensor Characteristics Measurement Method

Measurement condition

1. In the following measurements, the device drive conditions are at the typical values of the register setting, AC characteristics and DC characteristics.
2. In the following measurements, spot pixels are excluded, and unless otherwise specified, the level of optical black with sensor excluding spot pixels is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

Color Coding and Readout of this Image Sensor

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure above (Bayer array). Gr and Gb represent the G signal on the same line as the R and B signals, respectively.

Definition of Standard Imaging Conditions

◆ Standard imaging condition I

Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II

Image a light source (color temperature of 5100 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the integration time to 1/16.3 s by rolling shutter operation, measure the signal values (V_{Gr}, V_{Gb}, V_R, V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formula.

   $V_G = (V_{Gr} + V_{Gb})/2$
   $Sg = V_G \times 16.3/30$ [LSB]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition I. After setting the integration time to 1/16.3 s by rolling shutter operation, insert color temperature conversion filter and adjust the condition to color temperature 5100 K. Measure the signal values (V_{Gr}, V_{Gb}, V_R, V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formula.

   $V_G = (V_{Gr} + V_{Gb})/2$
   $Rr = V_R/V_G$
   $Rb = V_B/V_G$

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times of the intensity with the average value of the Gr signal output, 8192 LSB. After sensor saturation, perform readout operation in rolling shutter mode and measure the minimum values of the Gr, Gb, R and B signals using OB as a reference.

4. Video signal shading
   Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F5.6, adjust the luminous intensity so that the average value of the Gr signal output is 8192 LSB. Then measure the maximum value (Grmax) and the minimum value (Grmin) of the Gr signal output, and substitute the values into the following formula.

   SHg = (Grmax – Grmin) / 8192 × 100 [%]

5. Horizontal dark shading
   Set the device to a dark setting and the influence of the dark signal is eliminated enough. Generate the Vh signal which the output signals are added and averaged in vertical direction. Then measure the maximum value (Vhmax [LSB]) and the minimum value (Vhmin [LSB]), and substitute the values into the following formula.

   ΔVh = Vhmax – Vhmin [LSB]

6. Vertical stripe fixed pattern
   Following the item 5, measure the local change point of the Vh signal. V_{FPN} is the maximum value of the measurement.

7. Dark signal
   Measure the average value (Vdt [LSB]) of the signal output based on output level of VOB in the light-obstructed state.

8. Dark signal shading
   Following the item 7, measure the maximum value (Vdmax [LSB]) and minimum value (Vdmin [LSB]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [LSB]

9. Line crawl

Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F5.6, after adjusting the average value of the Gr signal output to 8192 LSB, insert R, G and B filters, and then measure the difference between the G signal lines (ΔGlr, ΔGlg, ΔGlb [LSB]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

$$Lci = (\Delta Gli / Gai) \times 100 \ [\%] \ (i = r, g, b)$$

10. Line crawl uniformity

Following the item 9, measure the difference between the G signal lines (ΔGlrn, ΔGlgn, ΔGlbn [LSB]) and the average value of the G signal output (Garn, Gagn, Gabn [LSB]) in the local area divided into 30 × 25 (= 750) of Zone II'. Substitute the values into the following formula.

$$Lcin = (\Delta Glin / Gain) \times 100 \ [\%] \ (i = r, g, b, n = 1 \text{ to } 750)$$

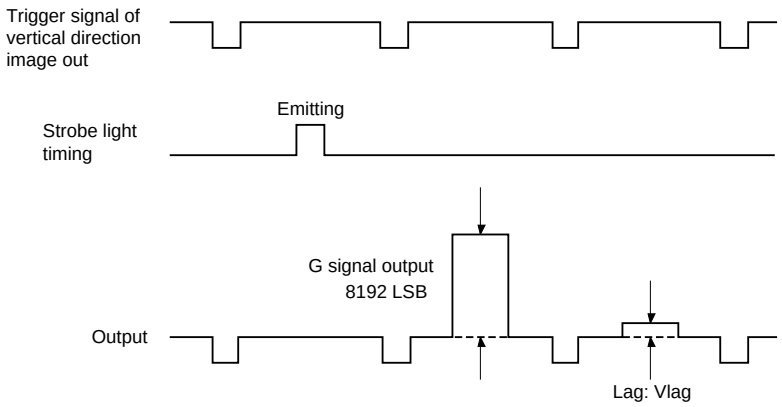
Measure the maximum value Lcin_max and the minimum value Lcin_min of them, and substitute the values into the following formula.

$$\Delta Lci = Lcin\_max - Lcin\_min \ [\%]$$

11. Lag

Adjust the G signal output value generated by strobe light to 8192 LSB. After setting the strobe light so that it strobes with the following timing, measure the residual signal level (Vlag), and substitute the value into the following formula.

$$Lag = (Vlag/8192) \times 100 \ [\%]$$



12. Vertical stripes by gain

Adjusts the luminous intensity so that the average value of the Zone II' signal output is 8192 LSB. The output signals are added and averaged in vertical direction and they are defined as Vh. Measures measure the local change point of the Vh signal, and divide the maximum value of Vh by the average value of Vh.

Setting Registers by Serial Communication

1. Setting Registers by Serial Communication

Sensor operation is controlled by the register settings. Follow the procedure below and make the register settings by serial communication.

1. Set XCE Low to enable the chip's serial communication function.
2. Transmit serial data (SDI) synchronized with SCK 1 bit at a time from the lower bits.
3. Transmit the Chip ID (fixed value: 81h) in the first byte.
4. Transmit the address value of the register to be set in the second and third bytes.
5. Transmit the register setting value to the address designated by the second and third bytes in the fourth byte.
6. Transmit the register setting value to the address following the address designated by the second and third bytes in the fifth byte.
7. Transmit the register setting values to subsequent addresses in order thereafter.
8. Set XCE High to end serial communication.

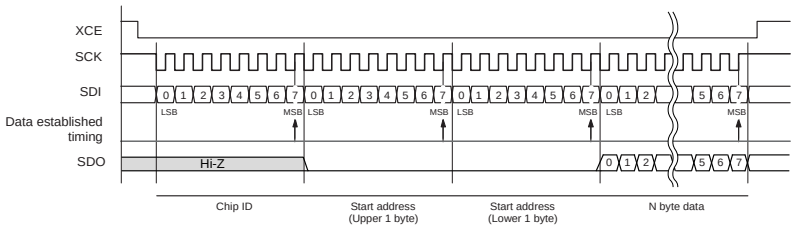
The sensor clears the Chip ID and address setting data by setting XCE High. Therefore, the Chip ID and address settings must also be made when the next serial communication is performed.
Continuous write across upper bytes is prohibited. When writing across upper bytes, first complete the above sequence, and then perform communication again. In addition, when jumping to a discontinuous address, also first complete the above sequence, and then perform communication again.
Perform serial communication within rear V blank period to avoid affecting the image quality.

Note) 1. Communication is always accepted except for the XCLR = Low period.
2. Communication should be completed within the recommended serial communication period to prevent noise. However, this restriction does not apply during the readout period of non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), so register communication can be performed other than during the communication period of those frames.

Table Chip ID and Serial Communication Operation

Chip ID	Mode	Internal register write	Internal register readout
81h	Normal communication	Yes	Yes
82h	Read back	No	Yes

Example of Serial Communication Timing



Example of Serial Communication

2. Register Value Reflection Timing

The register values established by register communication are reflected at the following timings.

Reflection timing	Description
Immediately	The communication contents are reflected immediately.
V sync	In case of rolling shutter operation, the communication contents are reflected when readout frame XVS pules is input. And in case of global reset shutter operation, the communication contents are reflected when exposure frame XVS pulse is input.

For which reflection timing of each register, see “Register Map”.

Immediately

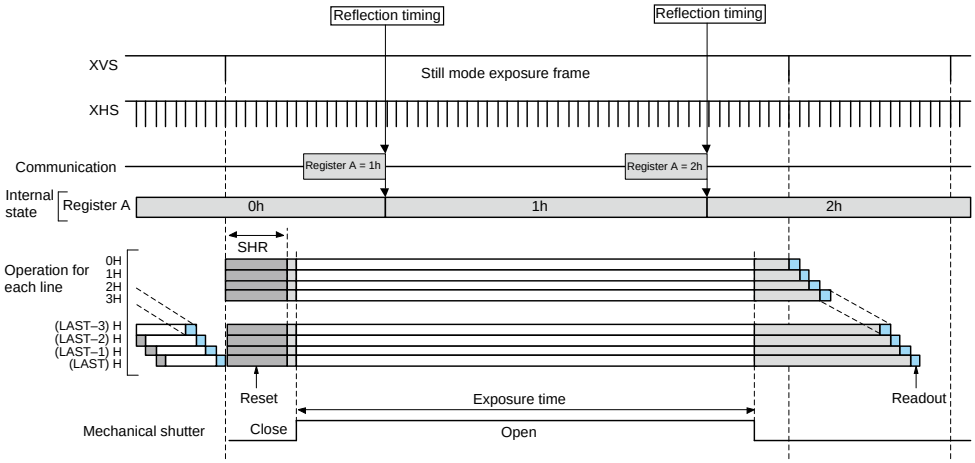


Fig. Example of Immediately reflection timing (Register A)

V sync

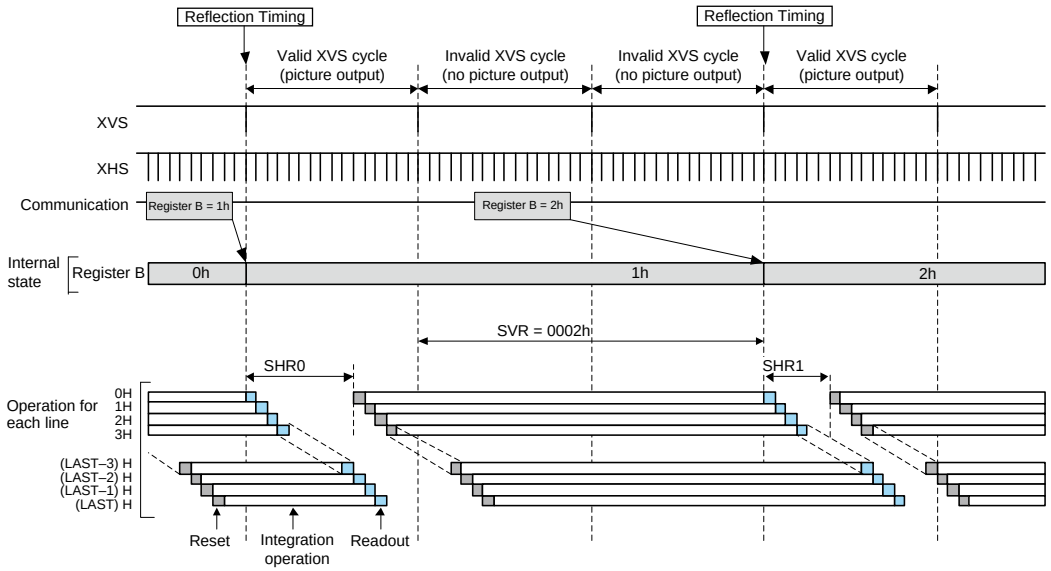


Fig. Example of V sync Reflection Timing in Rolling Shutter Operation (Register B)

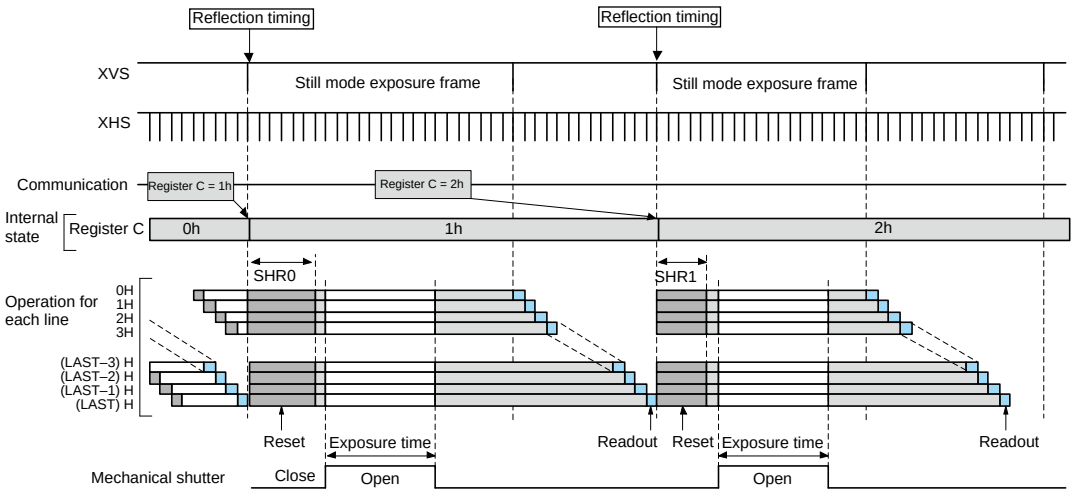


Fig. Example of V sync Reflection Timing in Global Reset Shutter Operation (Register C)

Register Map

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
0000h	[0]	STANDBY	Immediately	Standby control register 0h: Normal operation 1h: Standby mode	0h
	[1]	—	—	—	0h
	[2]	WAKEUP	Immediately	When changed from 0h to 1h: Cancels pre-startup stop mode	0h
	[7:3]	—	—	—	00h
0001h	[4:0]	MODE	V sync	Drive mode select See the value according to each readout mode register setting	00h
	[7:5]	—	—	—	0h
0003h	[0]	SMD	V sync	Shutter mode select 0h: Rolling shutter 1h: Global reset shutter	0h
	[1]	MSMD	V sync	Global reset shutter mode control 0h: All-pixel simultaneous reset mode 1h: Electronic first curtain shutter mode	0h
	[2]	OPMODE	V sync	Electronic first curtain shutter mode select 0h: Polygon electronic first curtain shutter 1h: Non-linear electronic first curtain shutter	0h
	[4:3]	—	—	—	2h
	[5]	VSHT_DIR	V sync	Electronic first curtain shutter scanning direction switching 0h: Normal Direction Area 1 → Area 48 (Pixel address small → large) 1h: Inverted Direction Area 48 → Area 1 (Pixel address large → small)	1h
	[6]	SSBRK	Immediately	Slow shutter break	0h
	[7]	—	—	—	0h
0004h	[0]	LESS_SHUT	V sync	Shutter less mode switch 0h: Shutter less mode OFF 1h: Shutter less mode ON	0h
	[1]	LESS_SHUT_DOL1	V sync	Shutter less mode switch for digital overlap drive at short time exposure frame 0h: Shutter less mode OFF 1h: Shutter less mode ON	0h
	[2]	LESS_SHUT_DOL2	V sync	Shutter less mode switch for digital overlap drive at long time exposure frame 0h: Shutter less mode OFF 1h: Shutter less mode ON	0h
	[7:3]	—	—	—	00h
0005h	[0]	GLB4FLD	V sync	Global 4 field readout drive switch 0h: Normal operation 1h: Global 4 field readout drive	0h
	[7:1]	—	—	—	00h
0007h	[1:0]	WND	V sync	Window readout mode 0h: Window readout mode OFF 1h: Window readout mode ON 2h, 3h: Prohibited	0h
	[7:2]	—	—	—	00h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
0008h	[7:0]	WIN_START	V sync	Start line for window readout (Physical address)	0019h
0009h	[5:0]				
	[7:6]	—	—	—	0h
000Ah	[7:0]	WIN_WIDTH	V sync	Number of output lines for window readout	1050h
000Bh	[5:0]				
	[7:6]	—	—	—	0h
0014h	[7:0]	SVR	V sync	Rolling storage frame period	000h
0015h	[3:0]				
	[7:4]	—	—	—	0h
0016h	[7:0]	SPL	V sync	Rolling storage start timing XVS control	000h
0017h	[3:0]				
	[7:4]	—	—	—	0h
0018h	[7:0]	SHR	V sync	Storage start timing XHS control	0002h
0019h	[6:0]				
	[7]	—	—	—	0h
001Ah	[7:0]	SINT	V sync	Electronic first curtain shutter reset start timing (64clk@36[MHz] unit) *00h : Setting prohibited.	01h
001Bh	[7:0]	READ_START_DOL1	V sync	Read start position for short time exposure in digital overlap mode.	0009h
001Ch	[6:0]				
	[7]	—	—	—	0h
001Dh	[7:0]	SHR_DOL1	V sync	XHS control of short time exposure start timing in digital overlap mode	0005h
001Eh	[6:0]				
	[7]	—	—	—	0h
001Fh	[7:0]	SHR_DOL2	V sync	XHS control of long time exposure start timing in digital overlap mode.	000Eh
0020h	[6:0]				
	[7]	—	—	—	0h
0027h	[5:0]	VBLK_WIDTH	V sync	Number of lines for Front V blank Must be even number (unit: XHS) *Min. 04h Recommended value: 06h	04h
	[7:6]	—	—	—	0h
0028h	[7:0]	BK_WIDTH	V sync	Number of lines for black dummy Must be even number (unit: XHS)	0000h
0029h	[5:0]				
	[7:6]	—	—	—	0h
002Ah	[7:0]	OPBN_WIDTH	V sync	Number of lines for OB without sensor Must be even number	0004h
002Bh	[5:0]				
	[7:6]	—	—	—	0h
002Fh	[3:0]	—	—	—	0h
	[7:4]	APGC_ADD	V sync	Additional analog gain setting See “Gain Setting” for detail	0h
0030h	[7:0]	APGC_N	V sync	North column analog gain setting	000h
0031h	[3:0]				
	[7:4]	—	—	—	0h
0032h	[7:0]	APGC_S	V sync	South column analog gain setting	000h
0033h	[3:0]				
	[7:4]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
0034h	[7:0]	APGC_LT_N	V sync	North column analog gain setting Long time exposure frame (digital overlap drive mode only)	000h
0035h	[3:0]				
	[7:4]	—	—	—	0h
0036h	[7:0]	APGC_LT_S	V sync	South column analog gain setting Long time exposure frame (digital overlap drive mode only)	000h
0037h	[3:0]				
	[7:4]	—	—	—	0h
0038h	[7:0]	APGC_ST_N	V sync	North column analog gain setting Short time exposure frame (digital overlap drive mode only)	000h
0039h	[3:0]				
	[7:4]	—	—	—	0h
003Ah	[7:0]	APGC_ST_S	V sync	South column analog gain setting Short time exposure frame (digital overlap drive mode only)	000h
003Bh	[3:0]				
	[7:4]	—	—	—	0h
0040h	[3:0]	—	—	—	0h
	[6:4]	DGAIN	V sync	Digital gain 0h: OFF 1h: 6[dB] 2h: 12[dB] 3h: 18[dB] 4h: 24[dB] 5h: 30[dB] 6h: 36[dB] 7h: Prohibited	0h
	[7]	—	—	—	0h
0042h	[7:0]	BLKLEVEL_N	V sync	North side Black level setting *Designated as AD 16 bit equivalent.	0FFFh
0043h	[7:0]				
0044h	[7:0]	BLKLEVEL_S	V sync	South side Black level setting *Designated as AD 16 bit equivalent.	0FFFh
0045h	[7:0]				
0048h	[0]	CLPOFF	V sync	Clamp operation 0h: Clamp operation ON 1h: Clamp operation OFF	1h
	[1]	CLPBKOFF	V sync	Black dummy clamp operation 0h: Black dummy clamp operation ON 1h: Black dummy clamp operation OFF	1h
	[2]	CLPOPBOFF	V sync	VOB clamp operation 0h: VOB clamp operation ON 1h: VOB clamp operation OFF	0h
	[7:3]	—	—	—	0h
0049h	[7:0]	CLPBK_VST	V sync	Black dummy clamp start line	00h
004Ah	[7:0]	CLPBK_V	V sync	Number of lines for black dummy clamp	008h
004Bh	[2:0]				
	[7:3]	—	—	—	00h
004Ch	[6:0]	CLPOB_VST	V sync	VOB clamp start line *Prohibited setting to be outside the VOB area with sensor.	00h
	[7]	—	—	—	0h
004Dh	[7:0]	CLPOB_V	V sync	Number of lines VOB clamp *Prohibited setting to be outside the VOB area with sensor.	00Ch
004Eh	[2:0]				
	[7:3]	—	—	—	00h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
004Fh	[2:0]	CLPAPGC	V sync	Clamp gain setting See “Gain Setting” for detail.	2h
	[7:3]	—	—	—	01h
0051h	[2:0]	—	—	—	0h
	[3]	SDO_ACT	Immediately	SDO output enable 0h: Hi-Z 1h: ACT	0h
	[7:4]	—	—	—	0h
00A7h	[0]	HCROP_START_EN	V sync	Horizontal cropping start position setting enable	0h
	[7:1]	—	—	—	00h
00A8h	[7:0]	HCROP_START	V sync	Horizontal cropping start position	000h
00A9h	[0]				
	[7:1]	—	—	—	00h
00D1h	[0]	FIXDTON	V sync	Fixed pattern output mode 0h: OFF 1h: Fixed pattern data output	0h
	[7:1]	—	—	—	00h
00D2h	[0]	—	—	—	0h
	[2:1]	FIXDTSEL	V sync	Fixed pattern output mode select 0h: Shading mode 1h: Color bars mode 2h: Each color channel fixed pattern mode 3h: Prohibited	0h
	[4:3]	FIXDTSFT	V sync	Fixed pattern output mode setting When shading mode: Increment value of sensor outputs 0d: +1d, 1d: +2d, 2d: +4d, 3d: +8d When each color channel fixed pattern mode: Fixed value shift setting 0d: No shift, 1d: 1bit(×2), 2d: 2bits(×4), 3d: 3bits(×8)	0h
	[5]	COLORBARSEL	V sync	Direction setting of color bars 0h: Vertical 1h: Horizontal	0h
	[7:6]	—	—	—	0h
00E6h	[0]	H3SEL	V sync	Horizontal 3 binning or horizontal 1/3 subsampling switching 0h: Horizontal 3 binning 1h: Horizontal 1/3 subsampling	0h
	[7:1]	—	—	—	01h
0113h	[0]	CRC_EN	Immediately	CRC insertion at the end of line 0h: Without CRC insertion 1h: With CRC insertion	0h
	[3:1]	—	—	—	0h
	[5:4]	ECC_EN	Immediately	ECC insertion in lines 0h: Without ECC (ECC Option = 0) 1h: With ECC (ECC Option = 1) 2h: With ECC (ECC Option = 2) 3h: Prohibited	2h
	[7:6]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
0115h	[4:0]	INIT_LENGTH	Immediately	Set the length of low output period during mode change and initialization. default: 0Ah min: 00h, max : 10h	0Ah
	[7:5]	—	—	—	0h
0116h	[7:0]	SYNC_LENGTH	Immediately	Sync Code transfer times default : 007FFFh min: 000001h max: FFFFFFh	007FFFh
0117h	[7:0]				
0118h	[7:0]				
0119h	[7:0]	DESKEW_LENGTH	Immediately	Deskew Code transfer times default: 10h min: 01h, max: FFh	10h
011Ah	[7:0]	DESKEW_INTERVAL	Immediately	Deskew Code transmission interval default: 10h min: 04h, max: FCh Setting value must be a multiple of 4.	10h
011Bh	[7:0]	STANDBY_LENGTH	Immediately	Standby Code transfer times default: 10h min: 03h, max: FFh	10h
011Ch	[7:0]	SYNC_SYMBOL	Immediately	Set the symbol following the comma symbol within the Sync Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.10.5 (0AAh)	0AAh
011Dh	[0]				
	[7:1]	—	—	—	00h
011Eh	[7:0]	DESKEW_SYMBOL	Immediately	Set the symbol following the comma symbol within the Deskew Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.00.3 (060h)	060h
011Fh	[0]				
	[7:1]	—	—	—	00h
0120h	[7:0]	IDLE_CODE1	Immediately	Set the 1st symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.00.0 (000h)	000h
0121h	[0]				
	[7:1]	—	—	—	00h
0122h	[7:0]	IDLE_CODE2	Immediately	Set the 2nd symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.00.0 (000h)	000h
0123h	[0]				
	[7:1]	—	—	—	00h
0124h	[7:0]	IDLE_CODE3	Immediately	Set the 3rd symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.00.0 (000h)	000h
0125h	[0]				
	[7:1]	—	—	—	00h
0126h	[7:0]	IDLE_CODE4	Immediately	Set the 4th symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.00.0 (000h)	000h
0127h	[0]				
	[7:1]	—	—	—	00h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
012Ah	[7:0]	STANDBY_SYMBOL	Immediately	Set the symbol following the comma symbol within the standby code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character default : D.03.0 (003h)	003h
012Bh	[0]				
	[7:1]	—	—	—	00h
013Ah	[7:0]	POLYGON_OP_SPEED1	V sync	Polygon electronic first curtain shutter speed adjustment of Area 1. *Area width is register setting value + 1clk.	14h
013Bh	[7:0]	POLYGON_OP_SPEED2	V sync	Polygon electronic first curtain shutter speed adjustment of Area 2. *Area width is register setting value + 1clk.	28h
013Ch	[7:0]	POLYGON_OP_SPEED3	V sync	Polygon electronic first curtain shutter speed adjustment of Area 3. *Area width is register setting value + 1clk.	3Ch
013Dh	[7:0]	POLYGON_OP_SPEED4	V sync	Polygon electronic first curtain shutter speed adjustment of Area 4. *Area width is register setting value + 1clk.	50h
013Eh	[7:0]	POLYGON_OP_SPEED5	V sync	Polygon electronic first curtain shutter speed adjustment of Area 5. *Area width is register setting value + 1clk.	50h
013Fh	[7:0]	POLYGON_OP_SPEED6	V sync	Polygon electronic first curtain shutter speed adjustment of Area 6. *Area width is register setting value + 1clk.	50h
0140h	[7:0]	POLYGON_OP_SPEED7	V sync	Polygon electronic first curtain shutter speed adjustment of Area 7. *Area width is register setting value + 1clk.	50h
0141h	[7:0]	POLYGON_OP_SPEED8	V sync	Polygon electronic first curtain shutter speed adjustment of Area 8. *Area width is register setting value + 1clk.	50h
0142h	[7:0]	POLYGON_OP_SPEED9	V sync	Polygon electronic first curtain shutter speed adjustment of Area 9. *Area width is register setting value + 1clk.	50h
0143h	[7:0]	POLYGON_OP_SPEED10	V sync	Polygon electronic first curtain shutter speed adjustment of Area 10. *Area width is register setting value + 1clk.	50h
0144h	[7:0]	POLYGON_OP_SPEED11	V sync	Polygon electronic first curtain shutter speed adjustment of Area 11. *Area width is register setting value + 1clk.	50h
0145h	[7:0]	POLYGON_OP_SPEED12	V sync	Polygon electronic first curtain shutter speed adjustment of Area 12. *Area width is register setting value + 1clk.	50h
0146h	[7:0]	POLYGON_OP_SPEED13	V sync	Polygon electronic first curtain shutter speed adjustment of Area 13. *Area width is register setting value + 1clk.	50h
0147h	[7:0]	POLYGON_OP_SPEED14	V sync	Polygon electronic first curtain shutter speed adjustment of Area 14. *Area width is register setting value + 1clk.	50h
0148h	[7:0]	POLYGON_OP_SPEED15	V sync	Polygon electronic first curtain shutter speed adjustment of Area 15. *Area width is register setting value + 1clk.	50h
0149h	[7:0]	POLYGON_OP_SPEED16	V sync	Polygon electronic first curtain shutter speed adjustment of Area 16. *Area width is register setting value + 1clk.	50h
014Ah	[7:0]	POLYGON_OP_SPEED17	V sync	Polygon electronic first curtain shutter speed adjustment of Area 17. *Area width is register setting value + 1clk.	50h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
014Bh	[7:0]	POLYGON_OP_SPEED18	V sync	Polygon electronic first curtain shutter speed adjustment of Area 18. *Area width is register setting value + 1clk.	50h
014Ch	[7:0]	POLYGON_OP_SPEED19	V sync	Polygon electronic first curtain shutter speed adjustment of Area 19. *Area width is register setting value + 1clk.	50h
014Dh	[7:0]	POLYGON_OP_SPEED20	V sync	Polygon electronic first curtain shutter speed adjustment of Area 20. *Area width is register setting value + 1clk.	50h
014Eh	[7:0]	POLYGON_OP_SPEED21	V sync	Polygon electronic first curtain shutter speed adjustment of Area 21. *Area width is register setting value + 1clk.	50h
014Fh	[7:0]	POLYGON_OP_SPEED22	V sync	Polygon electronic first curtain shutter speed adjustment of Area 22. *Area width is register setting value + 1clk.	50h
0150h	[7:0]	POLYGON_OP_SPEED23	V sync	Polygon electronic first curtain shutter speed adjustment of Area 23. *Area width is register setting value + 1clk.	50h
0151h	[7:0]	POLYGON_OP_SPEED24	V sync	Polygon electronic first curtain shutter speed adjustment of Area 24. *Area width is register setting value + 1clk.	50h
0152h	[7:0]	POLYGON_OP_SPEED25	V sync	Polygon electronic first curtain shutter speed adjustment of Area 25. *Area width is register setting value + 1clk.	50h
0153h	[7:0]	POLYGON_OP_SPEED26	V sync	Polygon electronic first curtain shutter speed adjustment of Area 26. *Area width is register setting value + 1clk.	50h
0154h	[7:0]	POLYGON_OP_SPEED27	V sync	Polygon electronic first curtain shutter speed adjustment of Area 27. *Area width is register setting value + 1clk.	50h
0155h	[7:0]	POLYGON_OP_SPEED28	V sync	Polygon electronic first curtain shutter speed adjustment of Area 28. *Area width is register setting value + 1clk.	50h
0156h	[7:0]	POLYGON_OP_SPEED29	V sync	Polygon electronic first curtain shutter speed adjustment of Area 29. *Area width is register setting value + 1clk.	50h
0157h	[7:0]	POLYGON_OP_SPEED30	V sync	Polygon electronic first curtain shutter speed adjustment of Area 30. *Area width is register setting value + 1clk.	50h
0158h	[7:0]	POLYGON_OP_SPEED31	V sync	Polygon electronic first curtain shutter speed adjustment of Area 31. *Area width is register setting value + 1clk.	50h
0159h	[7:0]	POLYGON_OP_SPEED32	V sync	Polygon electronic first curtain shutter speed adjustment of Area 32. *Area width is register setting value + 1clk.	50h
015Ah	[7:0]	POLYGON_OP_SPEED33	V sync	Polygon electronic first curtain shutter speed adjustment of Area 33. *Area width is register setting value + 1clk.	50h
015Bh	[7:0]	POLYGON_OP_SPEED34	V sync	Polygon electronic first curtain shutter speed adjustment of Area 34. *Area width is register setting value + 1clk.	50h
015Ch	[7:0]	POLYGON_OP_SPEED35	V sync	Polygon electronic first curtain shutter speed adjustment of Area 35. *Area width is register setting value + 1clk.	50h
015Dh	[7:0]	POLYGON_OP_SPEED36	V sync	Polygon electronic first curtain shutter speed adjustment of Area 36. *Area width is register setting value + 1clk.	50h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
015Eh	[7:0]	POLYGON_OP_SPEED37	V sync	Polygon electronic first curtain shutter speed adjustment of Area 37. *Area width is register setting value + 1clk.	50h
015Fh	[7:0]	POLYGON_OP_SPEED38	V sync	Polygon electronic first curtain shutter speed adjustment of Area 38. *Area width is register setting value + 1clk.	50h
0160h	[7:0]	POLYGON_OP_SPEED39	V sync	Polygon electronic first curtain shutter speed adjustment of Area 39. *Area width is register setting value + 1clk.	50h
0161h	[7:0]	POLYGON_OP_SPEED40	V sync	Polygon electronic first curtain shutter speed adjustment of Area 40. *Area width is register setting value + 1clk.	50h
0162h	[7:0]	POLYGON_OP_SPEED41	V sync	Polygon electronic first curtain shutter speed adjustment of Area 41. *Area width is register setting value + 1clk.	50h
0163h	[7:0]	POLYGON_OP_SPEED42	V sync	Polygon electronic first curtain shutter speed adjustment of Area 42. *Area width is register setting value + 1clk.	50h
0164h	[7:0]	POLYGON_OP_SPEED43	V sync	Polygon electronic first curtain shutter speed adjustment of Area 43. *Area width is register setting value + 1clk.	50h
0165h	[7:0]	POLYGON_OP_SPEED44	V sync	Polygon electronic first curtain shutter speed adjustment of Area 44. *Area width is register setting value + 1clk.	50h
0166h	[7:0]	POLYGON_OP_SPEED45	V sync	Polygon electronic first curtain shutter speed adjustment of Area 45. *Area width is register setting value + 1clk.	50h
0167h	[7:0]	POLYGON_OP_SPEED46	V sync	Polygon electronic first curtain shutter speed adjustment of Area 46. *Area width is register setting value + 1clk.	50h
0168h	[7:0]	POLYGON_OP_SPEED47	V sync	Polygon electronic first curtain shutter speed adjustment of Area 47. *Area width is register setting value + 1clk.	50h
0169h	[7:0]	POLYGON_OP_SPEED48	V sync	Polygon electronic first curtain shutter speed adjustment of Area 48. *Area width is register setting value + 1clk.	50h
016Eh	[7:0]	POLYGON_OP_VADR1	V sync	Last address setting of area 1 of the polygon electronic first curtain shutter.	03E8h
016Fh	[5:0]				
	[7:6]	—	—	—	0h
0170h	[7:0]	POLYGON_OP_VADR2	V sync	Last address setting of area 2 of the polygon electronic first curtain shutter.	07D0h
0171h	[5:0]				
	[7:6]	—	—	—	0h
0172h	[7:0]	POLYGON_OP_VADR3	V sync	Last address setting of area 3 of the polygon electronic first curtain shutter.	0BB8h
0173h	[5:0]				
	[7:6]	—	—	—	0h
0174h	[7:0]	POLYGON_OP_VADR4	V sync	Last address setting of area 4 of the polygon electronic first curtain shutter.	0BB9h
0175h	[5:0]				
	[7:6]	—	—	—	0h
0176h	[7:0]	POLYGON_OP_VADR5	V sync	Last address setting of area 5 of the polygon electronic first curtain shutter.	0BBAh
0177h	[5:0]				
	[7:6]	—	—	—	0h
0178h	[7:0]	POLYGON_OP_VADR6	V sync	Last address setting of area 6 of the polygon electronic first curtain shutter.	0BBBh
0179h	[5:0]				
	[7:6]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
017Ah	[7:0]	POLYGON_OP_VADR7	V sync	Last address setting of area 7 of the polygon electronic first curtain shutter.	0BBCh
017Bh	[5:0]				
	[7:6]	—	—	—	0h
017Ch	[7:0]	POLYGON_OP_VADR8	V sync	Last address setting of area 8 of the polygon electronic first curtain shutter.	0BBDh
017Dh	[5:0]				
	[7:6]	—	—	—	0h
017Eh	[7:0]	POLYGON_OP_VADR9	V sync	Last address setting of area 9 of the polygon electronic first curtain shutter.	0BBEh
017Fh	[5:0]				
	[7:6]	—	—	—	0h
0180h	[7:0]	POLYGON_OP_VADR10	V sync	Last address setting of area 10 of the polygon electronic first curtain shutter.	0BBFh
0181h	[5:0]				
	[7:6]	—	—	—	0h
0182h	[7:0]	POLYGON_OP_VADR11	V sync	Last address setting of area 11 of the polygon electronic first curtain shutter.	0BC0h
0183h	[5:0]				
	[7:6]	—	—	—	0h
0184h	[7:0]	POLYGON_OP_VADR12	V sync	Last address setting of area 12 of the polygon electronic first curtain shutter.	0BC1h
0185h	[5:0]				
	[7:6]	—	—	—	0h
0186h	[7:0]	POLYGON_OP_VADR13	V sync	Last address setting of area 13 of the polygon electronic first curtain shutter.	0BC2h
0187h	[5:0]				
	[7:6]	—	—	—	0h
0188h	[7:0]	POLYGON_OP_VADR14	V sync	Last address setting of area 14 of the polygon electronic first curtain shutter.	0BC3h
0189h	[5:0]				
	[7:6]	—	—	—	0h
018Ah	[7:0]	POLYGON_OP_VADR15	V sync	Last address setting of area 15 of the polygon electronic first curtain shutter.	0BC4h
018Bh	[5:0]				
	[7:6]	—	—	—	0h
018Ch	[7:0]	POLYGON_OP_VADR16	V sync	Last address setting of area 16 of the polygon electronic first curtain shutter.	0BC5h
018Dh	[5:0]				
	[7:6]	—	—	—	0h
018Eh	[7:0]	POLYGON_OP_VADR17	V sync	Last address setting of area 17 of the polygon electronic first curtain shutter.	0BC6h
018Fh	[5:0]				
	[7:6]	—	—	—	0h
0190h	[7:0]	POLYGON_OP_VADR18	V sync	Last address setting of area 18 of the polygon electronic first curtain shutter.	0BC7h
0191h	[5:0]				
	[7:6]	—	—	—	0h
0192h	[7:0]	POLYGON_OP_VADR19	V sync	Last address setting of area 19 of the polygon electronic first curtain shutter.	0BC8h
0193h	[5:0]				
	[7:6]	—	—	—	0h
0194h	[7:0]	POLYGON_OP_VADR20	V sync	Last address setting of area 20 of the polygon electronic first curtain shutter.	0BC9h
0195h	[5:0]				
	[7:6]	—	—	—	0h
0196h	[7:0]	POLYGON_OP_VADR21	V sync	Last address setting of area 21 of the polygon electronic first curtain shutter.	0BCAh
0197h	[5:0]				
	[7:6]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
0198h	[7:0]	POLYGON_OP_VADR22	V sync	Last address setting of area 22 of the polygon electronic first curtain shutter.	BCBh
0199h	[5:0]				
	[7:6]	—	—	—	0h
019Ah	[7:0]	POLYGON_OP_VADR23	V sync	Last address setting of area 23 of the polygon electronic first curtain shutter.	0BCCh
019Bh	[5:0]				
	[7:6]	—	—	—	0h
019Ch	[7:0]	POLYGON_OP_VADR24	V sync	Last address setting of area 24 of the polygon electronic first curtain shutter.	0BCDh
019Dh	[5:0]				
	[7:6]	—	—	—	0h
019Eh	[7:0]	POLYGON_OP_VADR25	V sync	Last address setting of area 25 of the polygon electronic first curtain shutter.	0BCEh
019Fh	[5:0]				
	[7:6]	—	—	—	0h
01A0h	[7:0]	POLYGON_OP_VADR26	V sync	Last address setting of area 26 of the polygon electronic first curtain shutter.	0BCFh
01A1h	[5:0]				
	[7:6]	—	—	—	0h
01A2h	[7:0]	POLYGON_OP_VADR27	V sync	Last address setting of area 27 of the polygon electronic first curtain shutter.	0BD0h
01A3h	[5:0]				
	[7:6]	—	—	—	0h
01A4h	[7:0]	POLYGON_OP_VADR28	V sync	Last address setting of area 28 of the polygon electronic first curtain shutter.	0BD1h
01A5h	[5:0]				
	[7:6]	—	—	—	0h
01A6h	[7:0]	POLYGON_OP_VADR29	V sync	Last address setting of area 29 of the polygon electronic first curtain shutter.	0BD2h
01A7h	[5:0]				
	[7:6]	—	—	—	0h
01A8h	[7:0]	POLYGON_OP_VADR30	V sync	Last address setting of area 30 of the polygon electronic first curtain shutter.	0BD3h
01A9h	[5:0]				
	[7:6]	—	—	—	0h
01AAh	[7:0]	POLYGON_OP_VADR31	V sync	Last address setting of area 31 of the polygon electronic first curtain shutter.	0BD4h
01ABh	[5:0]				
	[7:6]	—	—	—	0h
01ACh	[7:0]	POLYGON_OP_VADR32	V sync	Last address setting of area 32 of the polygon electronic first curtain shutter.	0BD5h
01ADh	[5:0]				
	[7:6]	—	—	—	0h
01AEh	[7:0]	POLYGON_OP_VADR33	V sync	Last address setting of area 33 of the polygon electronic first curtain shutter.	0BD6h
01AFh	[5:0]				
	[7:6]	—	—	—	0h
01B0h	[7:0]	POLYGON_OP_VADR34	V sync	Last address setting of area 34 of the polygon electronic first curtain shutter.	0BD7h
01B1h	[5:0]				
	[7:6]	—	—	—	0h
01B2h	[7:0]	POLYGON_OP_VADR35	V sync	Last address setting of area 35 of the polygon electronic first curtain shutter.	0BD8h
01B3h	[5:0]				
	[7:6]	—	—	—	0h
01B4h	[7:0]	POLYGON_OP_VADR36	V sync	Last address setting of area 36 of the polygon electronic first curtain shutter.	0BD9h
01B5h	[5:0]				
	[7:6]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01B6h	[7:0]	POLYGON_OP_VADR37	V sync	Last address setting of area 37 of the polygon electronic first curtain shutter.	0BDAh
01B7h	[5:0]				
	[7:6]	—	—	—	0h
01B8h	[7:0]	POLYGON_OP_VADR38	V sync	Last address setting of area 38 of the polygon electronic first curtain shutter.	0BDBh
01B9h	[5:0]				
	[7:6]	—	—	—	0h
01BAh	[7:0]	POLYGON_OP_VADR39	V sync	Last address setting of area 39 of the polygon electronic first curtain shutter.	0BDCh
01BBh	[5:0]				
	[7:6]	—	—	—	0h
01BCh	[7:0]	POLYGON_OP_VADR40	V sync	Last address setting of area 40 of the polygon electronic first curtain shutter.	0BDDh
01BDh	[5:0]				
	[7:6]	—	—	—	0h
01BEh	[7:0]	POLYGON_OP_VADR41	V sync	Last address setting of area 41 of the polygon electronic first curtain shutter.	0BDEh
01BFh	[5:0]				
	[7:6]	—	—	—	0h
01C0h	[7:0]	POLYGON_OP_VADR42	V sync	Last address setting of area 42 of the polygon electronic first curtain shutter.	0BDFh
01C1h	[5:0]				
	[7:6]	—	—	—	0h
01C2h	[7:0]	POLYGON_OP_VADR43	V sync	Last address setting of area 43 of the polygon electronic first curtain shutter.	0BE0h
01C3h	[5:0]				
	[7:6]	—	—	—	0h
01C4h	[7:0]	POLYGON_OP_VADR44	V sync	Last address setting of area 44 of the polygon electronic first curtain shutter.	0BE1h
01C5h	[5:0]				
	[7:6]	—	—	—	0h
01C6h	[7:0]	POLYGON_OP_VADR45	V sync	Last address setting of area 45 of the polygon electronic first curtain shutter.	0BE2h
01C7h	[5:0]				
	[7:6]	—	—	—	0h
01C8h	[7:0]	POLYGON_OP_VADR46	V sync	Last address setting of area 46 of the polygon electronic first curtain shutter.	0BE3h
01C9h	[5:0]				
	[7:6]	—	—	—	0h
01CAh	[7:0]	POLYGON_OP_VADR47	V sync	Last address setting of area 47 of the polygon electronic first curtain shutter.	0BE4h
01CBh	[5:0]				
	[7:6]	—	—	—	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01CCh	[1:0]	POLYGON_OP_DCMS1	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area1 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS2	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area2 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS3	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area3 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS4	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area4 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01CDh	[1:0]	POLYGON_OP_DCMS5	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area5 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS6	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area6 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS7	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area7 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS8	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area8 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01CEh	[1:0]	POLYGON_OP_DCMS9	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area9 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS10	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area10 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS11	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area11 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS12	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area12 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01CFh	[1:0]	POLYGON_OP_DCMS13	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area13 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS14	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area14 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS15	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area15 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS16	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area16 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D0h	[1:0]	POLYGON_OP_DCMS17	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area17 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS18	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area18 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS19	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area19 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS20	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area20 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D1h	[1:0]	POLYGON_OP_DCMS21	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area21 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS22	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area22 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS23	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area23 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS24	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area24 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01D2h	[1:0]	POLYGON_OP_DCMS25	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area25 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS26	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area26 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS27	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area27 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS28	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area28 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D3h	[1:0]	POLYGON_OP_DCMS29	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area29 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS30	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area30 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS31	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area31 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS32	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area32 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D4h	[1:0]	POLYGON_OP_DCMS33	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area33 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS34	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area34 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS35	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area35 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS36	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area36 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01D5h	[1:0]	POLYGON_OP_DCMS37	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area37 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS38	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area38 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS39	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area39 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS40	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area40 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D6h	[1:0]	POLYGON_OP_DCMS41	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area41 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS42	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area42 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS43	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area43 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS44	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area44 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
01D7h	[1:0]	POLYGON_OP_DCMS45	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area45 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[3:2]	POLYGON_OP_DCMS46	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area46 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[5:4]	POLYGON_OP_DCMS47	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area47 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h
	[7:6]	POLYGON_OP_DCMS48	V sync	Parallel row reset function of the polygon electronic first curtain shutter at Area48 0h: Sequential reset, 1h:2-row parallel reset, (2h: Setting prohibited) 3h: 4-row parallel reset	0h

Address		Name	Reflection timing	Description	Default value
Byte	Bits				
01D8h	[1:0]	—	—	—	0h
	[2]	HCROP_WIDTH_EN	V sync	Horizontal cropping output width setting enable	0h
	[7:3]	—	—	—	00h
01DDh	[7:0]	HCROP_WIDTH	V sync	Horizontal cropping output width setting	0000h
01DEh	[6:0]				
	[7]	—	—	—	0h
01EEh	[0]	PWR_AUTO	Immediately	Control automatic power-on sequence See “Power-ON Sequence”. When setting “1h”, automatic power-on sequence is started. It is prohibited to set “0h” after starting automatic sequence by setting “1h”.	0h
	[1]	—	—	—	0h
	[2]	SLP_CTRL	Immediately	See “Long Time Exposure”	0h
	[7:3]	—	—	—	00h
01F0h	[7:0]	PLL_AD_STB	Immediately	High speed AD setting register See “High Speed AD Mode” for detail	00h
0366h	[7:0]	PLL_AD_SETTING	Immediately	High speed AD setting register See “High Speed AD Mode” for detail	0Ch

Description of Each Register

Standby Control: STANDBY

This sets the standby mode that stops sensor operation. Only the communication interface remains active, so register settings can be made. This register is used with SLP_CTRL register when standby sequence. See “Standby Mode” for detail.

STANDBY register	Description of operation
0h	Normal operation
1h	Standby mode

Sensor Startup Control: WAKEUP

The sensor is set to the pre-startup stop mode by setting XCLR Low. Set the WAKEUP register to “1” to start image storage and readout drive operation. Once started, drive operation continues even if WAKEUP is set to “0”. To return to the pre-startup stop mode again, input Low to XCLR.

WAKEUP register	Description of operation
0h → 1h	Cancels pre-startup stop mode

Readout Drive Mode Control: MODE

MODE register switches readout drive mode of the pixel output area as shown in the table below. It becomes valid at the next XVS input after setting the register.

MODE register	SMD register	Description of operation
00h	0h or 1h	All-pixel scan readout mode
01h	0h or 1h	All-pixel scan readout mode 2-parallel ADC readout
02h	—	—
03h	0h	All-pixel scan readout mode digital overlap drive
04h	—	—
05h	0h	Vertical 2/2-line and horizontal 2/2-line weighted binning readout mode
06h	0h	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode
07h	0h	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode
08h	—	—
09h	—	—
0Ah	0h	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode digital overlap drive
0Bh	0h	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode digital overlap drive
0Ch	0h	Vertical 1/5 subsampling, horizontal 3 weighted binning readout mode
0Dh	0h	Vertical 3/5 subsampling binning, horizontal 3 weighted binning readout mode
0Eh	0h	Vertical 1/7 subsampling, horizontal 3 weighted binning readout mode
0Fh	0h	Vertical 3/7 subsampling binning, horizontal 3 weighted binning readout mode
10h	0h	Vertical 1/9 subsampling, horizontal 3 weighted binning readout mode
11h	0h	Vertical 3/9 subsampling binning, horizontal 3 weighted binning readout mode
12h	0h	Vertical 1/13 subsampling, horizontal 3 weighted binning readout mode
13h	0h	Vertical 3/13 subsampling binning, horizontal 3 weighted binning readout mode
14h	0h	Vertical 1/25 subsampling, horizontal 3 weighted binning readout mode
15h	0h	Vertical 3/25 subsampling binning, horizontal 3 weighted binning readout mode
16 to 1F	—	—

Note) When changing the mode, other registers must also be changed.

Control Data: SMD

SMD register switches the sensor shutter operation. The register setting becomes valid at the next XVS input after setting the register. This register is required to be set linked with readout mode.

SMD register	Description of operation
0h	Rolling shutter
1h	Global reset shutter

Control Data: MSMD

This register sets whether to reset all pixels at once or to perform pixel reset operation by electronic first curtain shutter operation in still image mode. This setting is valid only when SMD = “1h”

MSMD register	Description of operation
0h	All-pixel simultaneous reset mode
1h	Electronic first curtain shutter mode

Control Data: OPMODE

This register sets the scanning mode of the electronic first curtain shutter. This setting is valid only when SMD = “1h” and MSMD = “1h”.

OPMODE register	Description of operation
0h	Polygon electronic first curtain shutter
1h	Non-linear electronic first curtain shutter

Control Data: VSHT_DIR

This register sets the scanning direction of electronic first curtain shutter.

VSHT_DIR register	Description of operation
0h	Normal Direction: Area 1 → Area 48 (physical address small → large)
1h	Inverted Direction Area 48 → Area 1 (physical address large → small)

Control Data: SSBRK

When imaging operation in rolling shutter mode, slow shutter break can be set by the SSBRK register. When SSBRK is set to “1h” during slow shutter operation, at the next XVS the image integrated to the time is output.
The next slow shutter cannot be stopped by keeping SSBRK at “1h”. To stop slow shutter again, SSBRK must be returned to “0h” and then set to “1h” again.

Control Data: LESS_SHUT, LESS_SHUT_DOL1, LESS_SHUT_DOL2

This makes the shutter less setting in rolling shutter operation mode (when SMD is set “0h”).
LESS_SHUT register is for normal readout drive, LESS_SHUT_DOL1 register is for digital overlap drive at short time exposure frame and LESS_SHUT_DOL2 register is digital overlap drive at long time exposure frame.

LESS_SHUT register LESS_SHUT_DOL1 register LESS_SHUT_DOL2 register	Description of operation
0h	Shutter operation performed
1h	Shutter operation not performed (fixed to 1V integration time)

Control Data: GLB4FLD

This register sets the global 4 field readout drive when SMD = “1h”.
See “Global 4 Field Readout Function” section for detail

GLB4FLD register	Description of operation
0h	Normal operation
1h	Global 4 field readout drive

Control Data: WND

WND register enables the window readout function. The register setting becomes valid at the next XVS input after setting the register. See the description below for details.

WND register	Description of operation
0h	Window readout function OFF
1h	Window readout function ON Black dummy (variable area) → VOB without sensor (variable area) → VOB with sensor → Effective pixels
2h,3h	Setting prohibited

Control Data: WIN_START

WIN_START register sets the window readout start line. Readout is performed from the line designated by WIN_START. This register setting value has restrictions for each operating mode. See the description below for details.

Control Data: WIN_WIDTH

WIN_WIDTH register sets the number of lines in window readout mode. See the description below for details.

Control Data: SVR

This register in combination with SPL sets the integration time in XVS signal units. The register setting becomes valid at the next XVS input after setting the register. The setting becomes invalid in global reset shutter mode (SMD = 1).

Control Data: SPL

SPL register sets the integration start timing in XVS signal units. Always ensure the relationship of SPL ≤ SVR. The register setting becomes valid at the next XVS input after setting the register. This setting is invalid in global reset shutter mode (SMD = 1).

Control Data: SHR, SHR_DOL1, SHR_DOL2

SHR register sets the integration start timing in XHS signal units. The register setting becomes valid at the next XVS input after setting the register. Integration starts after SHR (or 2 × SHR) number of XHS pulses are input after XVS input. In global reset shutter mode, pixel integration operation starts for all pixels at once. In rolling shutter mode, pixel integration operation starts for successive pixels from the first H. When SHR (or 2 × SHR) which is larger than the XHS number within the 1 V period, is set in the rolling shutter drive mode, the shutter-less drive (1 V exposure fixed) is performed. SHR_DOL1 and SHR_DOL2 registers are for digital overlap readout mode.

Control Data: READ_START_DOL1

This register sets the read start position of short time exposure in digital overlap drive mode.

Control Data: SINT

This register sets reset timing of electronic first curtain shutter in combination with the SHR.
See “Electronic First Curtain Shutter Function”.

Control Data: VBLK_WIDTH

VBLK_WIDTH sets the number of lines for Front V blank.
The setting value must be 4 or more and even number. Recommended value is 06h.

Control Data: BK_WIDTH

BK_WIDTH sets the number of lines for black dummy area.
The setting value must be even number.

Control Data: OPBN_WIDTH

OPBN_WIDTH register sets the number of lines for VOB area without sensor.
The setting value must be even number.

Control Data: APGC_N, APGC_S, APGC_LT_N, APGC_LT_S, APGC_ST_N, APGC_ST_S, APGC_ADD

APGC_N, APGC_S set the analog gain. It becomes valid at the next XVS input after setting the register.
See “Gain Setting” for detail.
APGC_LT_N, APGC_LT_S, APGC_ST_N and APGC_ST_S registers are for digital overlap drive mode.
And change the setting value of “APGC_ADD” register according to APGC setting value.

Control Data: DGAIN

DGAIN register sets digital gain by bits shift. This register sets every color channel to the same gain.

DGAIN register	Description of operation
0h	Digital gain OFF
1h	Digital gain 6 dB
2h	Digital gain 12 dB
3h	Digital gain 18 dB
4h	Digital gain 24 dB
5h	Digital gain 30 dB
6h	Digital gain 36 dB
7h	Setting prohibited

Control Data: BLKLEVEL_N, BLKLEVEL_S

BLKLEVEL_N and BLKLEVEL_S registers set the black level. The relation between the setting and black level to be output differs according to drive mode. See “Black Level Setting” of each mode.

Control Data: CLPOFF

CLPOFF register stops the clamp operation. Set to 1h to stop the clamp function.

CLPOFF register	Description of operation
0h	Clamp operation ON
1h	Clamp operation OFF

Control Data: CLPBKOFF

CLPBKOFF register stops the black dummy clamp. Set to 1h to stop the clamp function.

CLPBKOFF register	Description of operation
0h	Black dummy clamp ON
1h	Black dummy clamp OFF

Control Data: CLPOPBOFF

CLPOPBOFF register stops the VOB clamp. Set to 1h to stop the clamp function.

CLPOPBOFF register	Description operation
0h	VOB clamp ON
1h	VOB clamp OFF

Control Data: CLPBK_VST

CLPBK_VST register sets the black dummy clamp start line. The first black dummy line is defined as “0”, and clamp operation starts from the line designated by CLPBK_VST.

Control Data: CLPBK_V

CLPBK_V sets the black dummy clamp period. Clamp operation is performed for the number of lines designated by CLPBK_V.

Control Data: CLPOB_VST

CLPOB_VST sets the VOB clamp start line. The first VOB line is defined as “0”, and clamp operation starts from the line designated by CLPOB_VST.

Control Data: CLPOB_V

CLPOB_V sets the VOB clamp period. Clamp operation is performed for the number of lines which is set by this register.

Control Data: CLPAPGC

CLPAPGC is clamp gain setting register. See “Gain Setting” for detail.

Control Data: SDO_ACT

SDO_ACT register change SDO output state.

SDO_ACT register	Description of operation
0h	SDO pin: Hi-Z
1h	SDO pin: register data output

Control Data: HCROP_START_EN

HCROP_START_EN register enables/disables horizontal cropping start position setting register.

HCROP_START_EN register	Description of operation
0h	Horizontal cropping start position setting disable
1h	Horizontal cropping start position setting enable

Control Data: HCROP_START

HCROP_START register sets the horizontal freely cropping start position.
See the description below for details.

Control Data: HCROP_WIDTH_EN

HCROP_WIDTH_EN register enables/disables horizontal cropping width setting register.

HCROP_WIDTH_EN register	Description of operation
0h	Horizontal cropping output width setting disable
1h	Horizontal cropping output width setting enable

Control Data: HCROP_WIDTH

HCROP_START register sets the horizontal freely cropping width. See the description below for details.

Control Data: FIXDTON

FIXDTON register enables/disables fixed pattern test mode.

FIXDTON register	Description of operation
0h	Fixed pattern test mode : OFF
1h	Fixed pattern test mode : ON

Control data: FIXDTSEL

This register selects patterns for fixed pattern test mode. See the detailed description hereafter.

FIXDTSEL register	Description of operation
0h	Shading mode
1h	Color bars mode
2h	Each color channel fixed pattern mode

Control data: FIXDTSFT

This register selects the increment value each column and row when in shading mode of fix pattern mode.

FIXDTSFT register	Description of operation
0h	Increment value: 1d
1h	Increment value: 2d
2h	Increment value: 4d
3h	Increment value: 8d

Control Data: COLORBARSEL

COLORBARSEL register switches direction of color bars in color bars fixed pattern test mode.

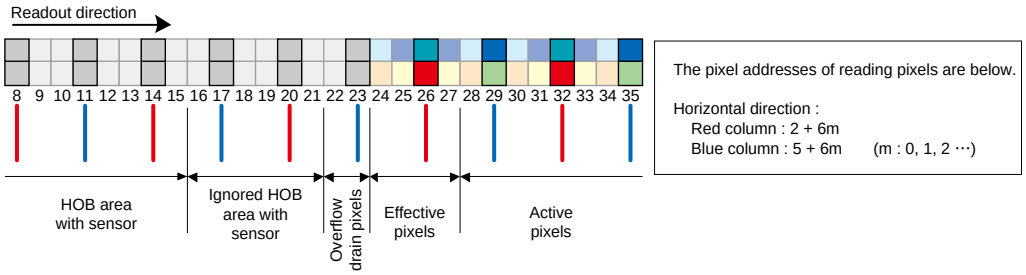
COLORBARSEL register	Description of operation
0h	Vertical
1h	Horizontal

Control data: H3SEL

In MODE 6, 7, 10 to 21, this register switches horizontal binning subsampling drive method from horizontal 3 weighted binning to horizontal 1/3 subsampling which is low power consumption movie mode. It becomes valid at the next XVS input after setting the register.

H3SEL register	Description of operation
0h	Horizontal 3 weighted binning
1h	Horizontal 1/3 subsampling

When Horizontal 1/3 subsampling drive, the pixel addresses of readout in horizontal direction are below.



Control Data: POLYGON_OP_SPEEDxx (xx=1,2,3,…,48)

This register changes the polygon electronic first curtain shutter scanning speed in each area.
The exposure time of the pixels in each area can be aligned by adjusting the scanning time set by the register POLYGON_OP_SPEEDxx[7:0] (xx=1,2,3,…,48) to match the (second curtain) mechanical shutter scanning speed.
See “Polygon Electronic First Curtain Shutter”.

Control Data: POLYGON_OP_VADRxx (xx=1,2,3,…,47)

This register sets the last address value of each area obtained by dividing the vertical area to 48 groups when polygon electronic first curtain shutter. The width of each area is freely-selected.
See “Polygon Electronic First Curtain Shutter”.

Control Data: POLYGON_OP_DCMSxx (xx=1,2,3,…,48)

This register sets the parallel row reset function of polygon electronic first curtain shutter area.

POLYGON_OP_DCMSxx register	Description of operation
0h	Sequential reset
1h	2-row parallel reset
2h	Setting prohibited
3h	4-row parallel reset

Control Data: PWR_AUTO

This register controls automatic power-on sequence. Please refer to the “Power-On Sequence”.
When setting “1h”, automatic power-on sequence is started. It is prohibited to set “0h” after starting automatic sequence by setting “1h”.

Control Data: SLP_CTRL

Please refer to the “Long Time Exposure”.

Control Data: PLL_AD_STB, PLL_AD_SETTING

Please refer to the “High Speed AD Mode”.

Register related to SLVS- EC

Payload Data ECC, CRC Setting

The registers ECC_EN (address 0113h, bit [5:4]) can set ECC option for payload data error correction. The registers CRC_EN (address 0113h, bit [0]) can set CRC option for data transfer error correction. ECCEN and CRCEN cannot be used together. And, change ECCEN or CRCEN value during initialize communication of standby cancel sequence. See “SLVS-EC Specification Version 1.2” for details of payload data, ECC and CRC.

Control Data : CRC_EN

CRC_EN	Description
0h	Without CRC insertion into Packet Footer
1h	With CRC insertion into packet footer ECC option and CRCEN option cannot be used together

Control Data : ECC_EN

ECC_EN	Description
0h	Without ECC insertion.
1h	With ECC [parity 2 byte]. ECC option and CRCEN option cannot be used together
2h	With ECC [parity 4 byte]. ECC option and CRCEN option cannot be used together
3h	Prohibited

Attribute Register and PHY Control Code

Correspondence of attribute register and PHY control code in “SLVS-EC Specification Version 1.2” to this sensor’s registers are shown below.

Attribute Register

Attribute Register	Register name	Address [bit]	Description
Sync Symbol	PHY Control Code : see Sync Code		
Deskew Symbol	PHY Control Code : see Deskew Code		
Standby Symbol	PHY Control Code : see Standby Code		
Sync Length	SYNC_LENGTH	0116h[7:0], 0117h[7:0], 0118h[7:0]	Sync code repeat count in training sequence. Default: 007FFFh Setting range: 000001h to FFFFFFh
Deskew Length	DESKEW_LENGTH	0119h[7:0]	Deskew code repeat count in training sequence. Default: 10h Setting range: 01h to FFh
Standby Length	STANDBY_LENGTH	011Bh[7:0]	Standby code repeat count in standby sequence. Default: 10h Setting range: 03h to FFh
Deskew Interval	DESKEW_INTERVAL	011Ah[7:0]	Idle code repeat count between deskew code in training sequence. Default: 10h Setting range: 04h to FCh Setting value must be a multiple of 4.
Initial Length	INIT_LENGTH	0115h[4:0]	Low output period during mode change and initialization. Default: 0Ah Setting range: 00h to 10h
Idle Code	PHY Control Code : see Idle Code		

PHY Control Code

PHY Control Code	Register name	Address[bit]	Description	8b10b symbol configuration			
Idle Code	IDLE_CODE1	0120h[7:0]	Any symbol	IDLE CODE1 (def D.00.0)	IDLE CODE2 (def D.00.0)	IDLE CODE3 (def D.00.0)	IDLE CODE4 (def D.00.0)
		0121h[0]	0:D character 1:K character				
	IDLE_CODE2	0122h[7:0]	Any symbol				
		0123h[0]	0:D character 1:K character				
	IDLE_CODE3	0124h[7:0]	Any symbol				
		0125h[0]	0:D character 1:K character				
	IDLE_CODE4	0126h[7:0]	Any symbol				
		0127h[0]	0:D character 1:K character				
Start Code	—	—	—	K.28.5	K.27.7	K.28.2	K.27.7
End Code	—	—	—	K.28.5	K.29.7	K.30.7	K.29.7
Pad Code	—	—	—	K.23.7	K.28.4	K.28.6	K.28.3
Sync Code	SYNC_SYMBOL	011Ch[7:0]	Any symbol	K.28.5	SYNC CODE (def D.10.5)	←	←
		011Dh[0]	0:D character 1:K character				
Deskew Code	DESKEW_SYMBOL	011Eh[7:0]	Any symbol	K.28.5	DESKEW CODE (def D.00.3)	←	←
		011Fh[0]	0:D character 1:K character				
Standby Code	STANDBY_SYMBOL	012Ah[7:0]	Any symbol	K.28.5	STBY CODE (def D.03.0)	←	←
		012Bh[0]	0:D character 1:K character				

Readout Drive Mode

The table below describes the readout drive modes that can be used to operate this sensor.
See the following section for the detailed output format of each mode.

Description of Readout Drive Mode

Table. Description of Readout Drive Modes

Mode No.		Readout mode	ADC	Word length	Mode description
0	-a	All-pixel readout mode	16 bits	16 bits	All pixels are read out. This mode can be used together with the global reset shutter function according to the SMD register setting.
	-b		14 bits	14 bits	
	-c		12 bits	12 bits	
	-e		11 bits	10 bits	
1	-a	All-pixel readout mode 2-parallel ADC readout	16 bits	16 bits	All pixels are read out. This mode can be used together with the global reset shutter function according to the SMD register setting.
	-b		14 bits	14 bits	
	-c		12 bits	12 bits	
3	-a	All-pixel readout mode digital overlap drive	16 bits	16 bits	All pixels are read out by digital overlap drive. Two frames of different exposure time are alternately output per line.
	-b		14 bits	14 bits	
	-c		12 bits	12 bits	
	-e		11 bits	10 bits	
5	-c	Vertical 2/2-line and horizontal 2/2-line weighted binning readout mode	12 bits	12 bits	2 of every 2 vertical lines and 2 of every 2 horizontal lines for pixels at the same color position are weighted binning and readout.
6	-c	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode	12 bits	12 bits	1 of every 3 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
7	-c	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode	12 bits	12 bits	3 of every 3 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
10	-c	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode digital overlap drive	12 bits	12 bits	1 of every 3 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout by digital overlap drive. Two frames of different exposure time are alternately output per line.
11	-c	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode digital overlap drive	12 bits	12 bits	3 of every 3 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout by digital overlap drive. Two frames of different exposure time are alternately output per line.
12	-d	Vertical 1/5 subsampling, horizontal 3 weighted binning readout mode	11 bits	12 bits	1 of every 5 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
13	-d	Vertical 3/5 subsampling binning, horizontal 3 weighted binning readout mode	11 bits	12 bits	3 of every 5 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
14	-d	Vertical 1/7 subsampling, horizontal 3 weighted binning readout mode	11 bits	12 bits	1 of every 7 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
15	-d	Vertical 3/7 subsampling binning, horizontal 3 weighted binning readout mode	11 bits	12 bits	3 of every 7 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.

Mode No.		Readout mode	ADC	Word length	Mode description
16	-d	Vertical 1/9 subsampling, horizontal 3 weighted binning readout mode	11 bits	12 bits	1 of every 9 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
17	-d	Vertical 3/9 subsampling binning, horizontal 3 weighted binning readout mode	11 bits	12 bits	3 of every 9 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
18	-d	Vertical 1/13 subsampling, horizontal 3 weighted binning readout mode	11 bits	12 bits	1 of every 13 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
19	-d	Vertical 3/13 subsampling binning, horizontal 3 weighted binning readout mode	11 bits	12 bits	3 of every 13 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
20	-d	Vertical 1/25 subsampling, horizontal 3 weighted binning readout mode	11 bits	12 bits	1 of every 25 vertical lines is subsampled and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.
21	-d	Vertical 3/25 subsampling binning, horizontal 3 weighted binning readout mode	11 bits	12 bits	3 of every 25 vertical lines at the same color position are averaged and 3 of every 3 horizontal lines for pixels at the same color position are weighted binning and readout.

Imaging Conditions in Each Readout Drive Mode

Table. Conditions for Readout Mode

Mode No.		Readout mode	Number of active horizontal pixels	Number of active vertical pixels	Number of OB without sensor lines *1	1XHS period [number of INCK] *2 *3	1V period [number of XHS] *3	Max frame rate [frame/s]
0	-a	All-pixel readout mode	6244	4168	10	2496	4224	6.82
	-b					1042	4224	16.35
	-c					454	4224	37.54
	-e					352	4224	48.42
1	-a	All-pixel readout mode 2-parallel ADC readout	6244	4168	10	4990	4222	3.41
	-b					2082	4222	8.19
	-c					906	4222	18.82
3	-a	All-pixel readout mode digital overlap drive	6244	4168	10	2496	8468	3.40
	-b					1042	8468	8.15
	-c					454	8468	18.72
	-e					352	8468	24.15
5	-c	Vertical 2/2-line and horizontal 2/2-line weighted binning readout mode	3122	2084	4	906	2116	37.55
6	-c	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode	2080	1388	4	454	1418	111.84
7	-c	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode	2080	1386	4	454	1416	111.99
10	-c	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode digital overlap drive	2080	1388	4	454	2856	55.52
11	-c	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode digital overlap drive	2080	1386	4	454	2856	55.52
12	-d	Vertical 1/5 subsampling, horizontal 3 weighted binning readout mode	2080	832	4	344	854	245.08
13	-d	Vertical 3/5 subsampling binning, horizontal 3 weighted binning readout mode	2080	832	4	344	854	245.08
14	-d	Vertical 1/7 subsampling, horizontal 3 binning weighted readout mode	2080	594	4	344	616	339.77
15	-d	Vertical 3/7 subsampling binning, horizontal 3 weighted binning readout mode	2080	594	4	344	616	339.77
16	-d	Vertical 1/9 subsampling, horizontal 3 weighted binning readout mode	2080	462	4	344	484	432.44
17	-d	Vertical 3/9 subsampling binning, horizontal 3 weighted binning readout mode	2080	462	4	344	484	432.44
18	-d	Vertical 1/13 subsampling, horizontal 3 weighted binning readout mode	2080	320	4	344	342	611.99
19	-d	Vertical 3/13 subsampling binning, horizontal 3 weighted binning readout mode	2080	319	4	344	342	611.99

Mode No.		Readout mode	Number of active horizontal pixels	Number of active vertical pixels	Number of OB without sensor lines *1	1XHS period [number of INCK] *2 *3	1V period [number of XHS] *3	Max frame rate [frame/s]
20	-d	Vertical 1/25 subsampling, horizontal 3 weighted binning readout mode	2080	166	4	344	188	1113.31
21	-d	Vertical 3/25 subsampling binning, horizontal 3 weighted binning readout mode	2080	164	4	344	186	1125.28

*1 Number of OB without sensor line can be set by OPBN_WIDTH register.
*2 Number of INCK pulse required to output the data for one line.
*3 The number of XHS pulse per 1V period and number of INCK per 1XHS must be even number in every mode.

Note)
The values in the table are the minimum 1XHS and 1V cycle values. When XHS and XVS have longer intervals than these, the sensor outputs a blank code signal. The data is output once per 1 XHS inputs.
The V period and the frame rate shown above is in the case that “Number of OB without sensor line” is the value in the above table and VBLK_WIDTH = 6h and BK_WIDTH = 0h.
The maximum frame rate varies depending on the number of readout lines in window readout mode.

Table. Output Conditions for Each Drive Mode

Readout mode (branch mode No.)	Output format	Word length	Min.	Max.
AD 16 bits, 16 bits word length mode (-a)	RAW16	16 bits	0000h	FFFFh
AD 14 bits, 14 bits word length mode (-b)	RAW14	14 bits	0000h	3FFFh
AD 12 bits, 12 bits word length mode (-c)	RAW12	12 bits	000h	FFFh
AD 11 bits, 12 bits word length mode (-d)	RAW12	12 bits	000h	FFEh
AD 11 bits, 10 bits word length mode (-e)	RAW10	10 bits	000h	3FFh

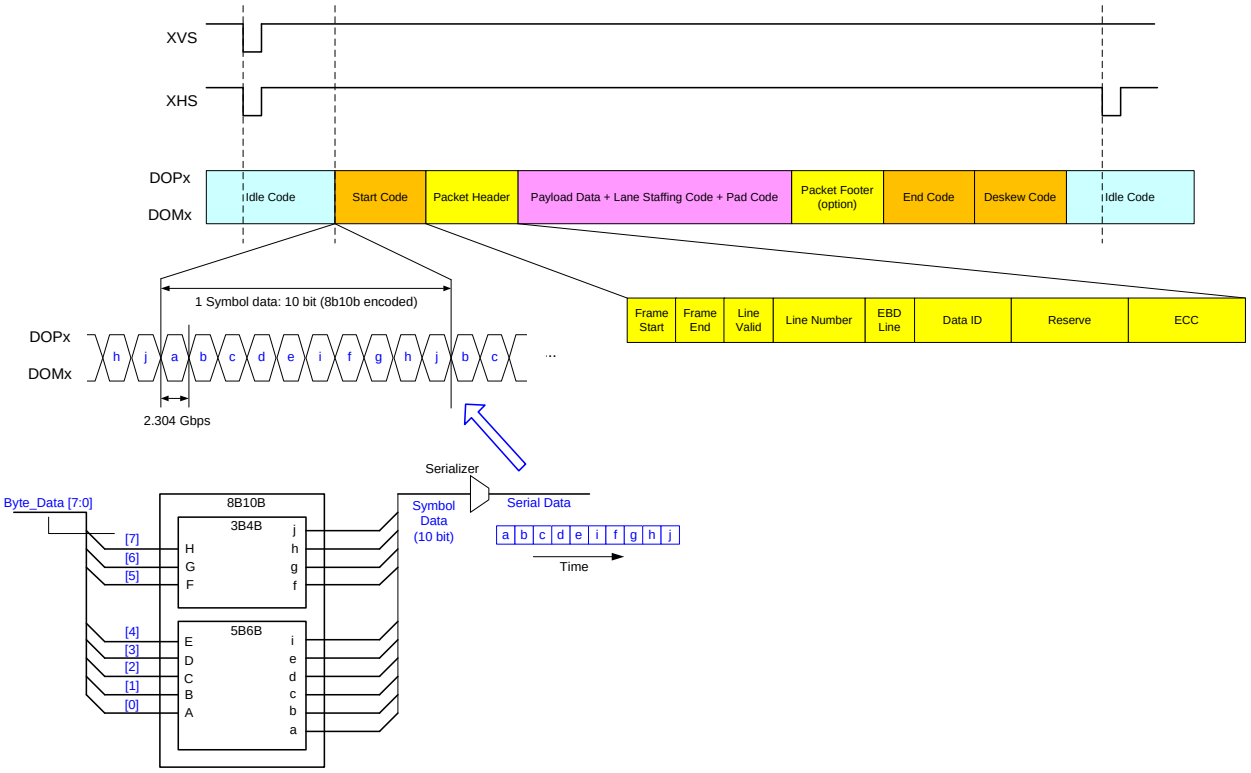
Image Data output Format

Line Format and Frame Format (Sync Signals and Data Output Timing)

The format of each line and each frame of this sensor are described below.
The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals. Timing control is performed at the falling edge of both the XVS and XHS signals.

Line Format

The figure below shows the line format of each line. 1 Symbol consists of 10 bits regardless of readout drive mode. Refer to “SLVS-EC Specification Version 1.2” for detail.



Frame Format

In this section the frame formats in following cases are described.

1. Normal frame
2. Digital overlap drive frame
3. Global 4 field readout frame
4. Invalid frame (with training sequence)
5. Invalid frame (without training sequence)

1. Normal frame

As an example, the figure below shows XVS timing and contents of the header in each line in the case of readout mode No. 0, All-pixel scan readout mode.

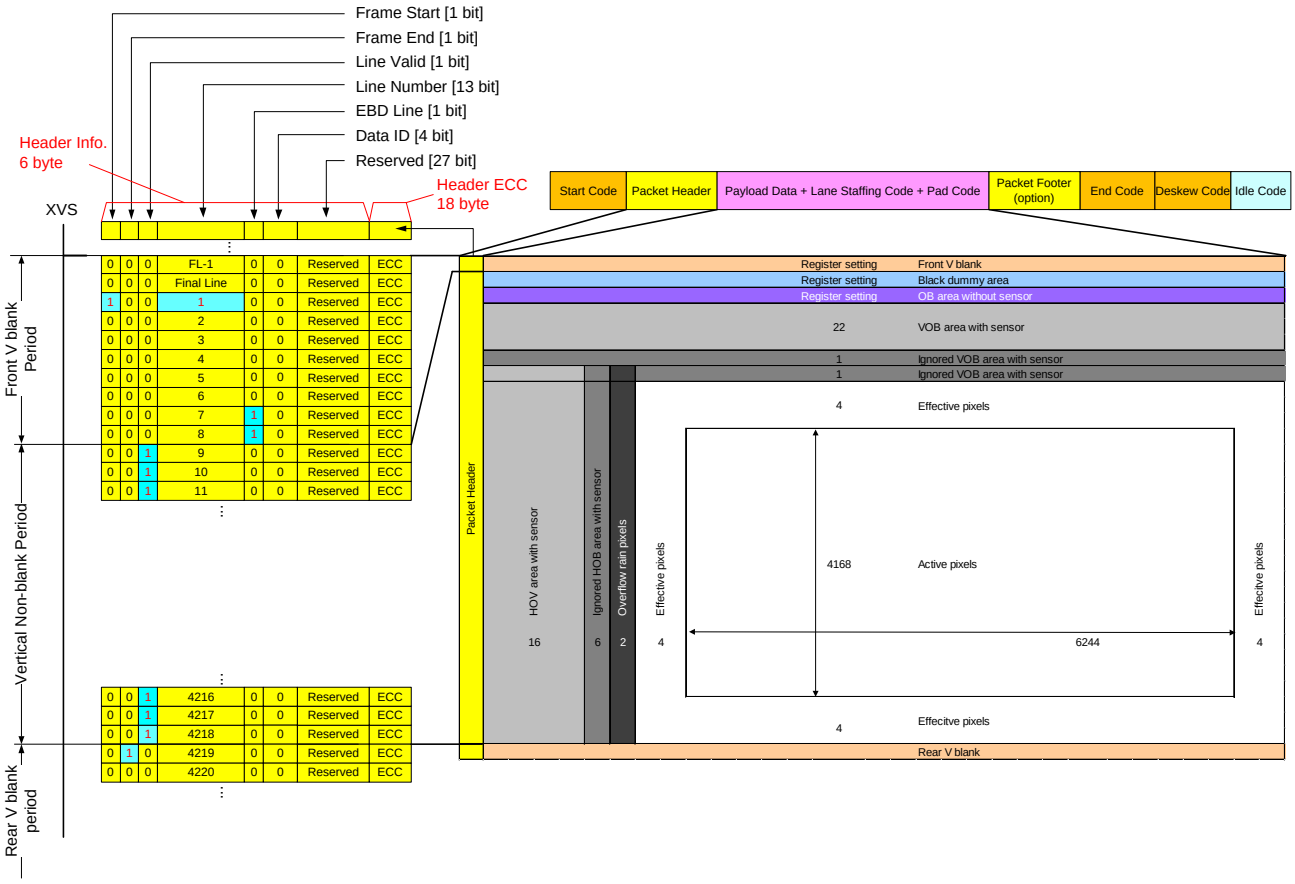


Fig. Frame Format (Normal frame, in the case of readout mode No.0, All-pixel scan readout mode)

Contents of Header in normal frame

Item	Function
Frame Start	1d is output when Line Number = 1d. (In all readout drive mode)
Frame End	1d is output at the top line of rear vertical blank period.
Line Valid	Continuously output 1d during vertical non-blank period.
Line Number	Line Number is reset to 1d while blank period in the top of the frame, and incremented by 1 unit next reset timing. Its max value is 8191d and when reaching max value, Line Number is reset to 0d and incremented by 1 unit again.
EBD Line	1d is output at the 2 lines just before the first valid line (Line Valid = 1).
Data ID	Data ID = 0h

In addition, during XVS-subsampled period by SVR, dummy data is output in vertical non-blank period, but frame format is output same as normal frame.

2. Digital overlap frame

As an example, the figure below shows contents of the header in each line in the case of digital overlap drive mode.

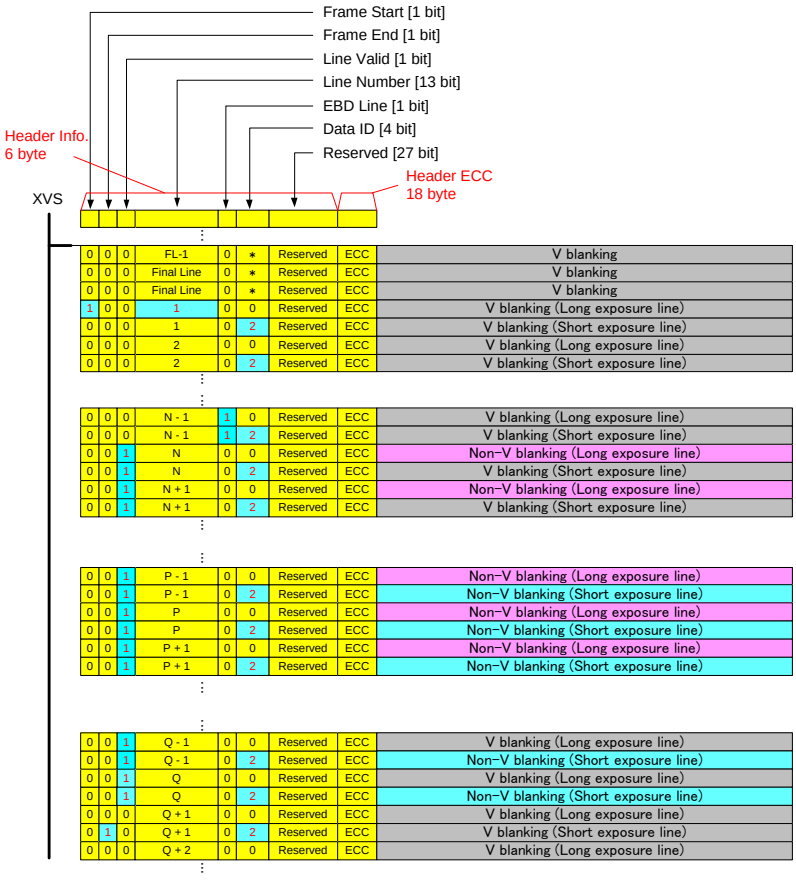


Fig. Frame Format of Digital overlap drive

Contents of Header in digital overlap frame

Item	Function
Frame Start	1d is output when Line Number = 1d at long time exposure frame line.
Frame End	1d is output at the top line of rear vertical blank period at short exposure frame line.
Line Valid	Continuously output 1d during vertical non-blank period.
Line Number	Line Number is reset to 1d while blank period in the top of the frame, and incremented by 1 unit next reset timing. Its max value is 8191d and when reaching max value, Line Number is reset to 0d and incremented by 1 unit again.
EBD Line	1d is output at the 2 lines just before the first valid line (Line Valid = 1).
Data ID	Data ID = 0h (0000b) is output when Long time exposure line Data ID = 2h (0010b) is output when Short time exposure line

3. Global 4 field readout frame

As an example, the figure below shows contents of the header in each line in the case of global 4 field readout operation.

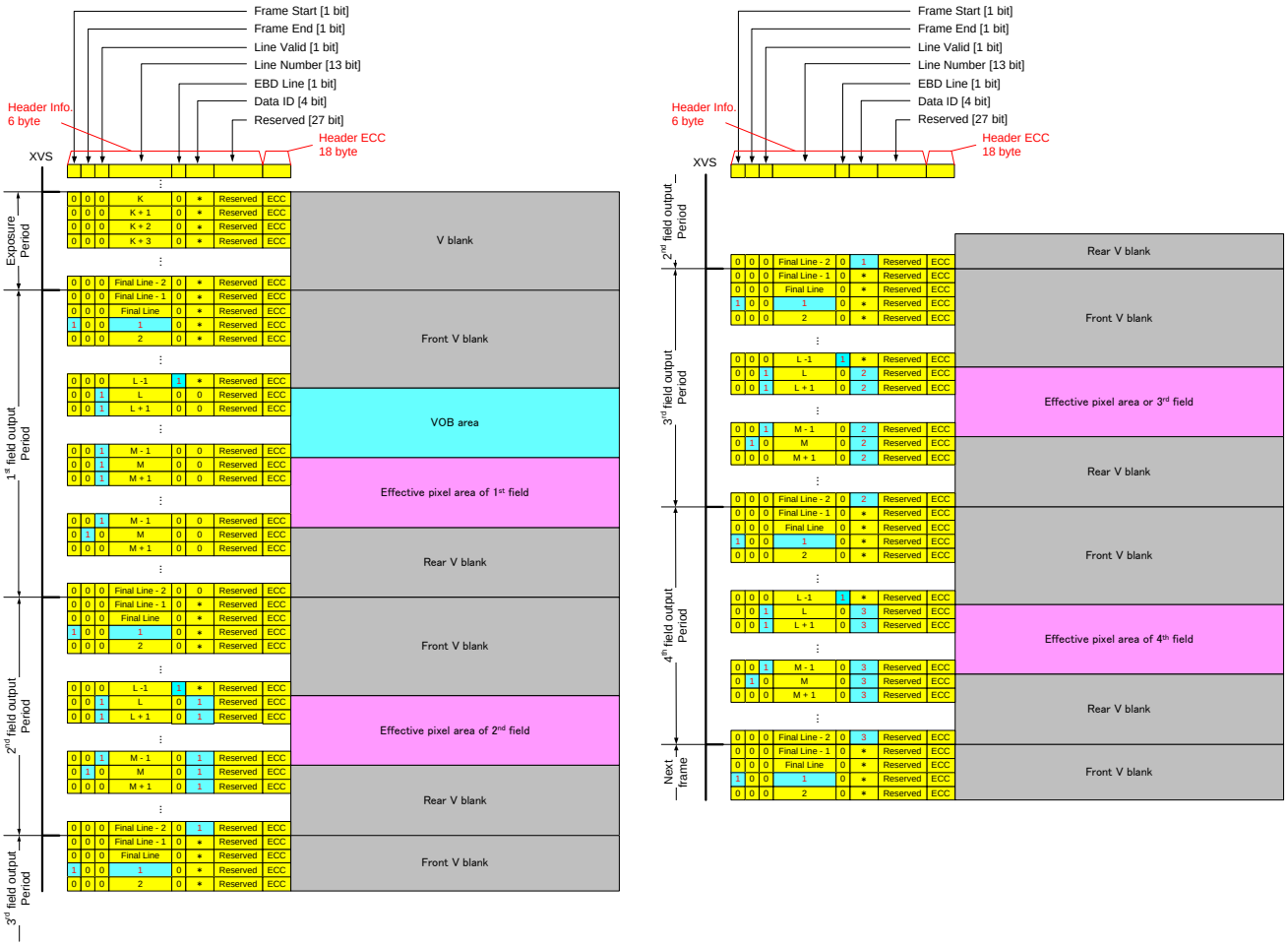


Fig. Frame Format of Global 4 Field Readout Operation

Contents of Header in global 4 field readout frame

Item	Function
Frame Start	1 is output when Line Number = 1d. (In all readout drive mode)
Frame End	1 is output at the top line of rear vertical blank period.
Line Valid	Continuously output 1 during vertical non-blank period.
Line Number	Line Number is reset to 1d while blank period in the top of the frame, and incremented by 1 unit next reset timing. Its max value is 8191d and when reaching max value, Line Number is reset to 0d and incremented by 1 unit again.
EBD Line	1d is output at the 2 lines just before the first valid line (Line Valid = 1) in every field.
Data ID	Data ID = 0h (0000b) is output when VOB and 1st field effective pixel area output period Data ID = 1h (0001b) is output when 2nd field effective pixel area output period Data ID = 2h (0010b) is output when 3rd field effective pixel area output period Data ID = 3h (0011b) is output when 4th field effective pixel area output period

4. Invalid frame (with training sequence)

This sensor generates training sequence in standby canceling, mode changing, and so on.
After 2 XHS period from XVS input, standby sequence, High-Z, low period, training sequence, idle codes are output. During this, Start Code, Packet Header and End Code are not output.

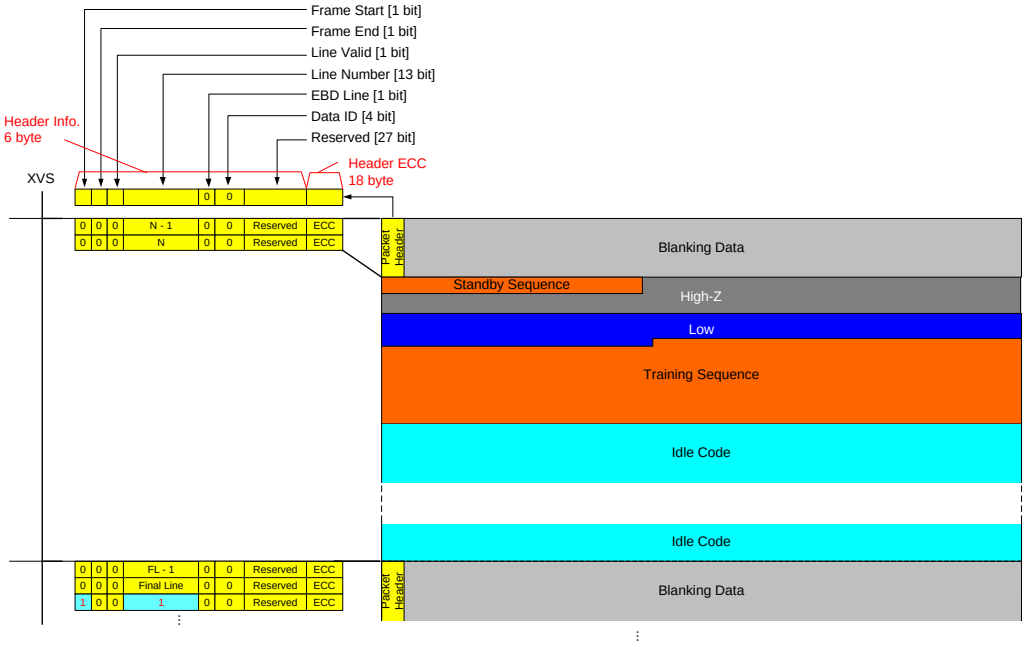


Fig. Frame Format (Invalid frame with training sequence)

Standby and training sequence are generated in case of following situations.

(1) Power-On
When power-on sequence, training sequence is generated before first XVS input.
In addition, initial setting mode of which registers are sent before first XVS input is fulfilled the condition of mode transition with training sequence from mode0-b All-pixel readout mode (AD 14 bits, 14 bits output word length), training sequence is also generated after first XVS input.

(2) Mode transition under the specific situations.
When mode transitions, invalid frame with training sequence is generated after XVS input in case of following situations.
a. Output word bit length is changed.
b. Number of horizontal output pixels is changed. (Including horizontal freely cropping function)
c. SLVS-EC setting registers[*1] are changed.

[*1] CRC_EN, ECC_EN, INIT_LENGTH, SYNC_LENGTH, DESKEW_LENGTH, DESKEW_INTERVAL, STANDBY_LENGTH, SYNC_SYMBOL, DESKEW_SYMBOL, IDLE_CODE1 to 4, STANDBY_SYMBOL

(3) SLEEP (Standby) start
When sleep or standby is started, standby sequence is generated without XVS input.

(4) SLEEP (Standby) cancel
When sleep or standby is canceled, training sequence is generated without XVS input.

5. Invalid frame (without training sequence)

During exposure frame period at global reset shutter operation, this sensor generates invalid frame without training sequence. Frame Start = 1d and Frame End = 1d is not output in this frame, and Line Number is not reset also.

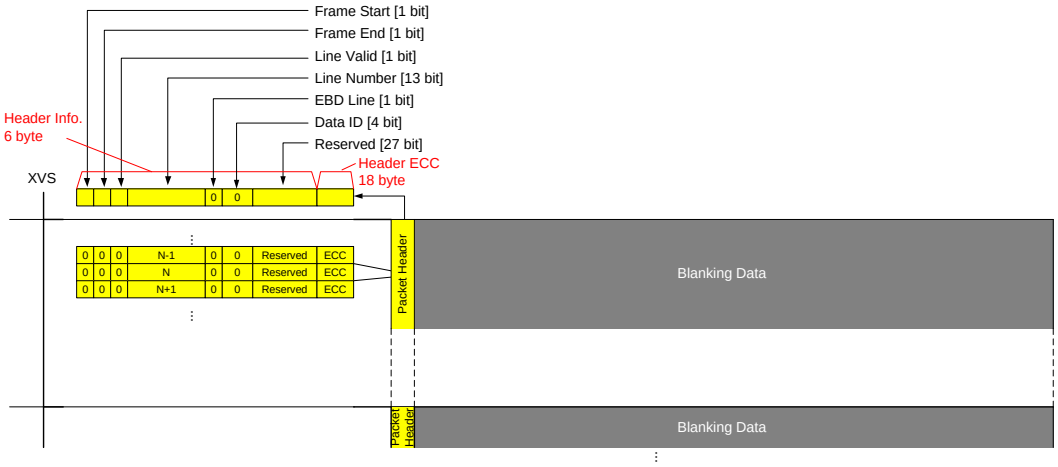


Fig. Frame Format (Invalid frame without training sequence)

Image Data Output Format

Mode0: All-pixel Readout Mode

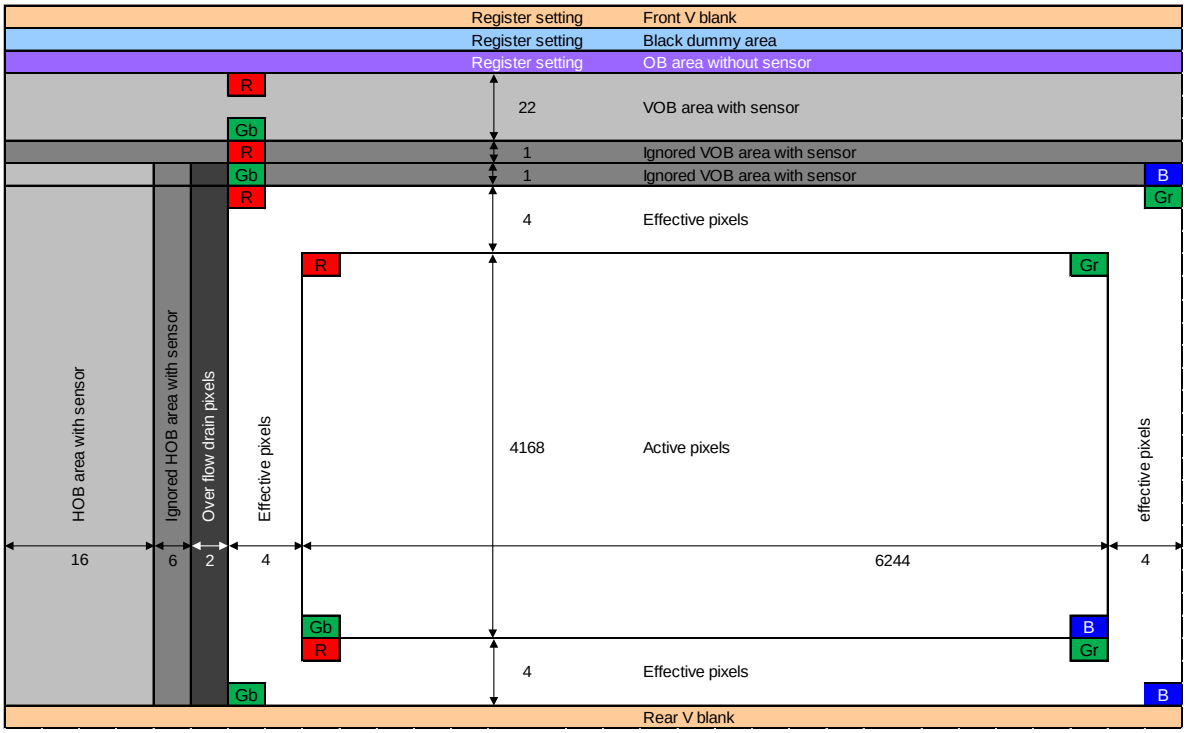
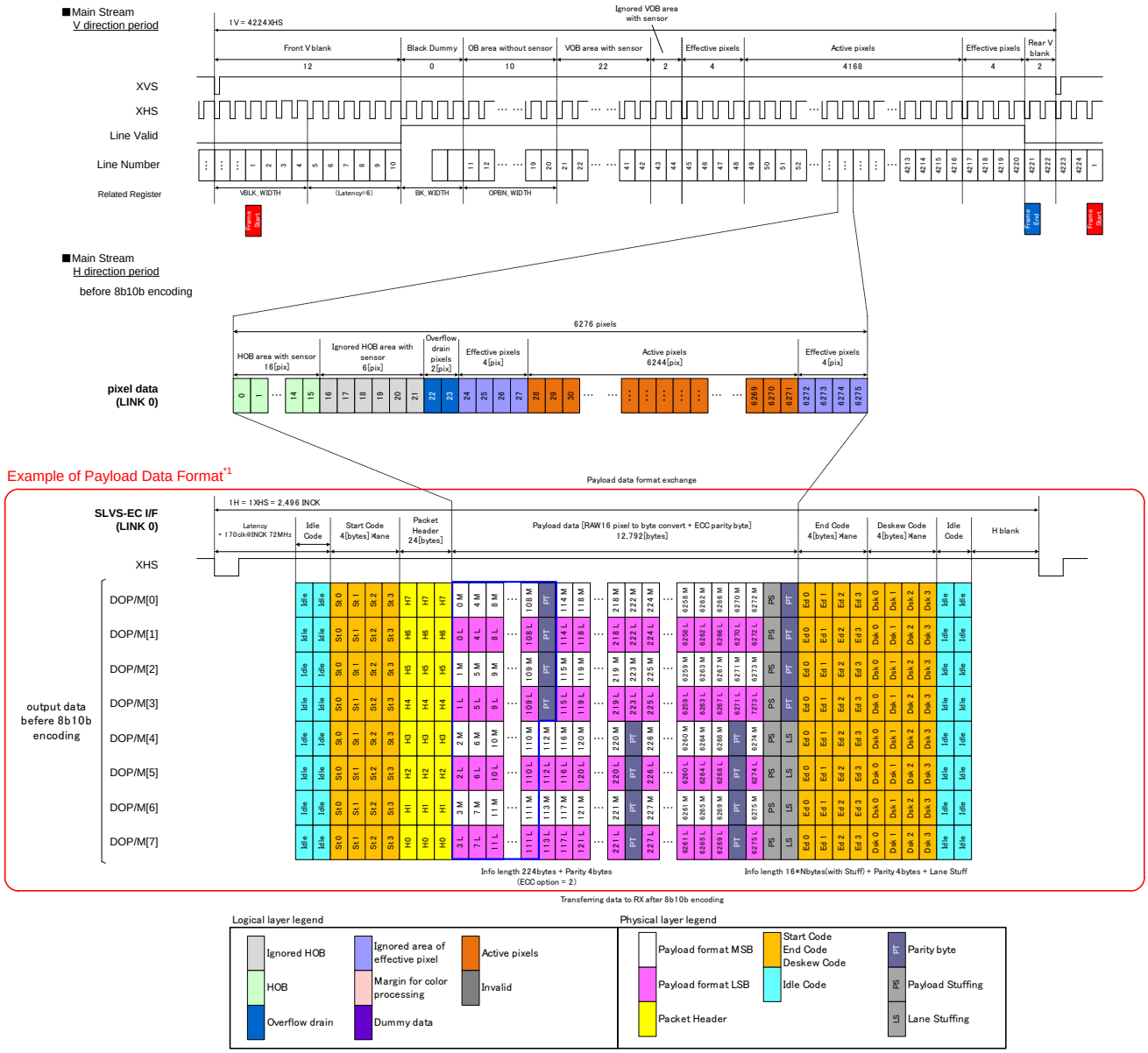


Fig. Readout Image Diagram in Mode0 All-pixel Readout Mode

Timing Chart



*1 Payload Data Format varies each AD bit and word length.
This Payload Data Format is example of Mode0-a All-pixel Readout Mode (AD 16 bits, Word Length 16 bits).
See "SLVS-EC Specification Version 1.2" for detail of Payload Data Format of other mode.

Fig. Drive Timing in Mode0 All-pixel Readout Mode

Mode1: All-pixel Readout Mode 2-Parallel ADC Readout

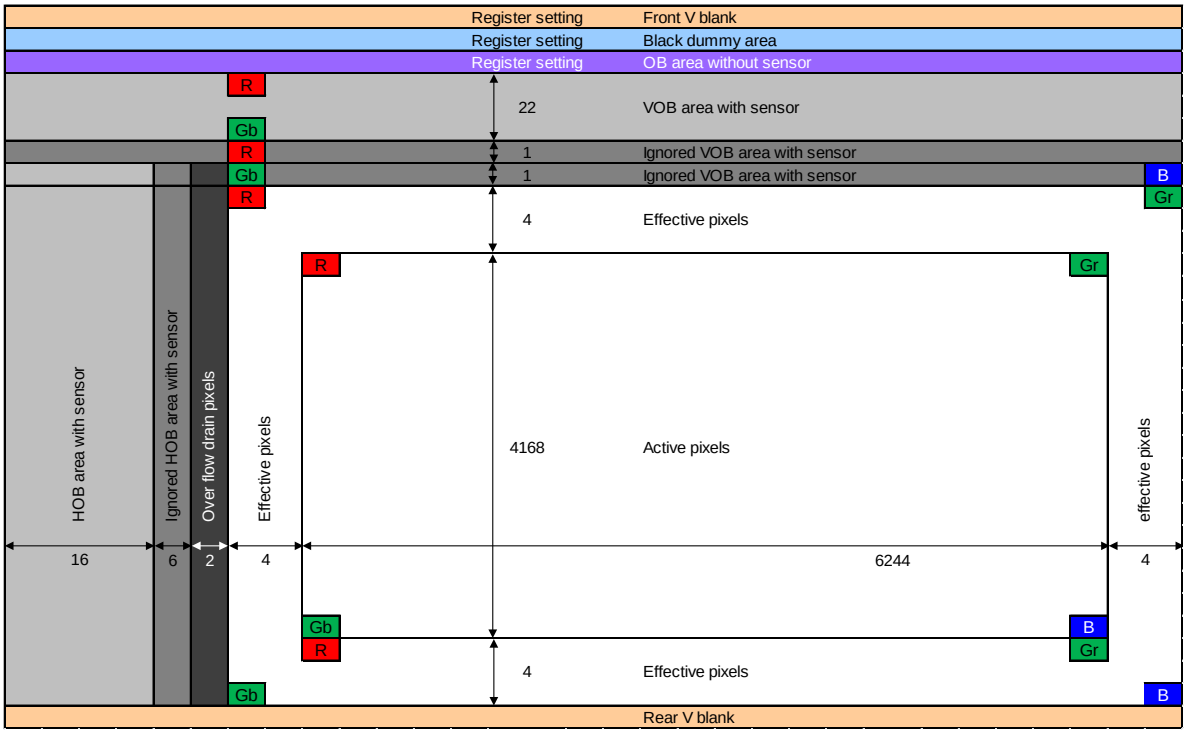
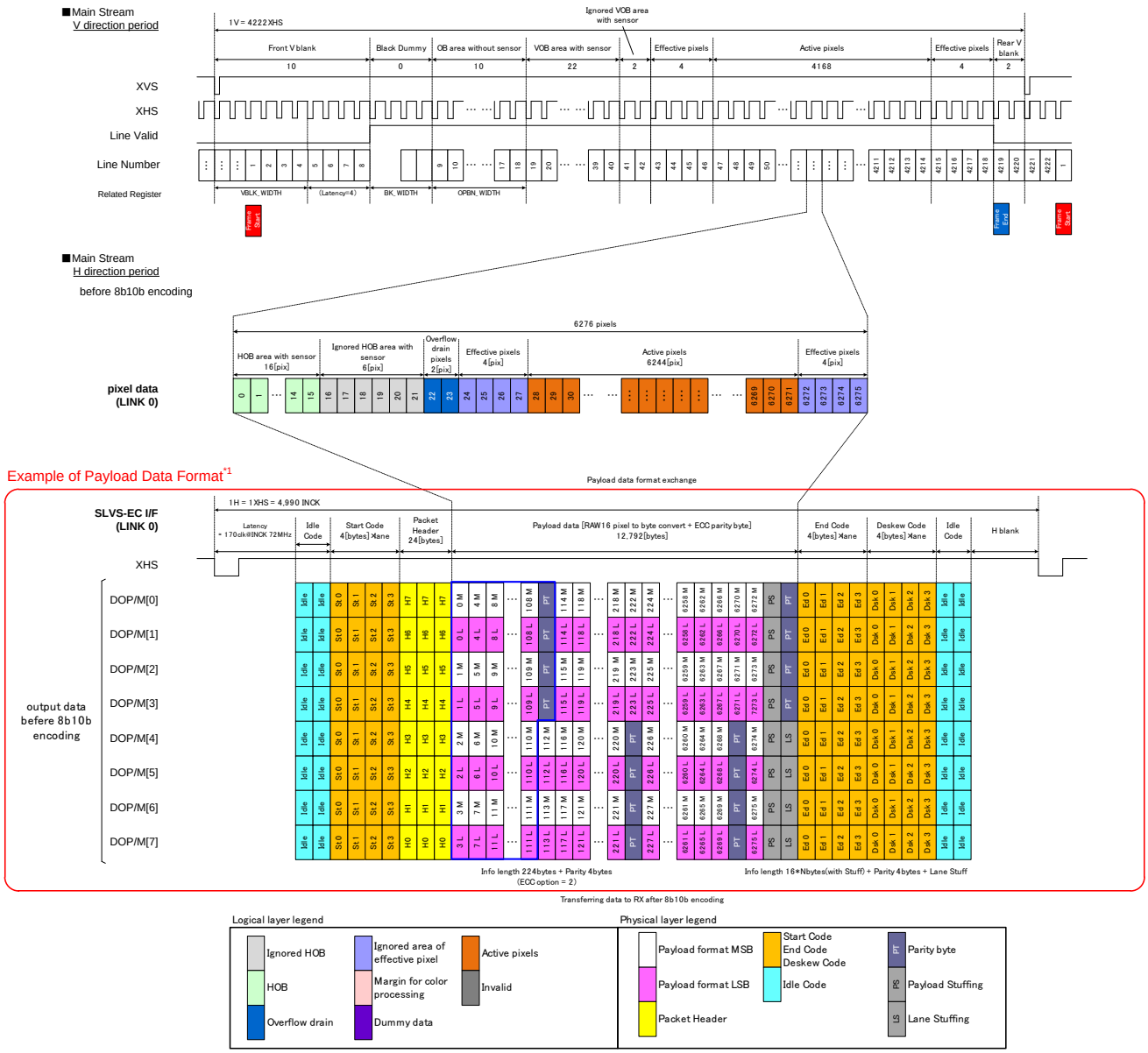


Fig. Readout Image Diagram in Mode1 All-pixel Readout Mode 2-Parallel ADC Readout

Timing Chart



*1 Payload Data Format varies each AD bit and word length.
This Payload Data Format is example of Mode1-a All-pixel Readout Mode 2-parallel ADC readout (AD 16 bits, Word Length 16 bits).
See "SLVS-EC Specification Version 1.2" for detail of Payload Data Format of other mode.

Fig. Drive Timing in Mode1 All-pixel Readout Mode 2-Parallel ADC Readout

Mode3: All-pixel Readout Mode Digital Overlap Drive

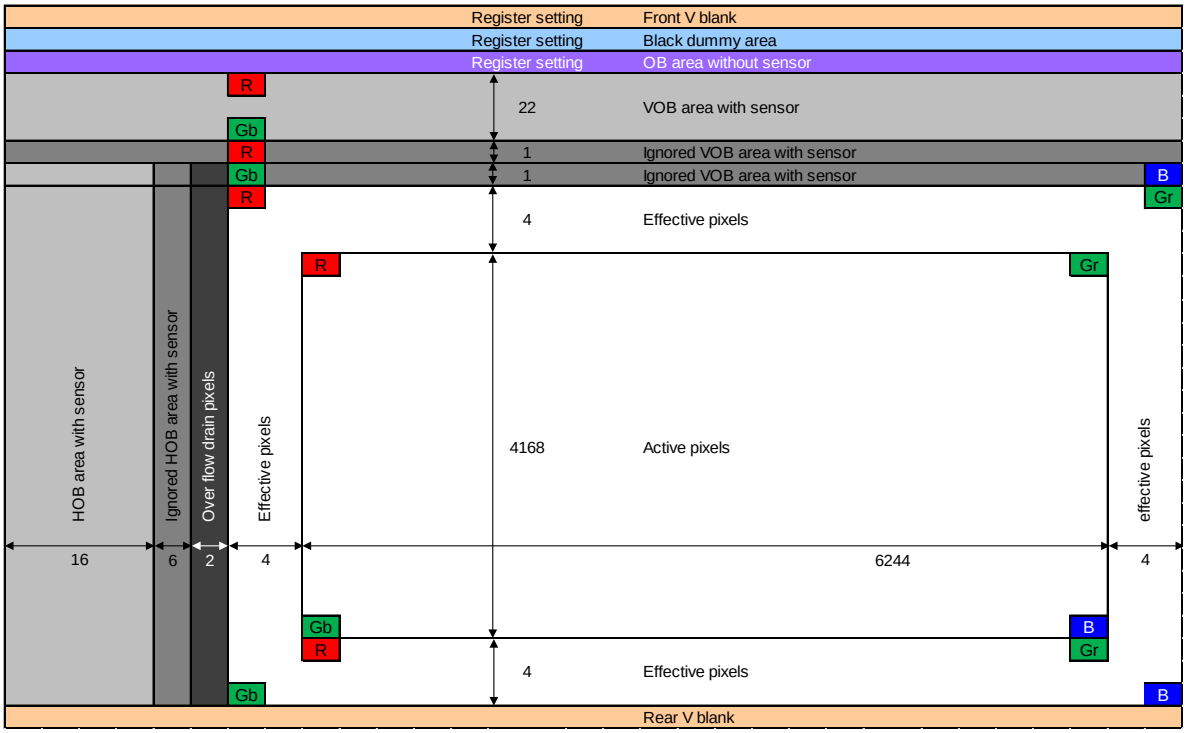
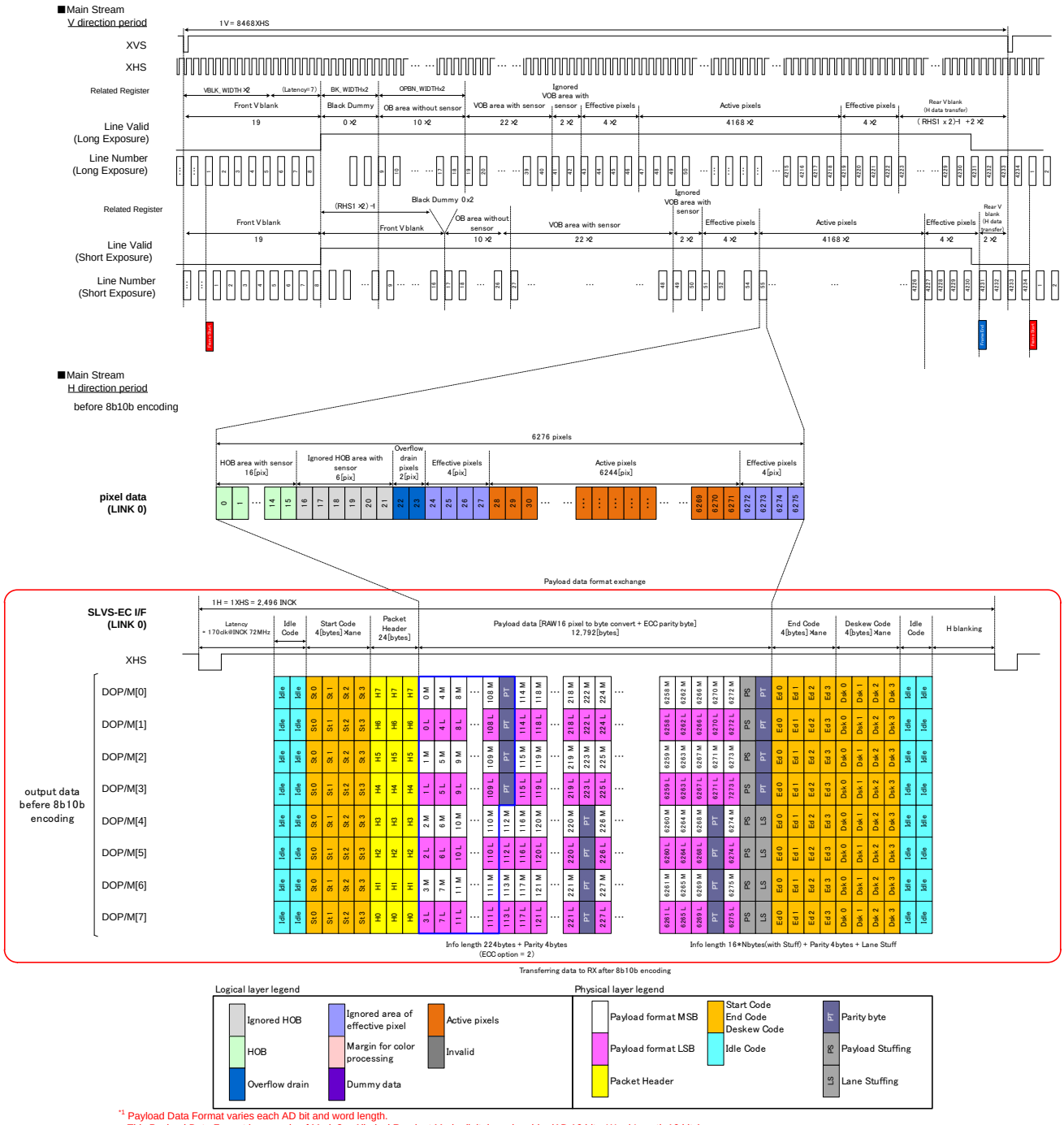


Fig. Readout Image Diagram in Mode3 All-pixel Readout Mode Digital Overlap Drive

Timing Chart



*1 Payload Data Format varies each AD bit and word length.
This Payload Data Format is example of Mode3-a All-pixel Readout Mode digital overlap drive(AD 16 bits, Word Length 16 bits).
See "SLVS-EC Specification Version 1.2" for detail of Payload Data Format of other mode.

Fig. Drive Timing in Mode3 All-pixel Readout Mode Digital Overlap Drive

Mode5: Vertical 2/2-line and Horizontal 2/2-line Weighted Binning Readout Mode

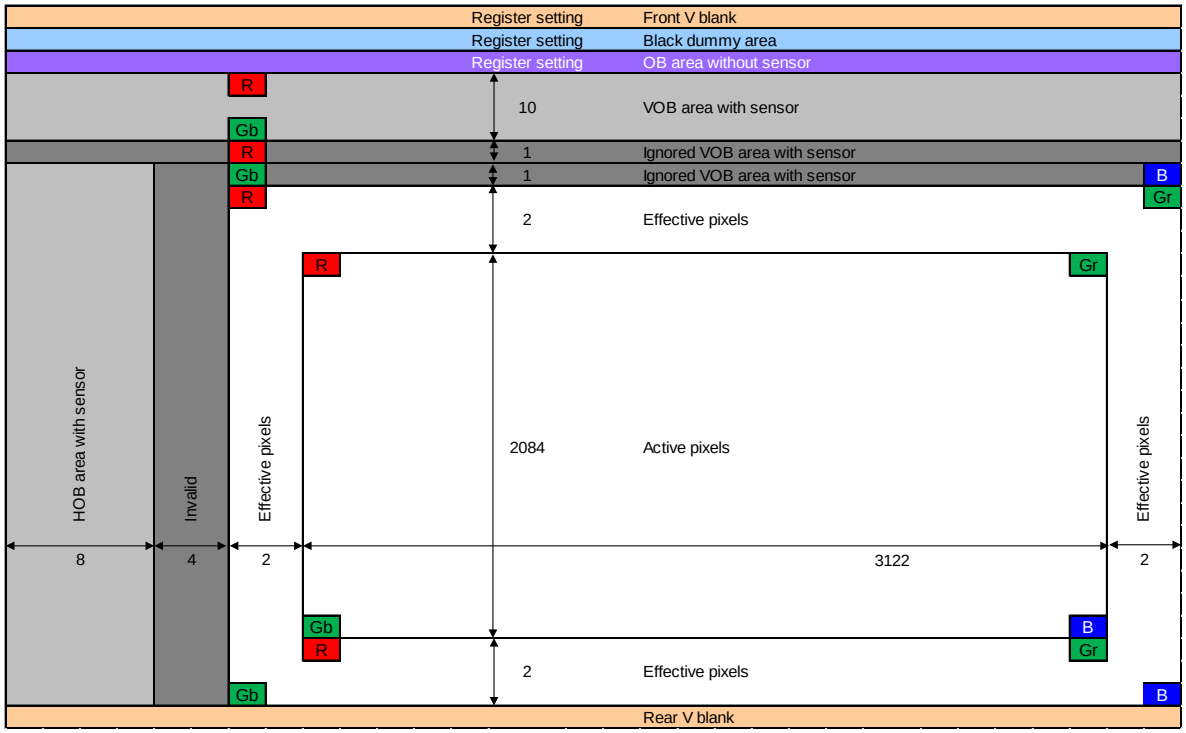


Fig. Readout Image Diagram in Mode5 Vertical 2/2-line and Horizontal 2/2-line Weighted Binning Readout Mode

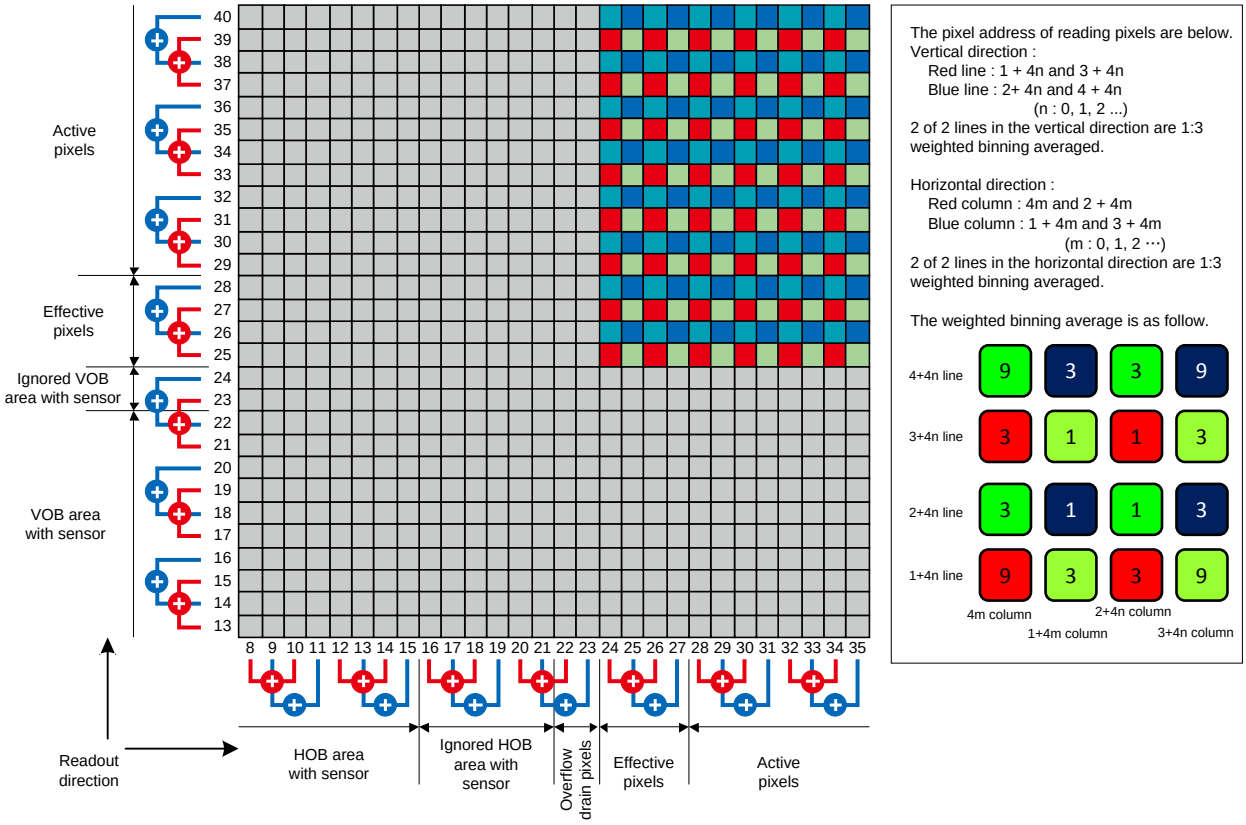


Fig. Binning Image

Timing Chart

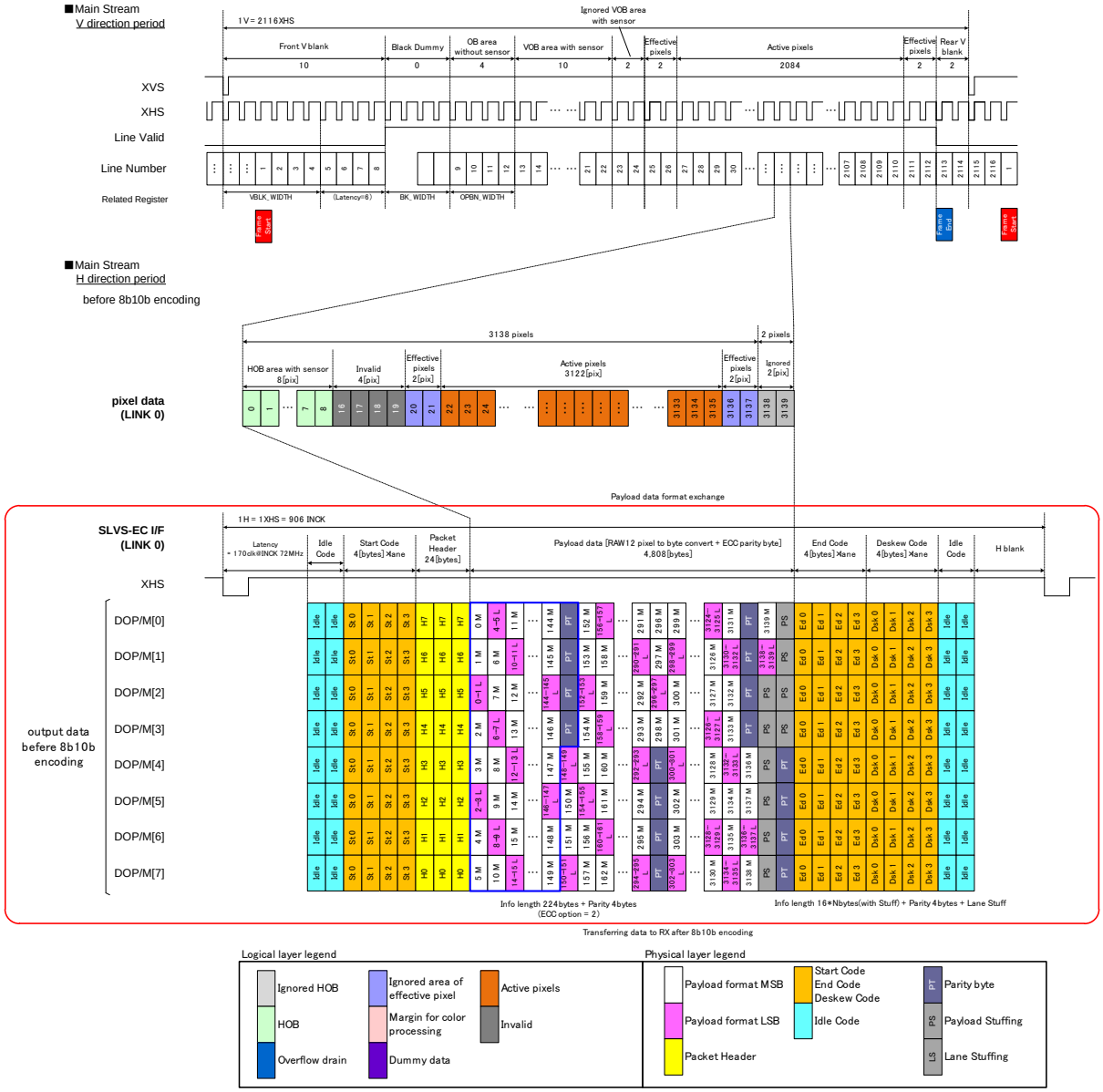


Fig. Drive Timing in Mode5 Vertical 2/2-line and Horizontal 2/2-line Weighted Binning Readout Mode

Mode6: Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode

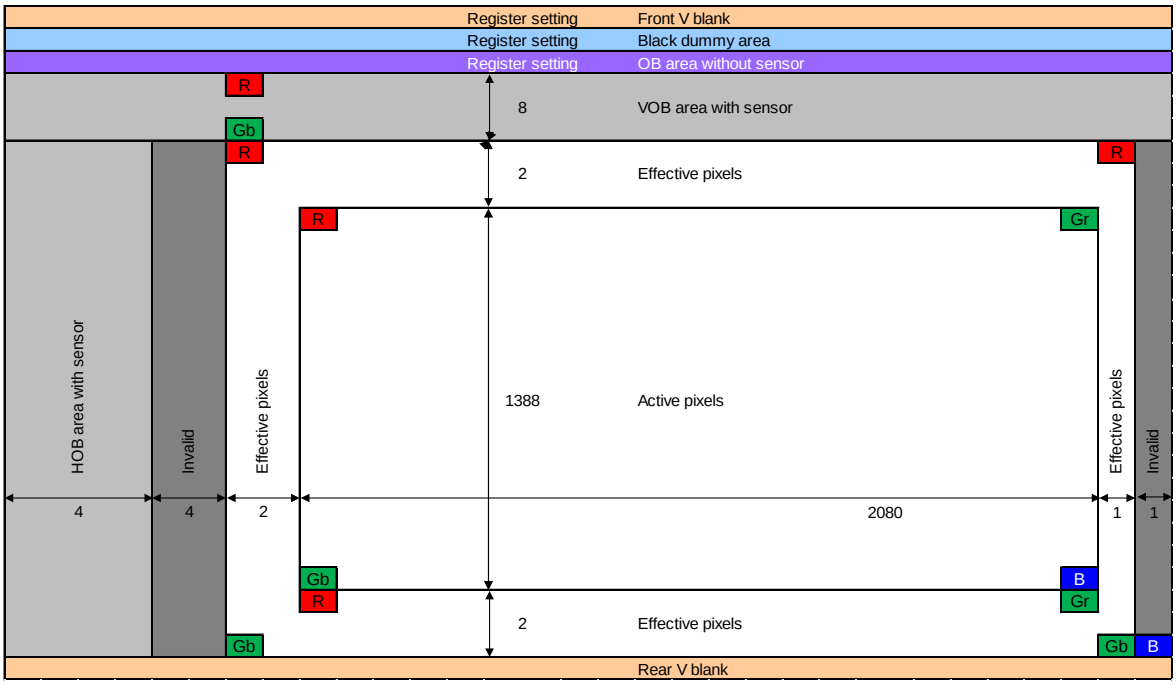


Fig. Readout Image Diagram in Mode6 Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode

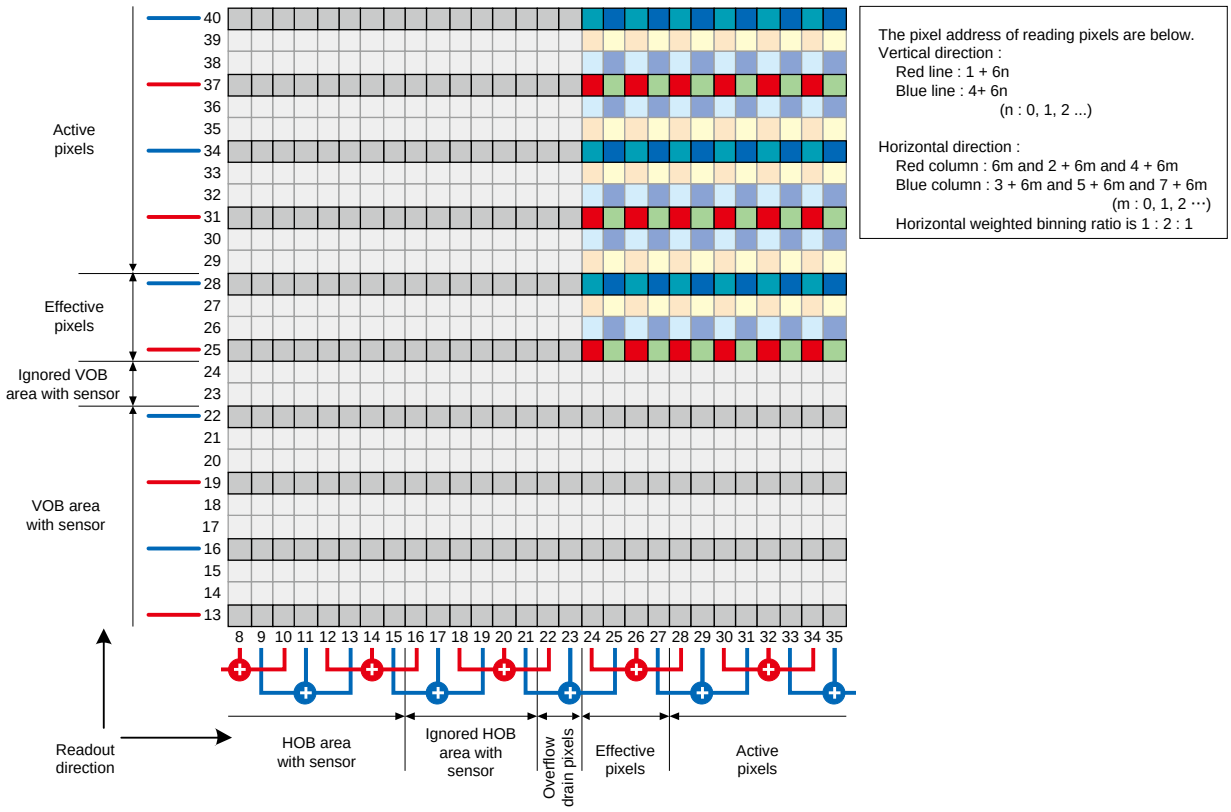


Fig. Binning Image

Timing Chart

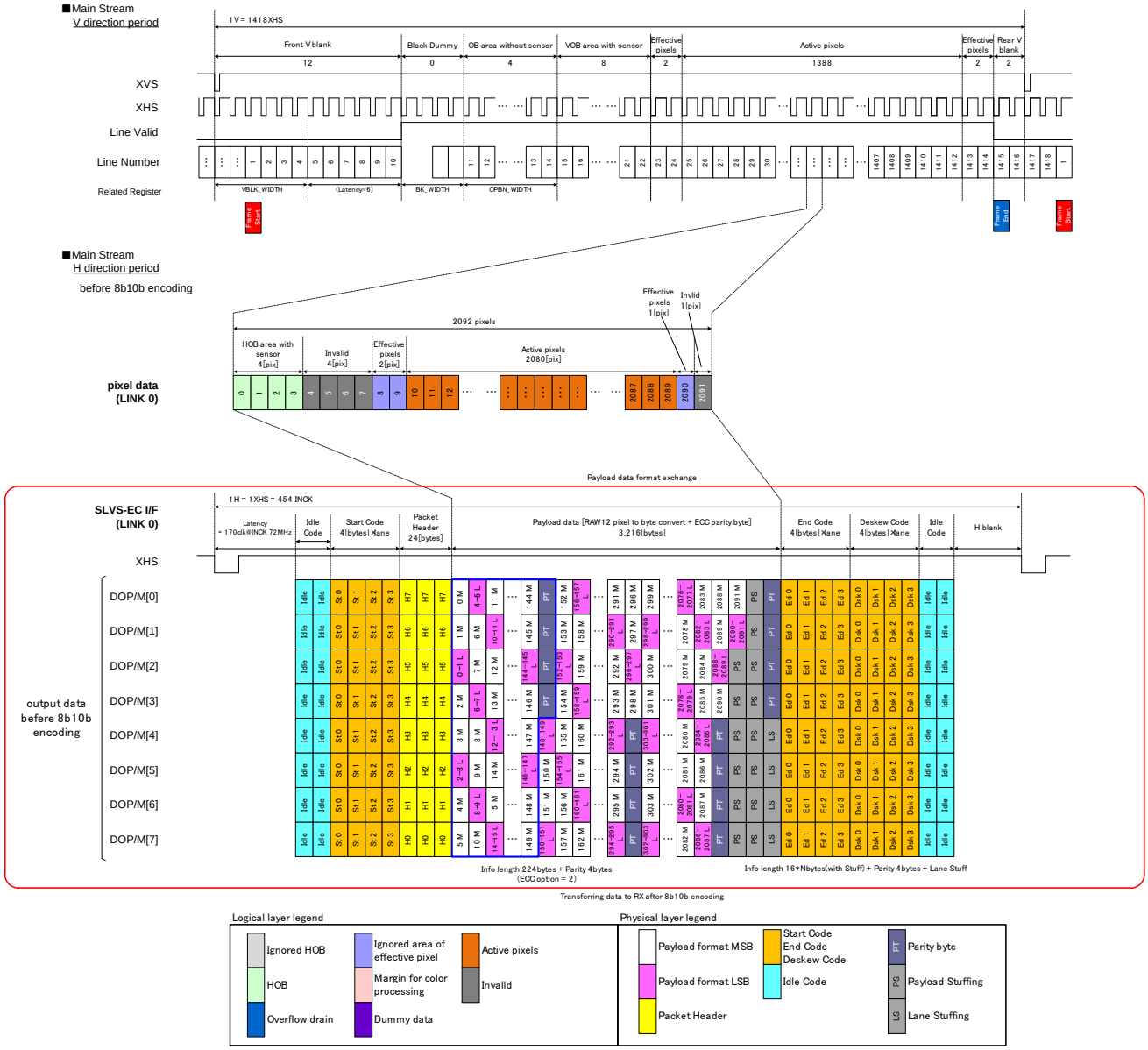


Fig. Drive Timing in Mode6 Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode

Mode7: Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode

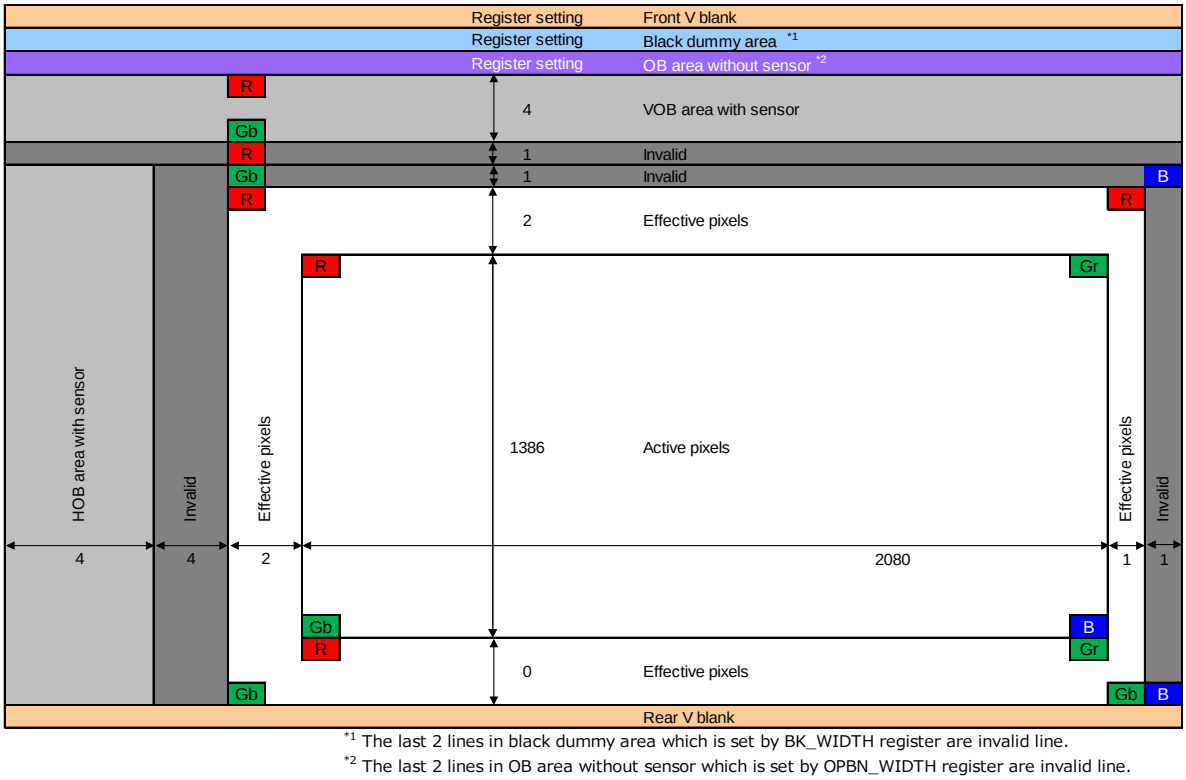


Fig. Readout Image Diagram in Mode7 Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode

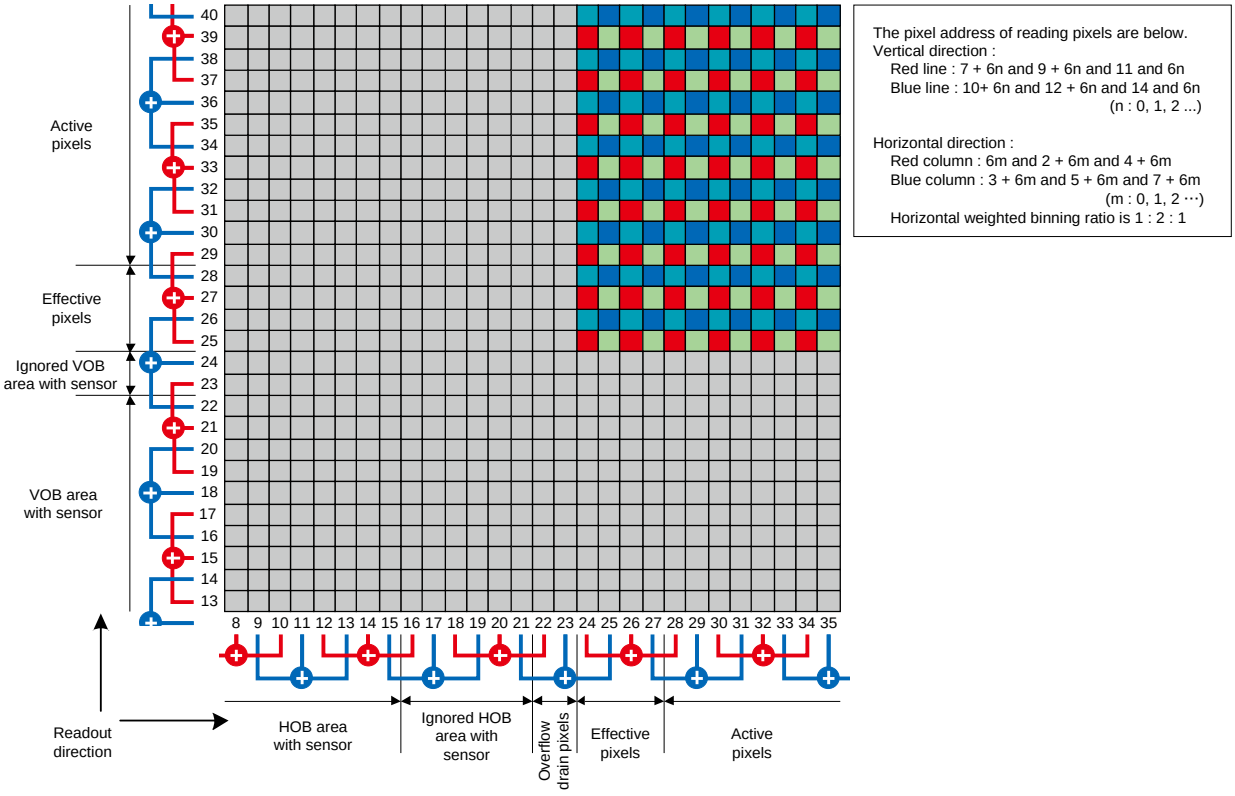


Fig. Binning Image

Timing Chart

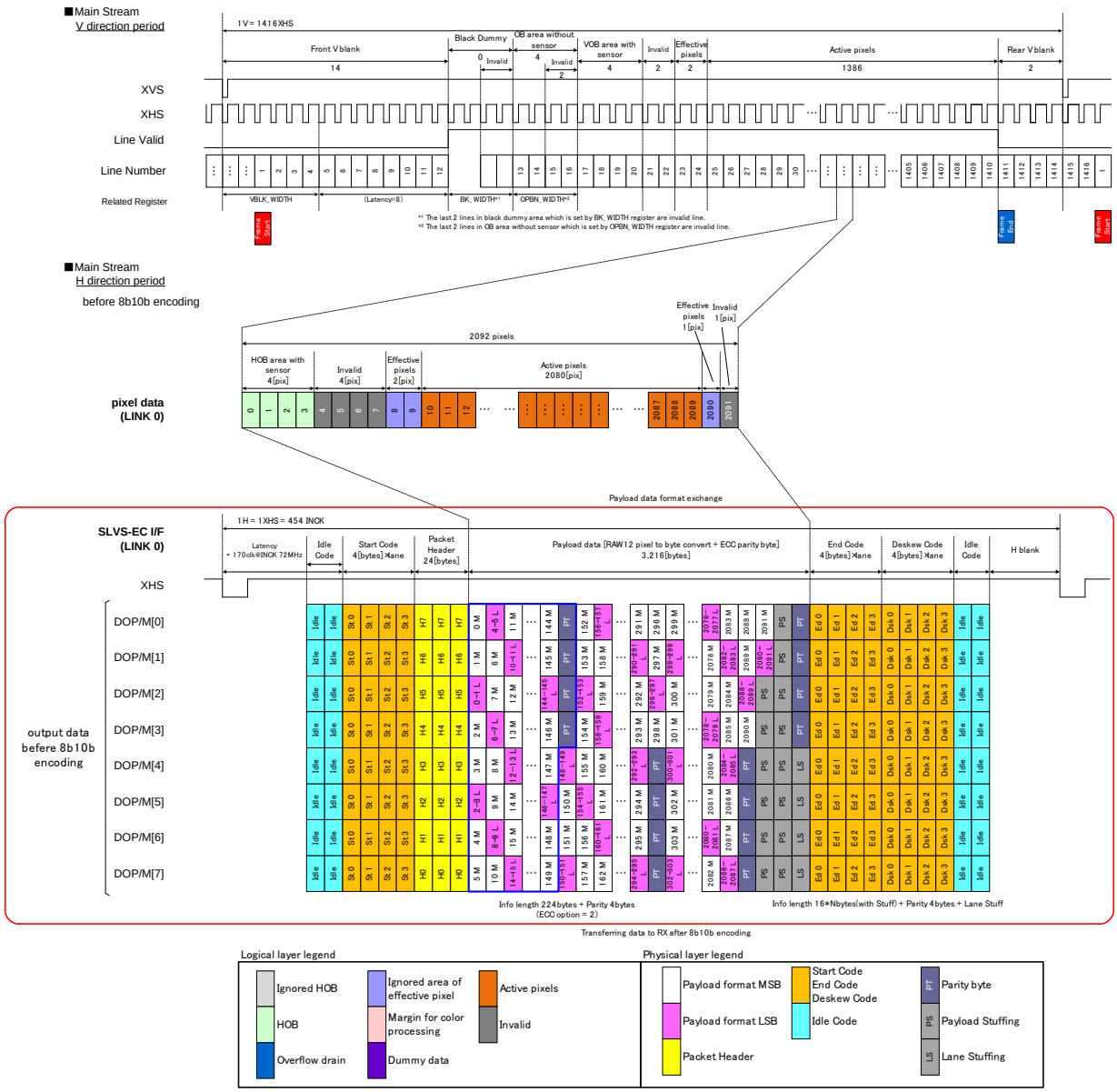


Fig. Drive Timing in Mode7 Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode

Mode10: Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

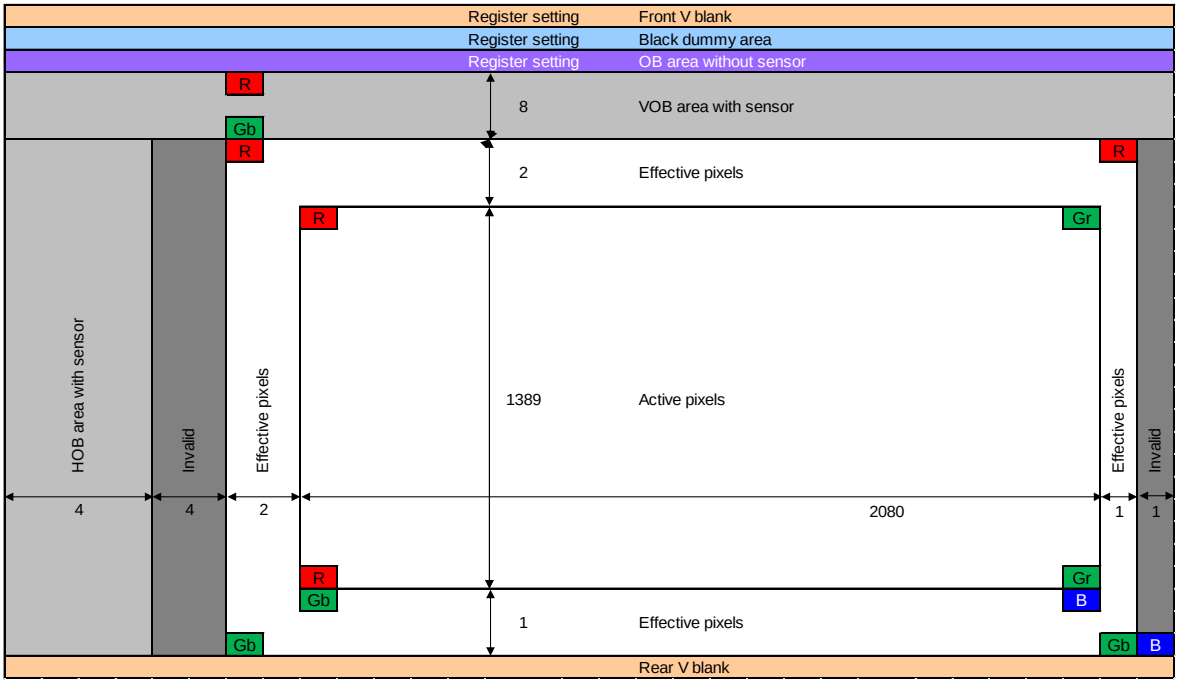


Fig. Readout Image Diagram in Mode10 Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

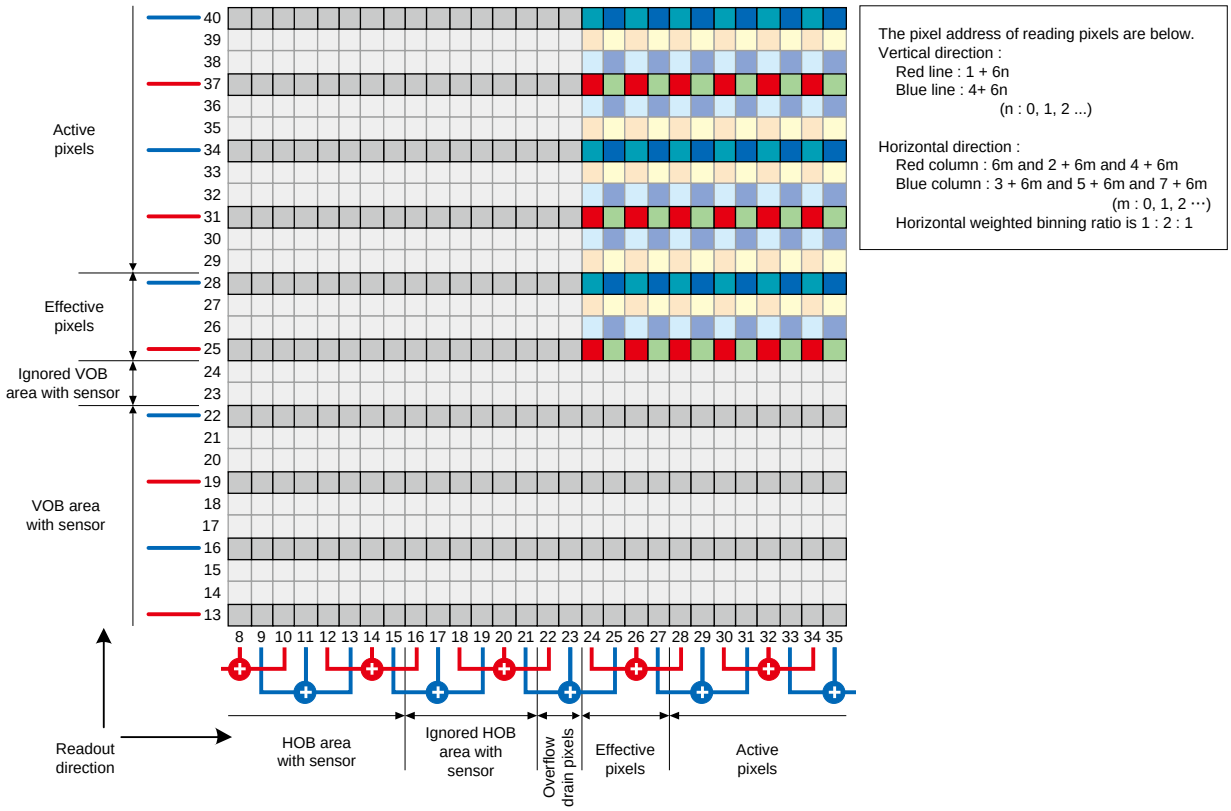


Fig. Binning Image

Timing Chart

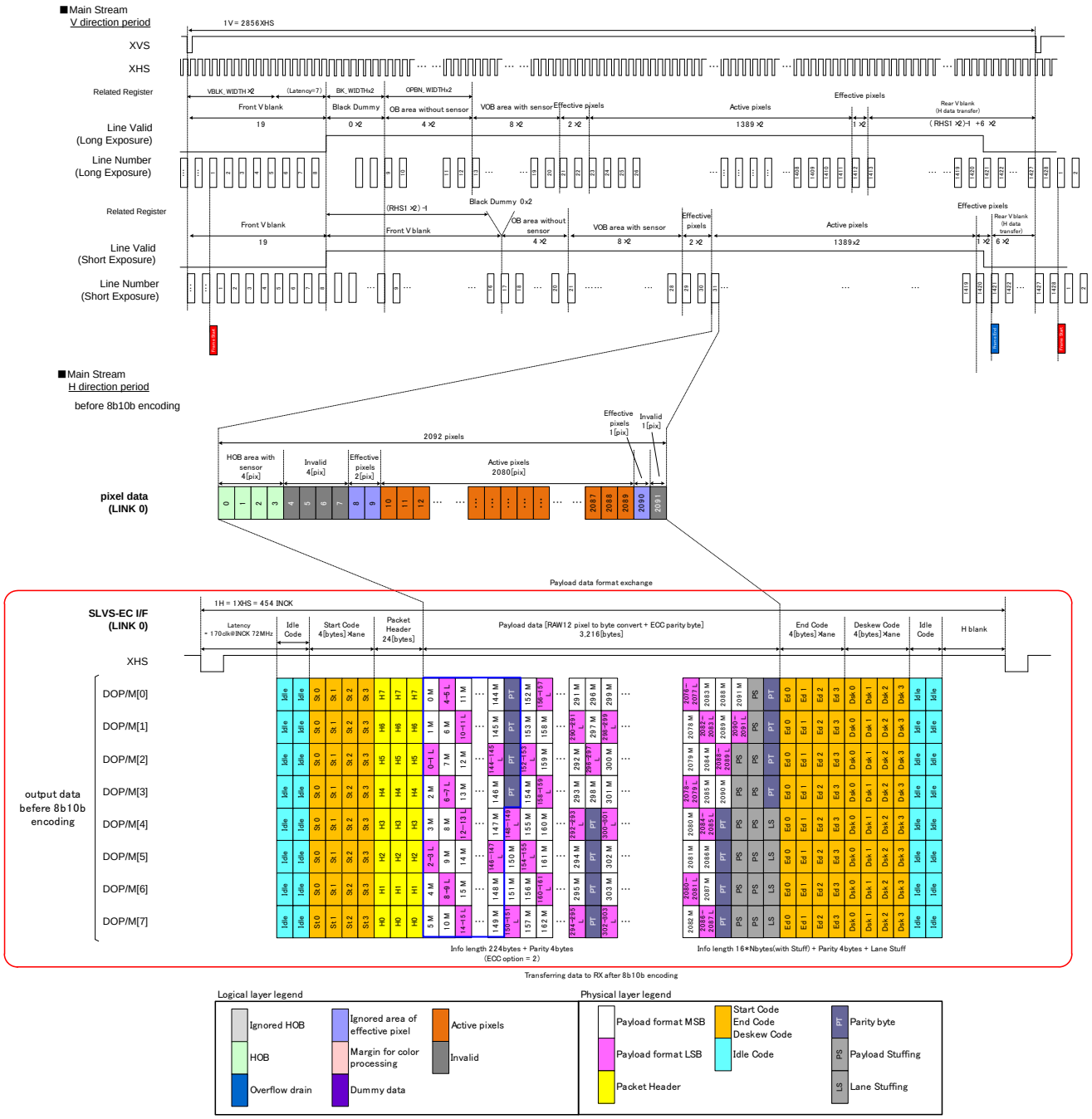


Fig. Drive Timing in Mode10 Vertical 1/3 Subsampling, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

Mode11: Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

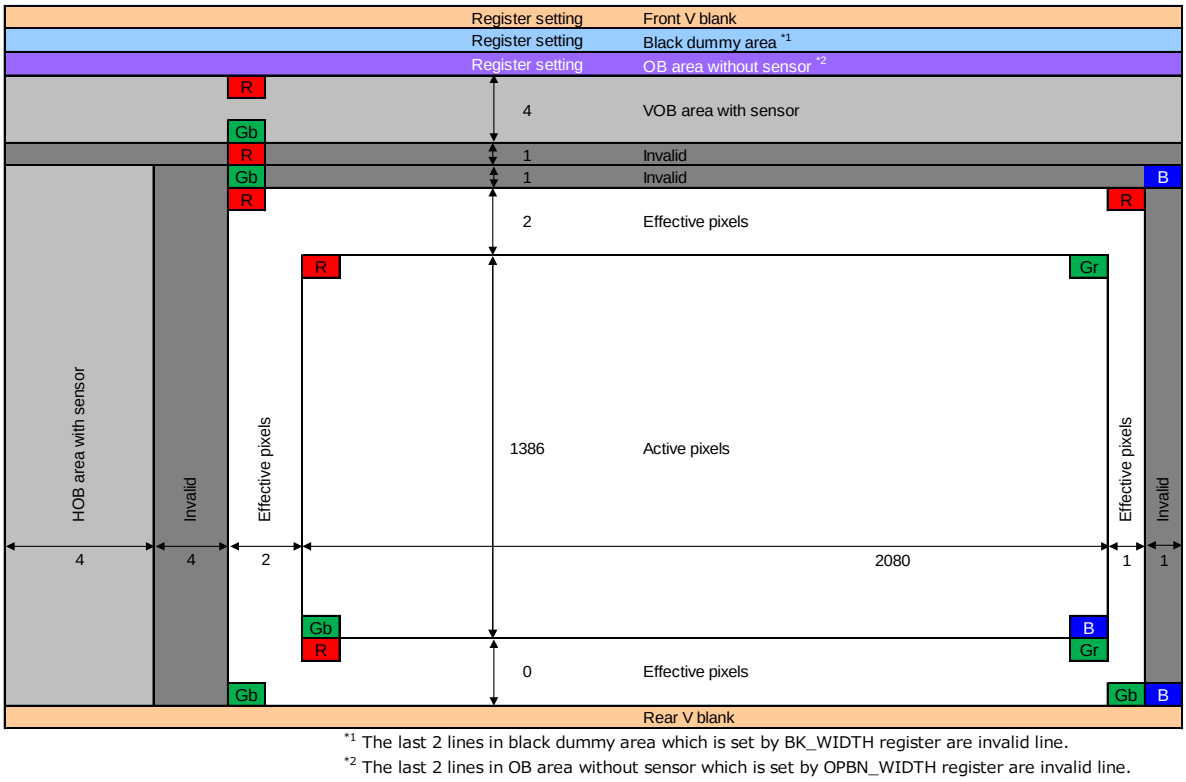


Fig. Readout Image Diagram in Mode11 Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

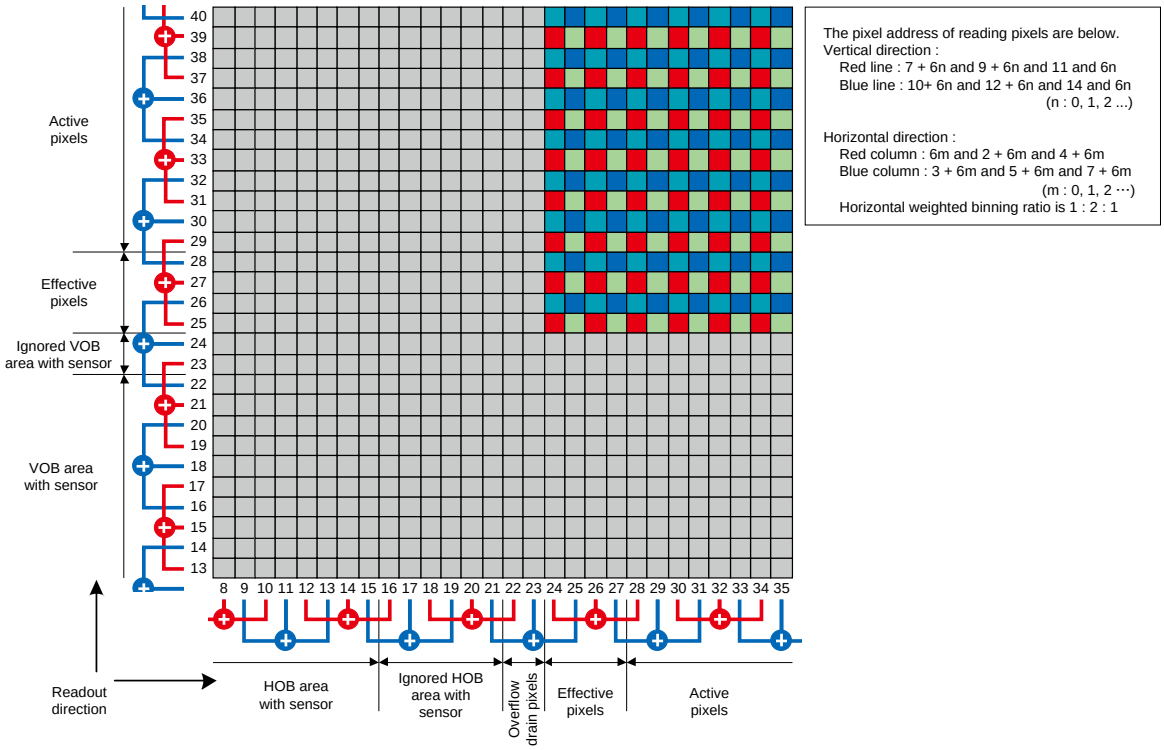


Fig. Binning Image

Timing Chart

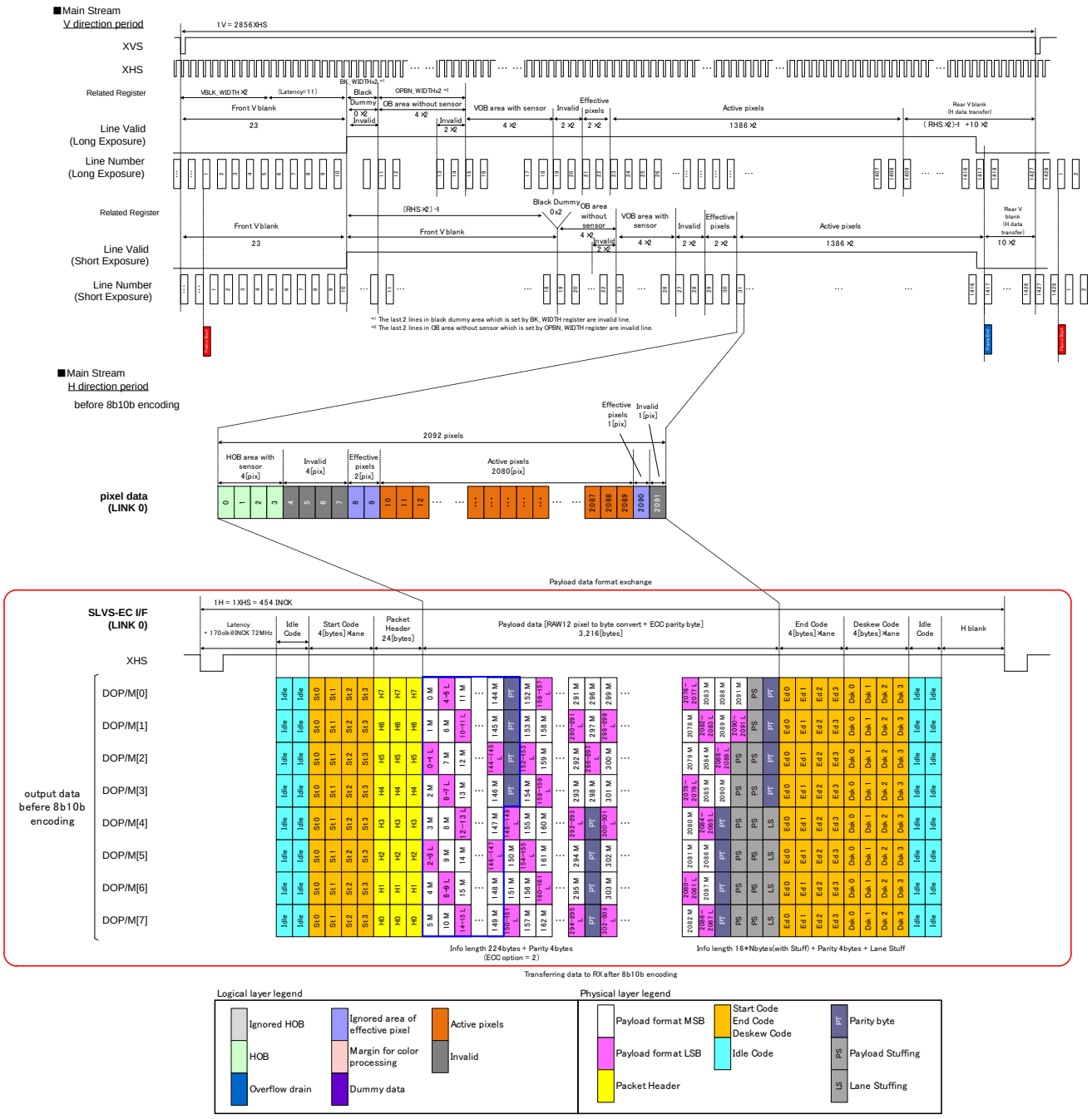


Fig. Drive Timing in Mode11 Vertical 3/3-line Binning, Horizontal 3 Weighted Binning Readout Mode Digital Overlap Drive

Mode12: Vertical 1/5 Subsampling, Horizontal 3 Binning Readout Mode

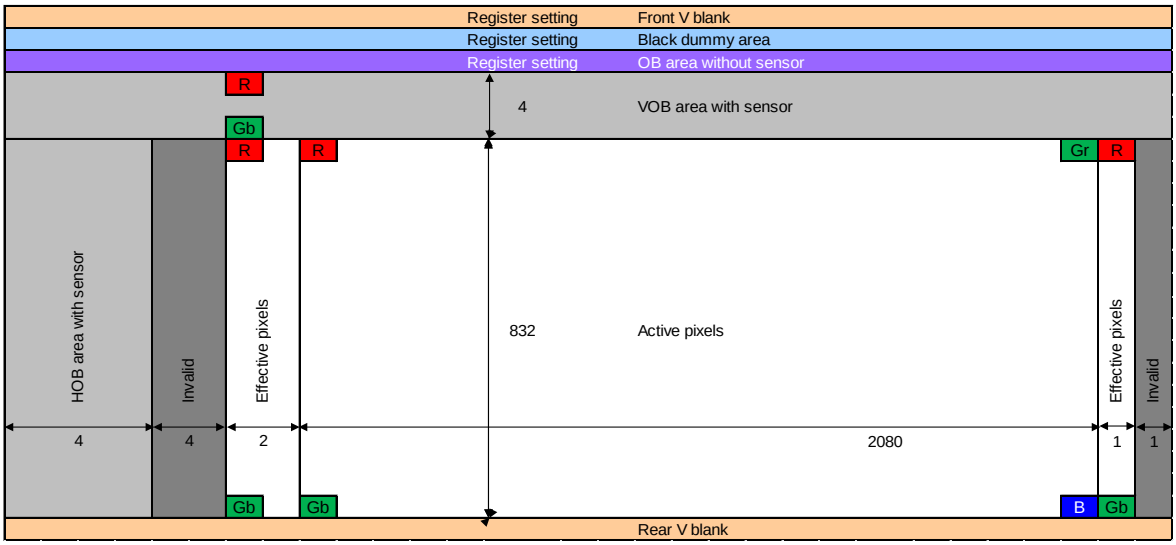


Fig. Readout Image Diagram in Mode12 Vertical 1/5 Subsampling, Horizontal 3 Weighted Binning Readout Mode

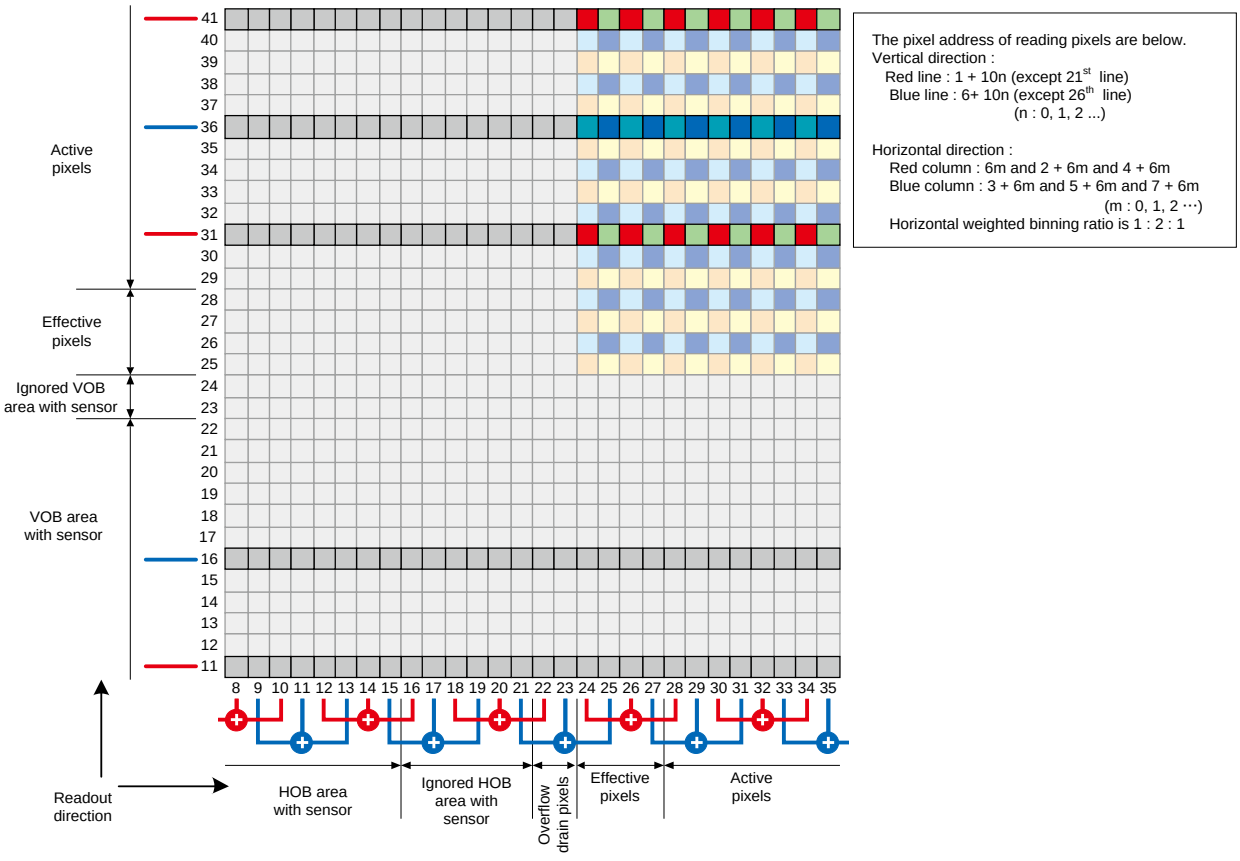


Fig. Binning Image

Timing Chart

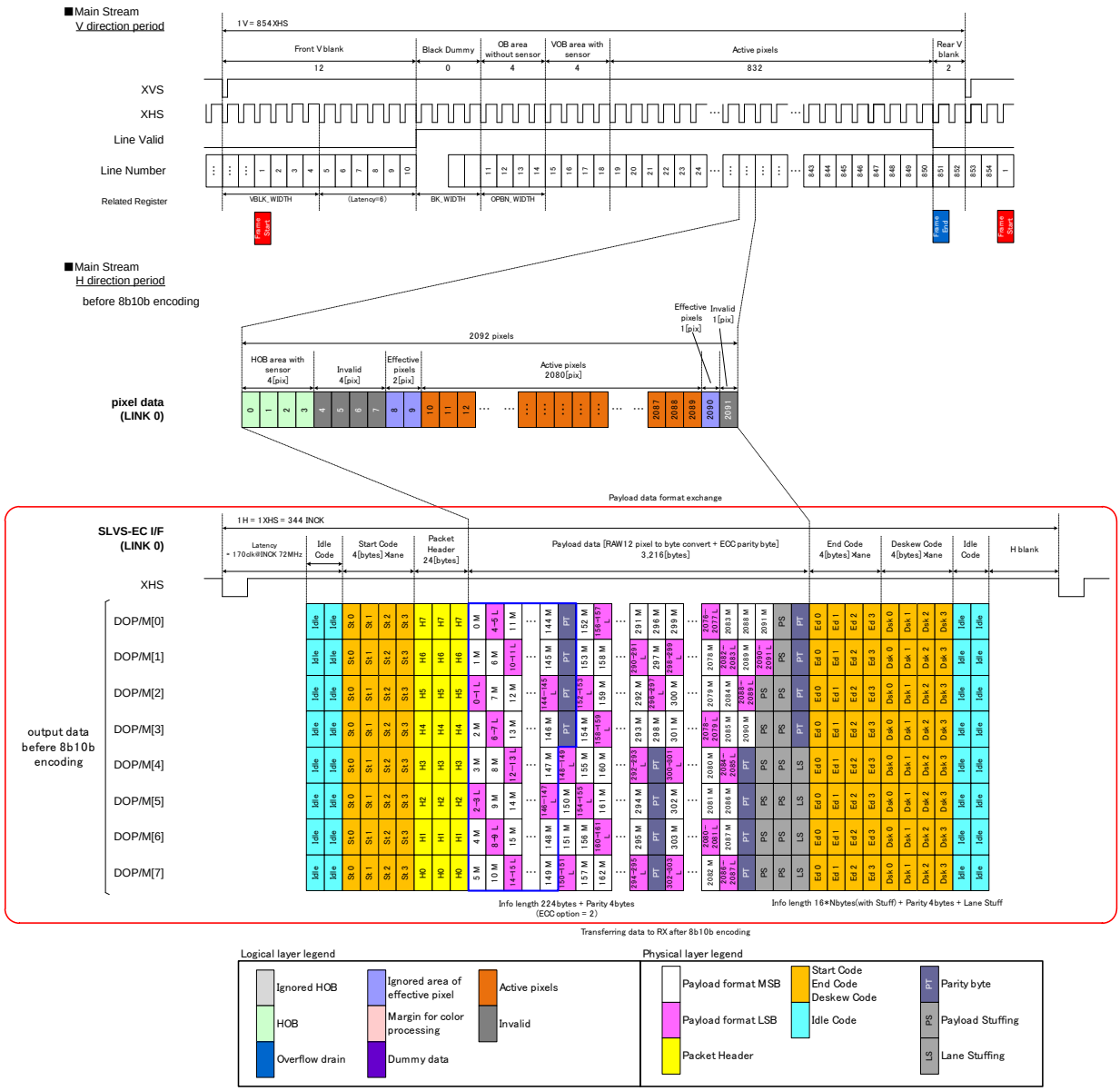


Fig. Drive Timing in Mode12 Vertical 1/5 Subsampling, Horizontal 3 Weighted Binning Readout Mode

Mode13: Vertical 3/5 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

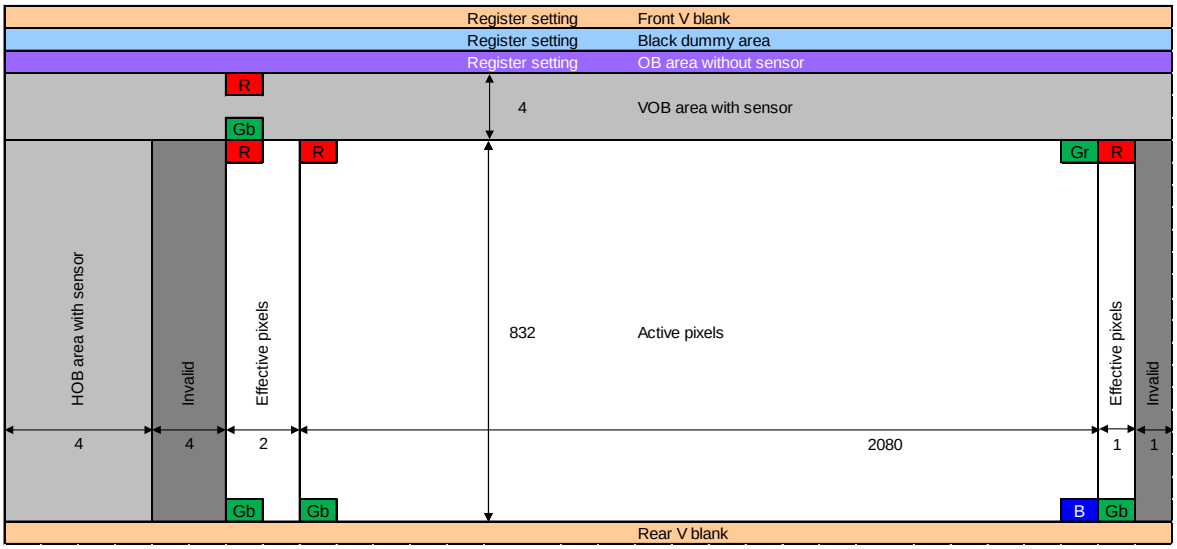


Fig. Readout Image Diagram in Mode13 Vertical 3/5 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

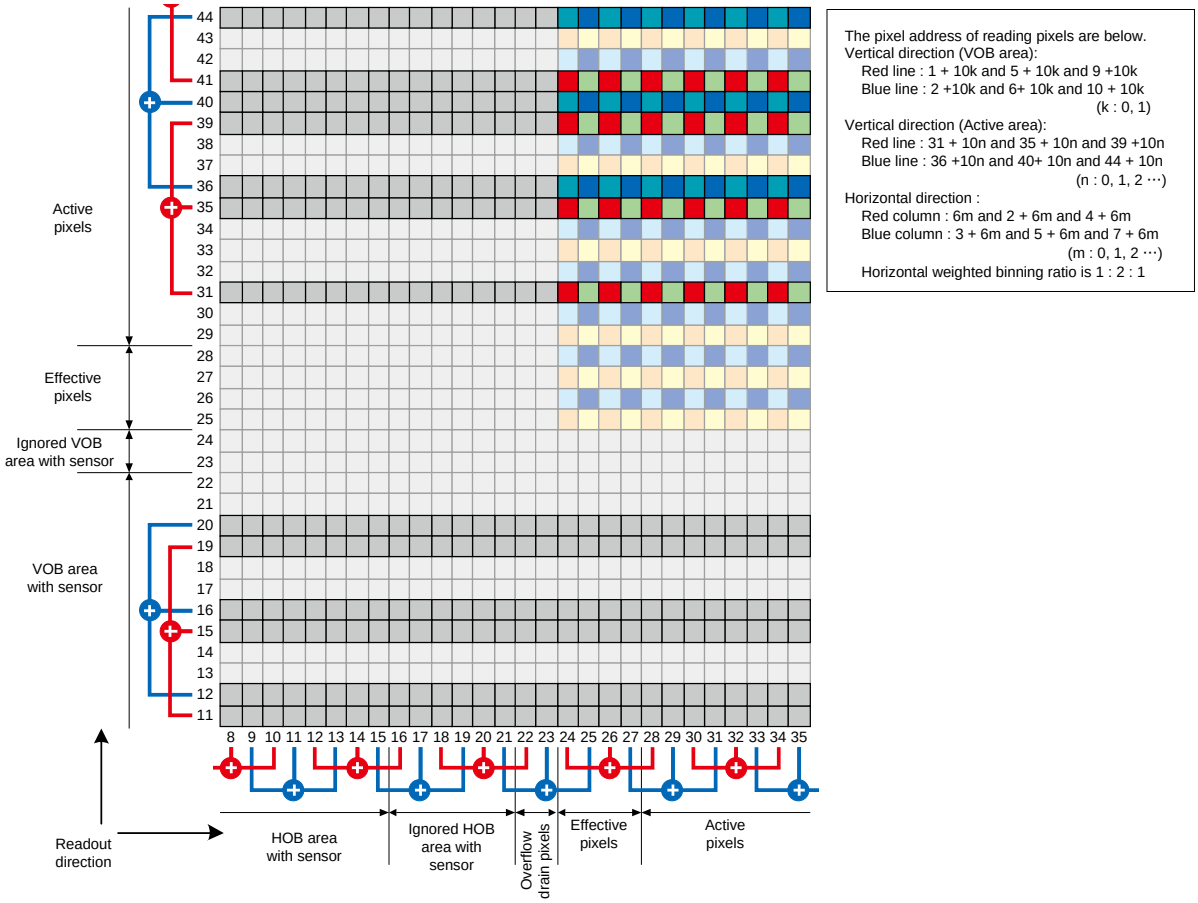


Fig. Binning Image

Timing Chart

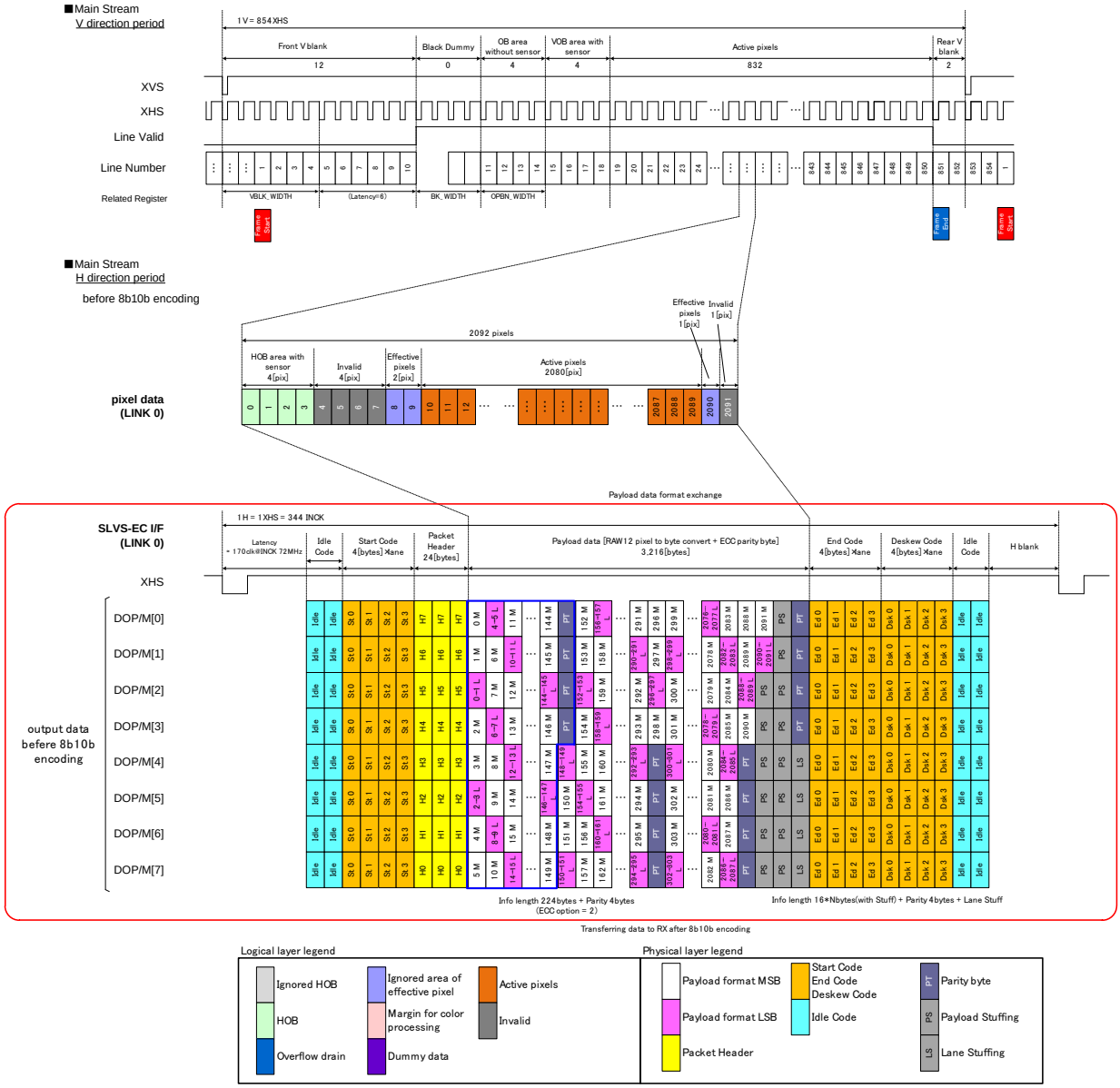


Fig. Drive Timing in Mode13 Vertical 3/5 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

Mode14: Vertical 1/7 Subsampling, Horizontal 3 Weighted Binning Readout Mode

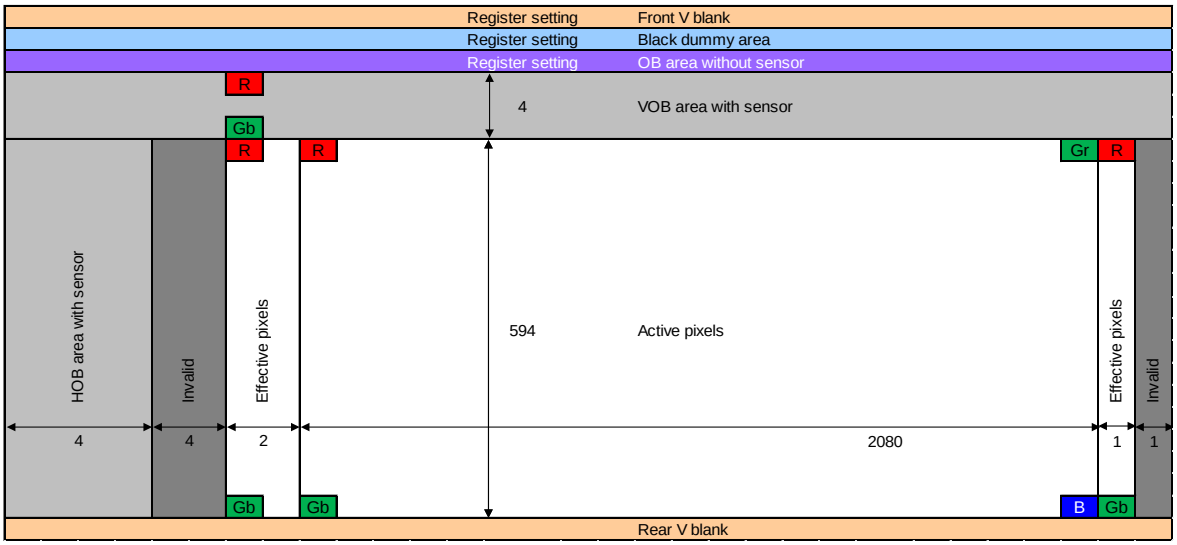


Fig. Readout Image Diagram in Mode14 Vertical 1/7 Subsampling, Horizontal 3 Weighted Binning Readout Mode

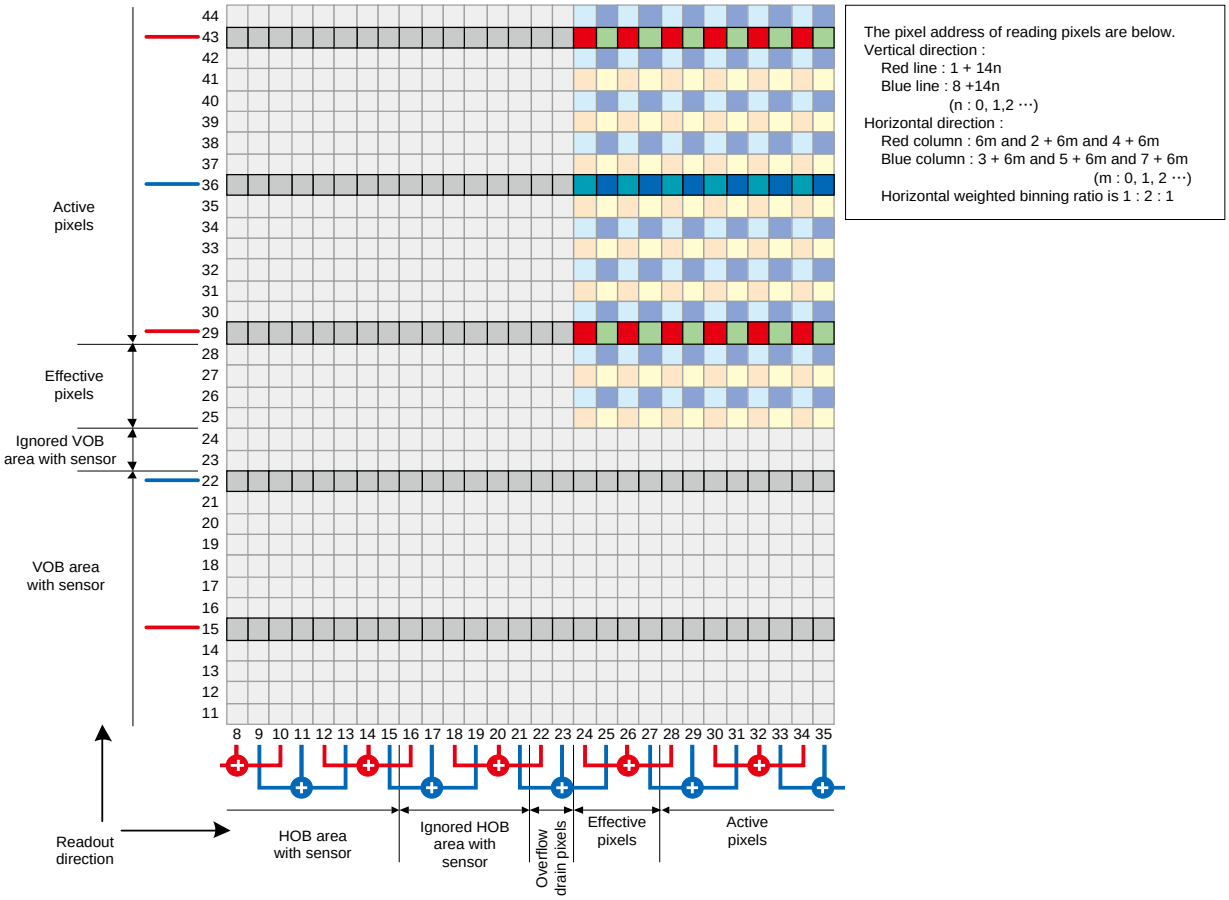


Fig. Binning Image

Timing Chart

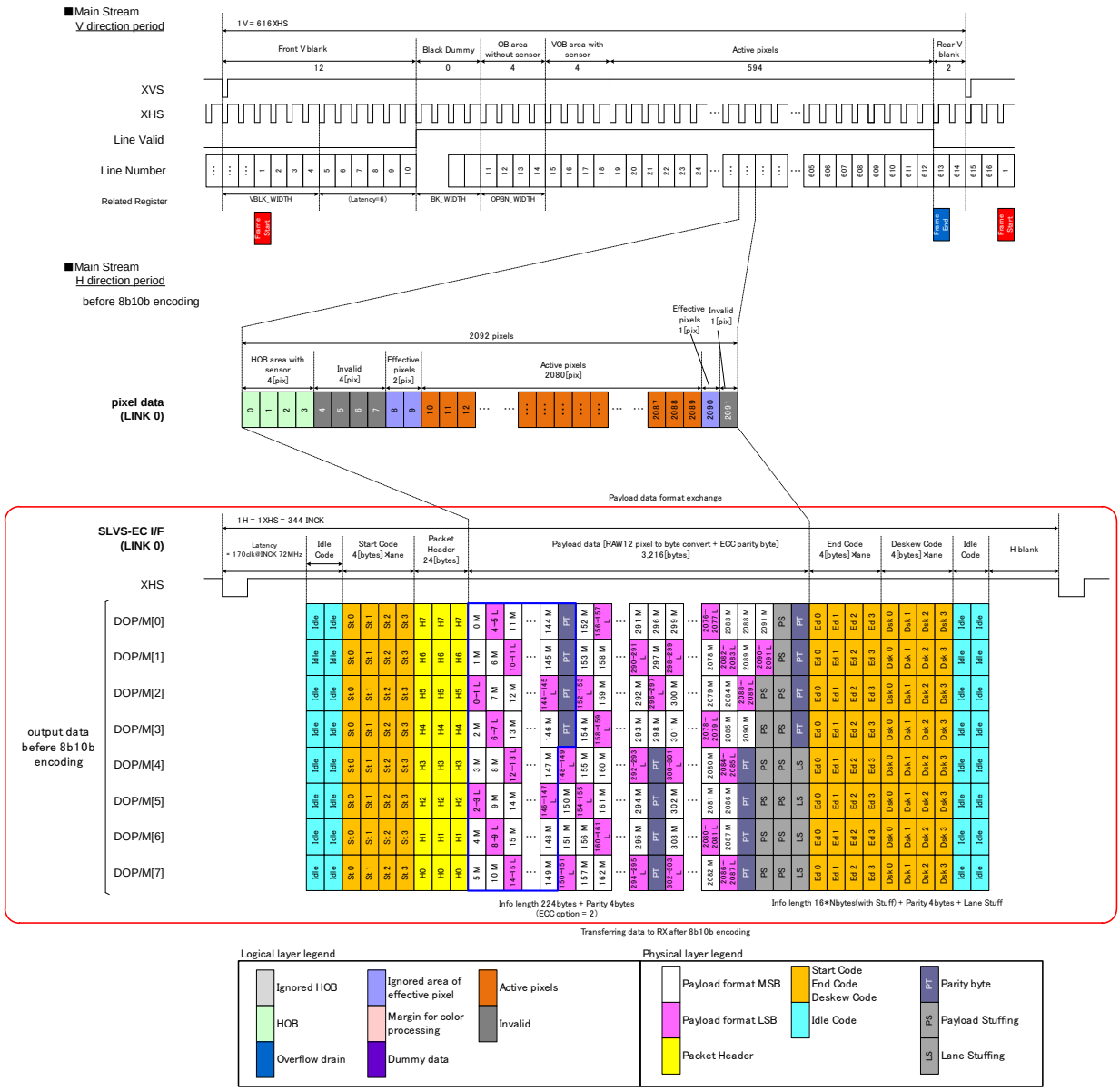


Fig. Drive Timing in Mode14 Vertical 1/7 Subsampling, Horizontal 3 Weighted Binning Readout Mode

Mode15: Vertical 3/7 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

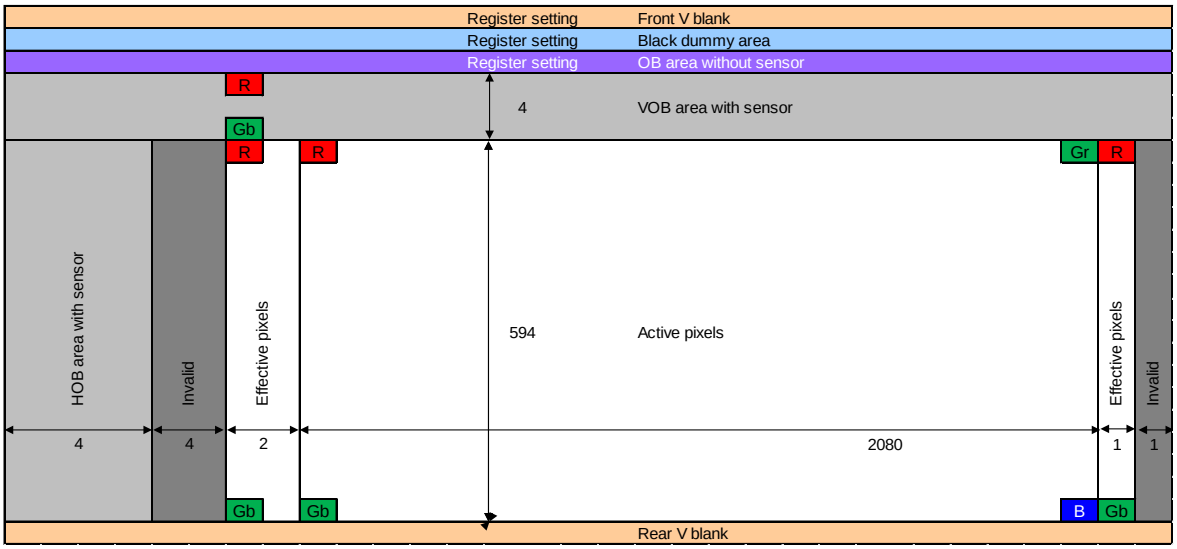


Fig. Readout Image Diagram in Mode15 Vertical 3/7 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

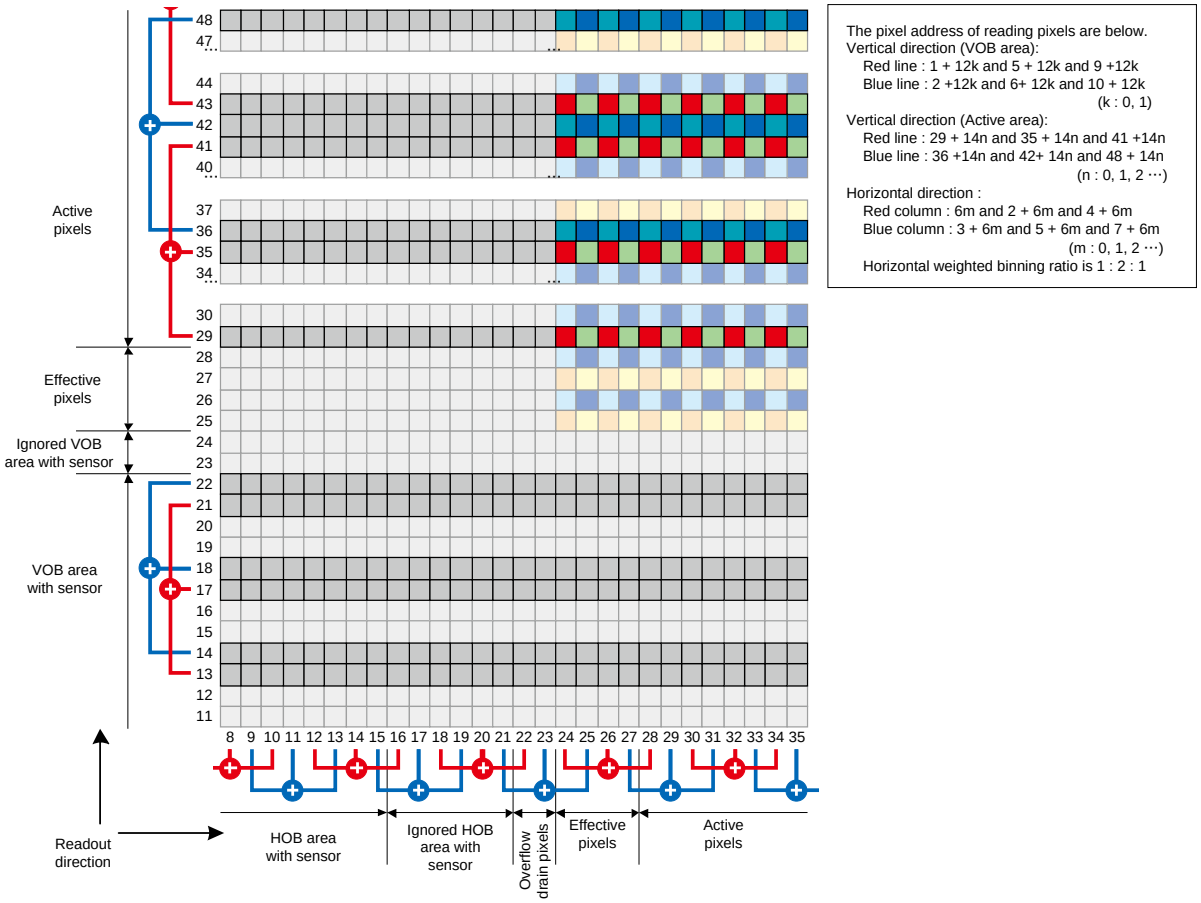


Fig. Binning Image

Timing Chart

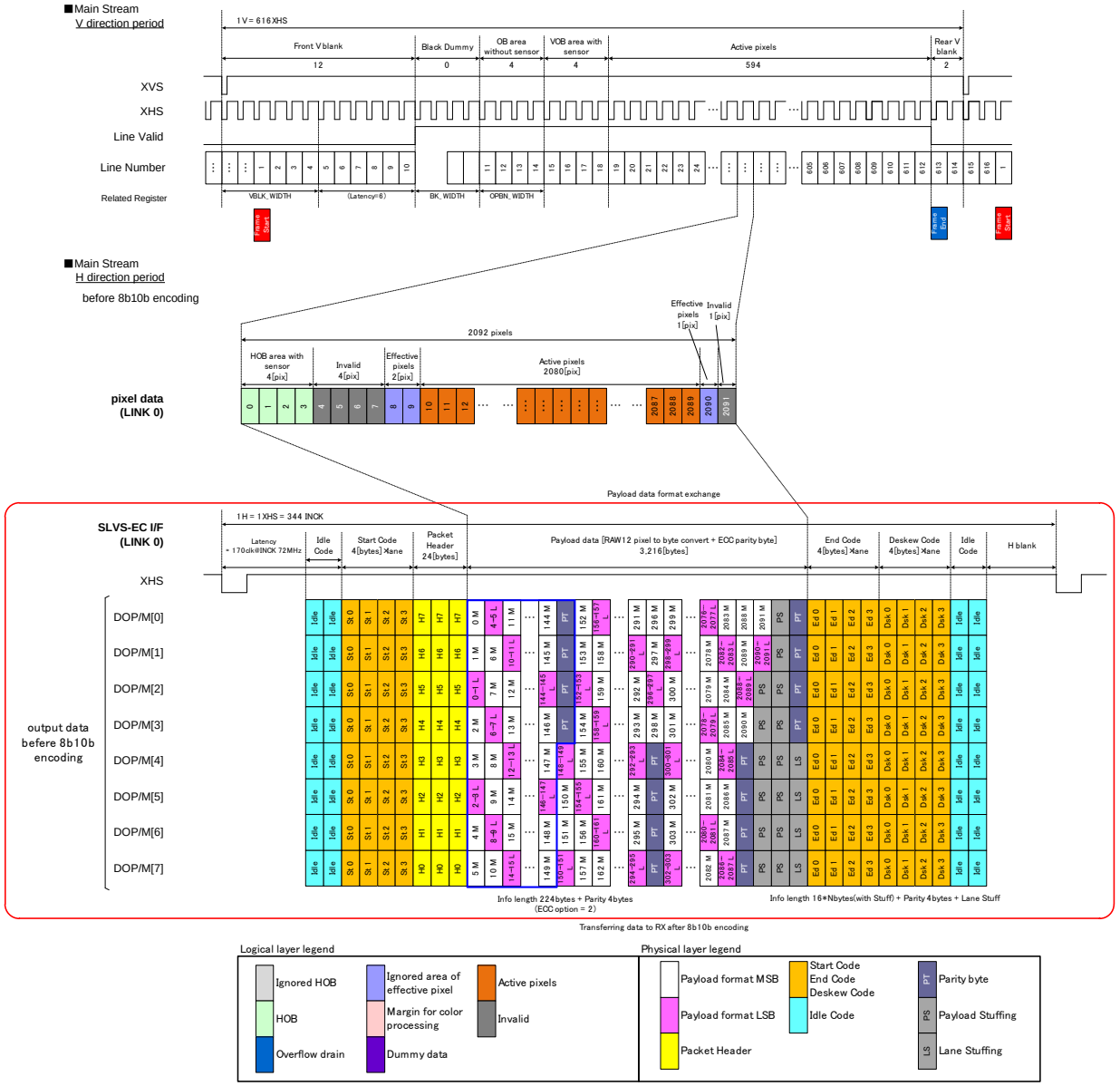


Fig. Drive Timing in Mode15 Vertical 3/7 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

Mode16: Vertical 1/9 Subsampling, Horizontal 3 Weighted Binning Readout Mode

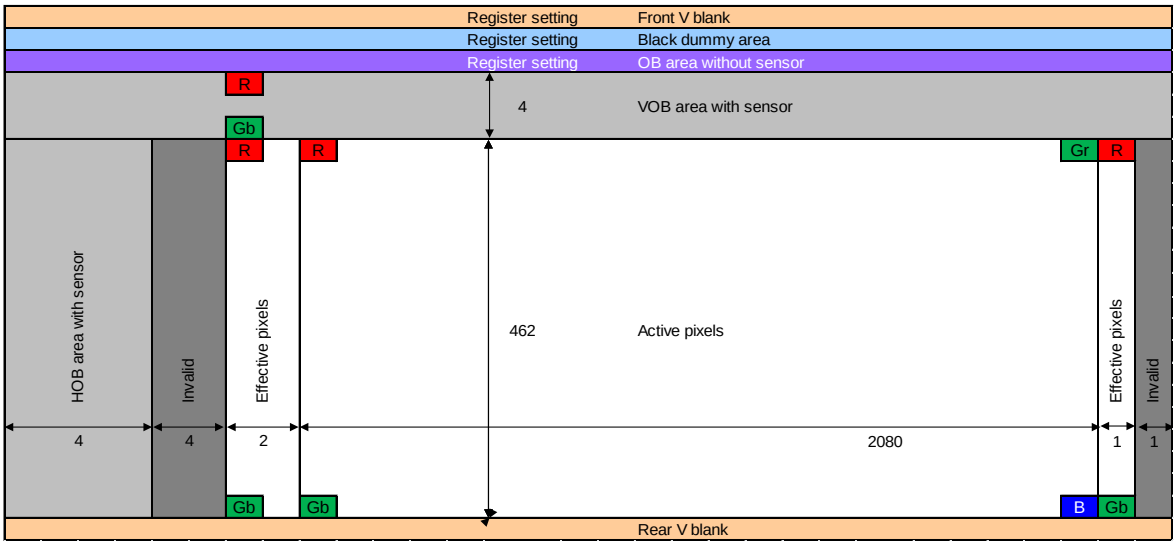


Fig. Readout Image Diagram in Mode16 Vertical 1/9 Subsampling, Horizontal 3 Weighted Binning Readout Mode

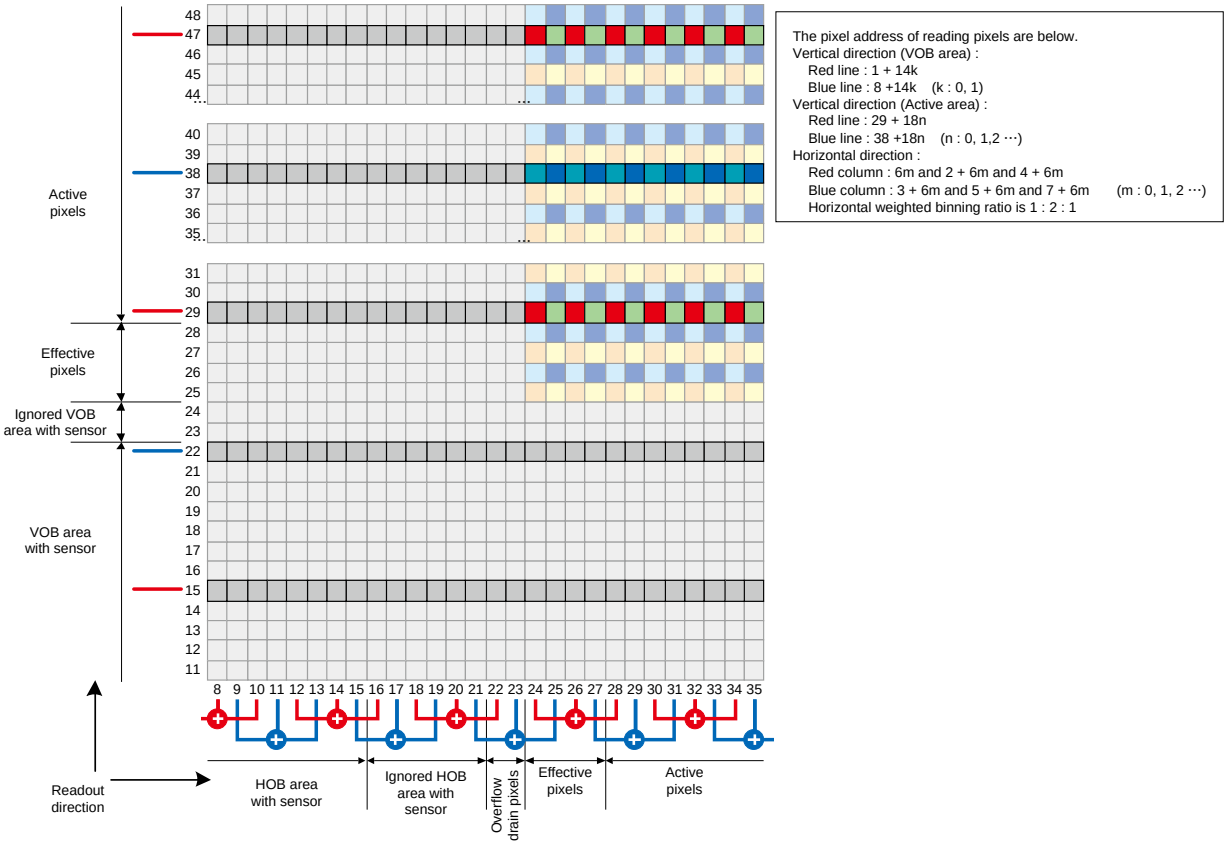


Fig. Binning Image

Timing Chart

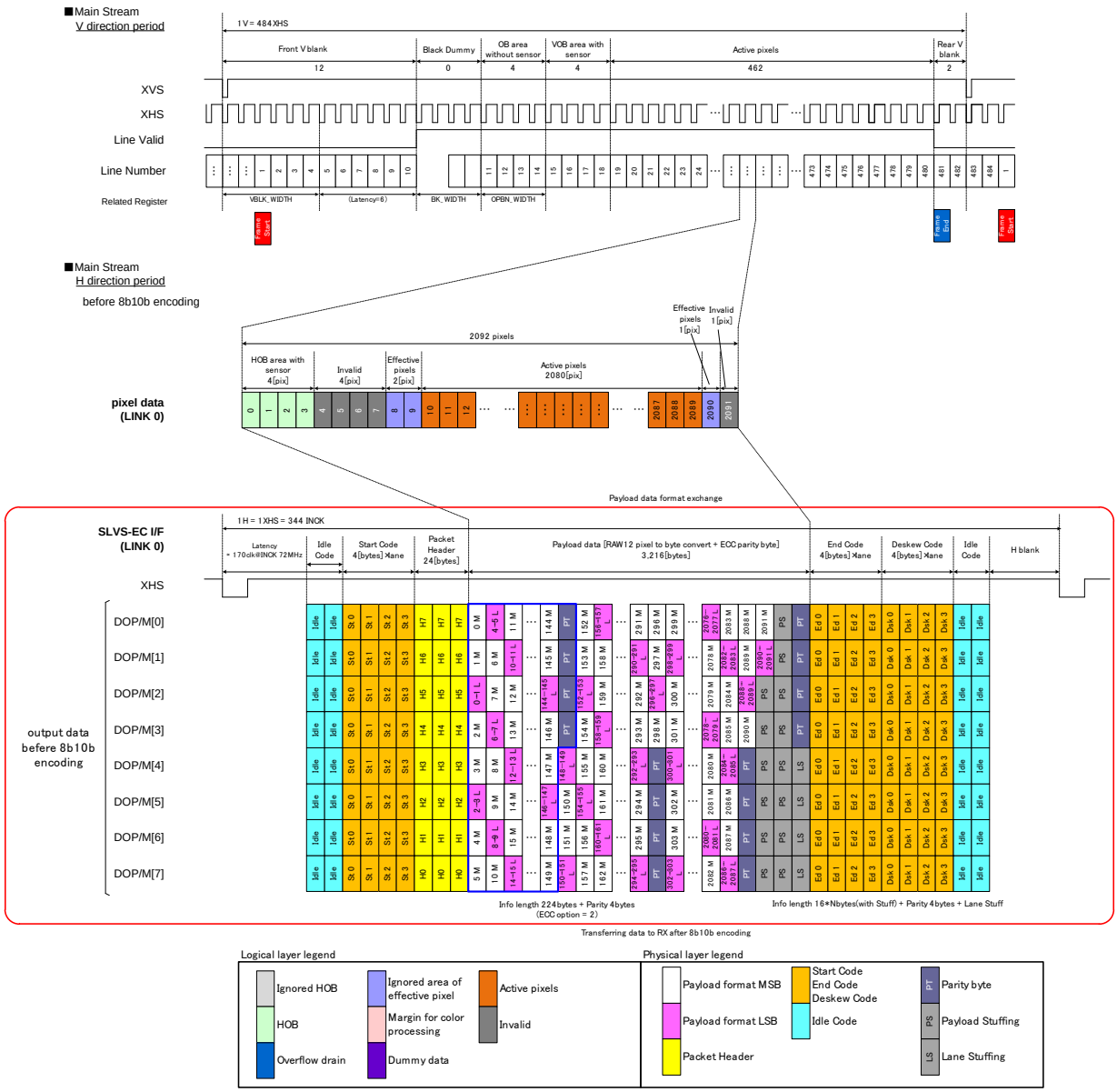


Fig. Drive Timing in Mode16 Vertical 1/9 Subsampling, Horizontal 3 Weighted Binning Readout Mode

Mode17: Vertical 3/9 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

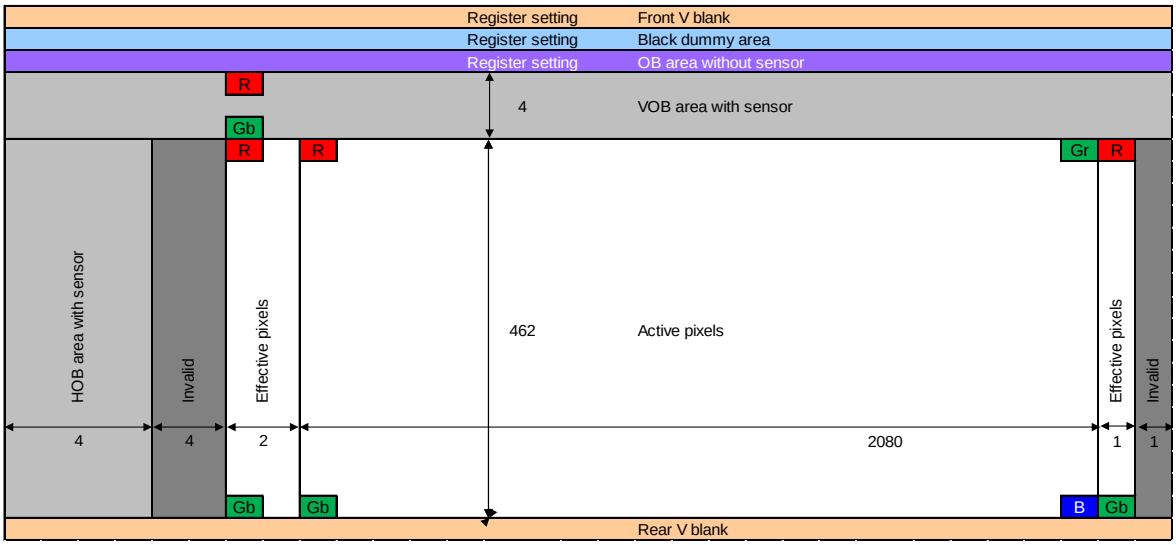


Fig. Readout Image Diagram in Mode17 Vertical 3/9 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

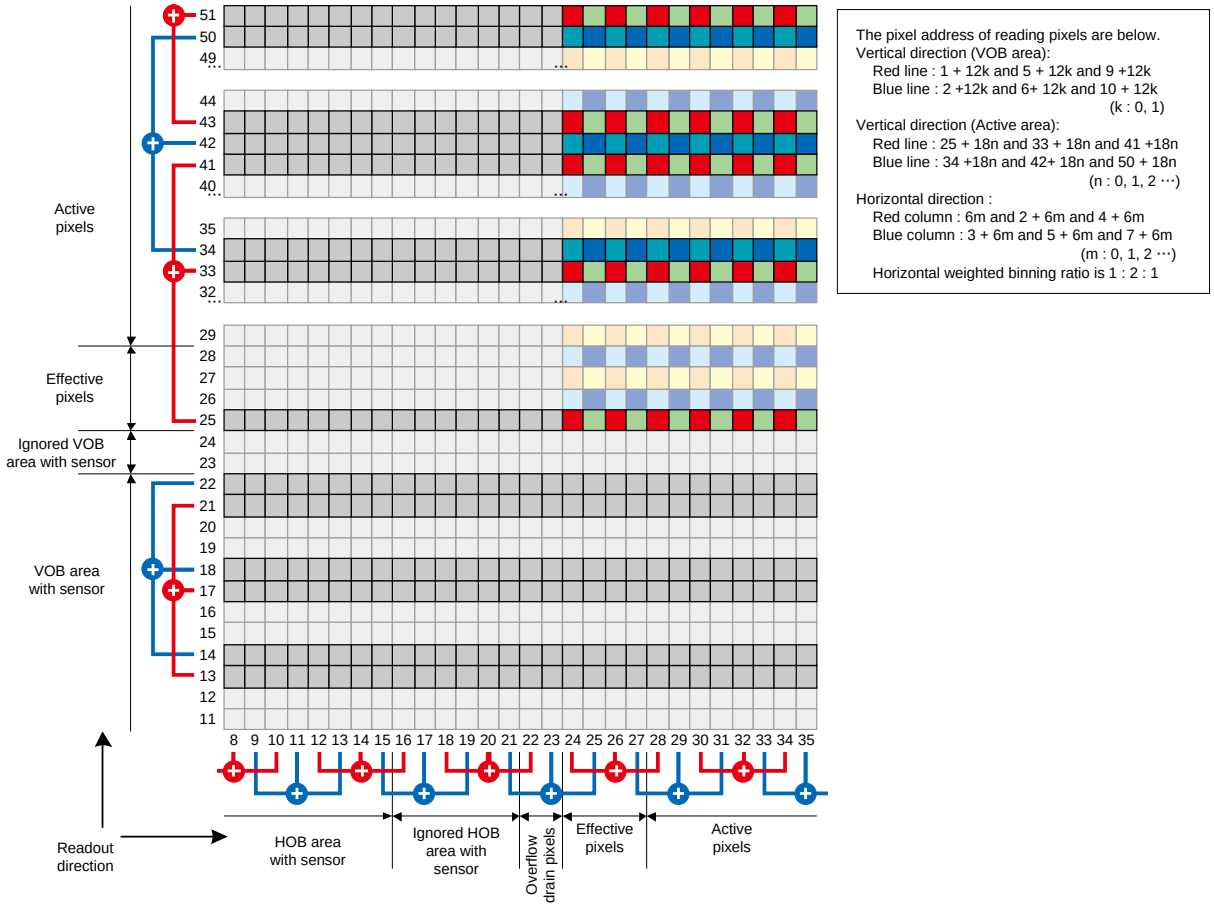


Fig. Binning Image

Timing Chart

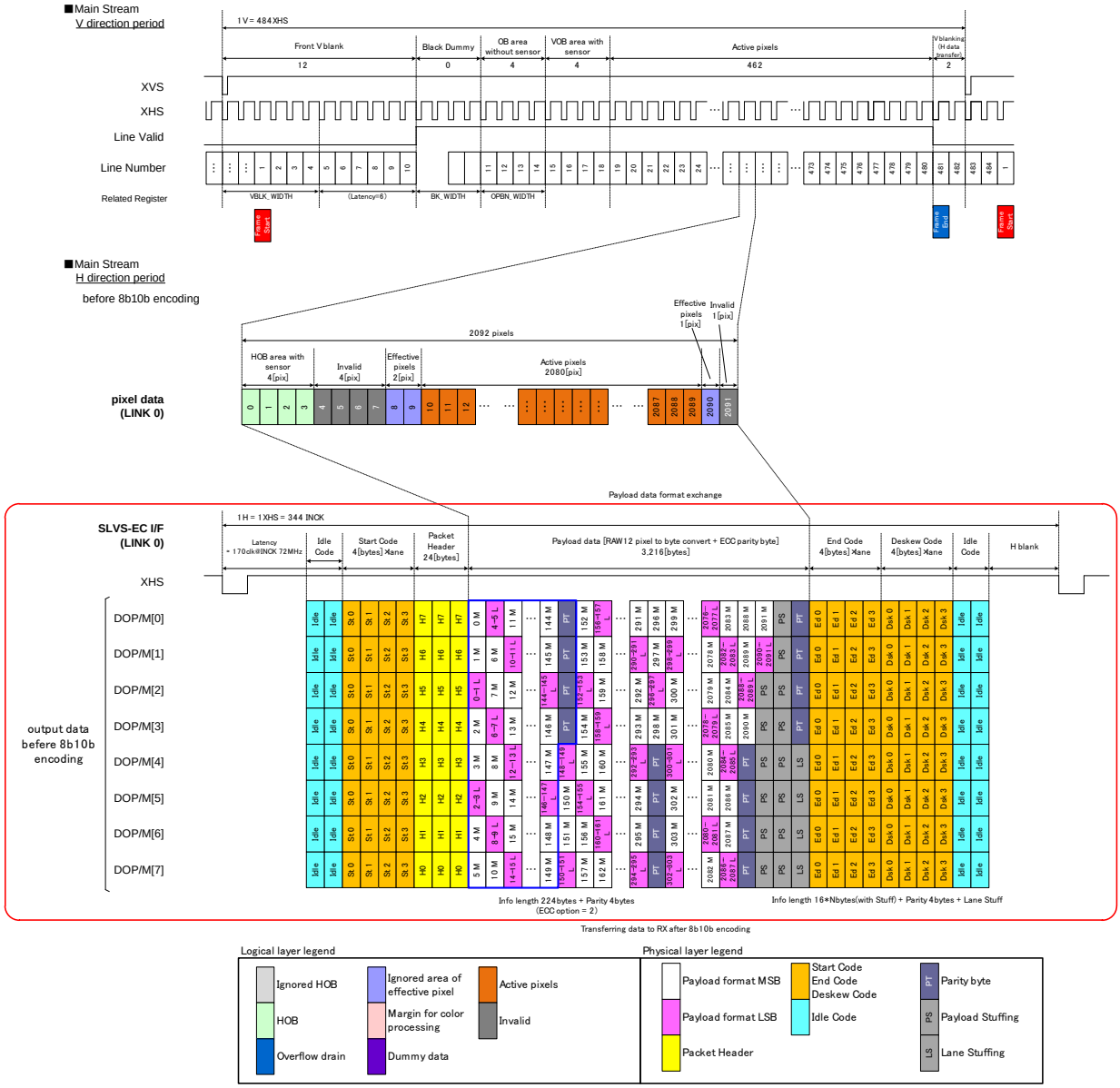


Fig. Drive Timing in Mode17 Vertical 3/9 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

Mode18: Vertical 1/13 Subsampling, Horizontal 3 Weighted Binning Readout Mode

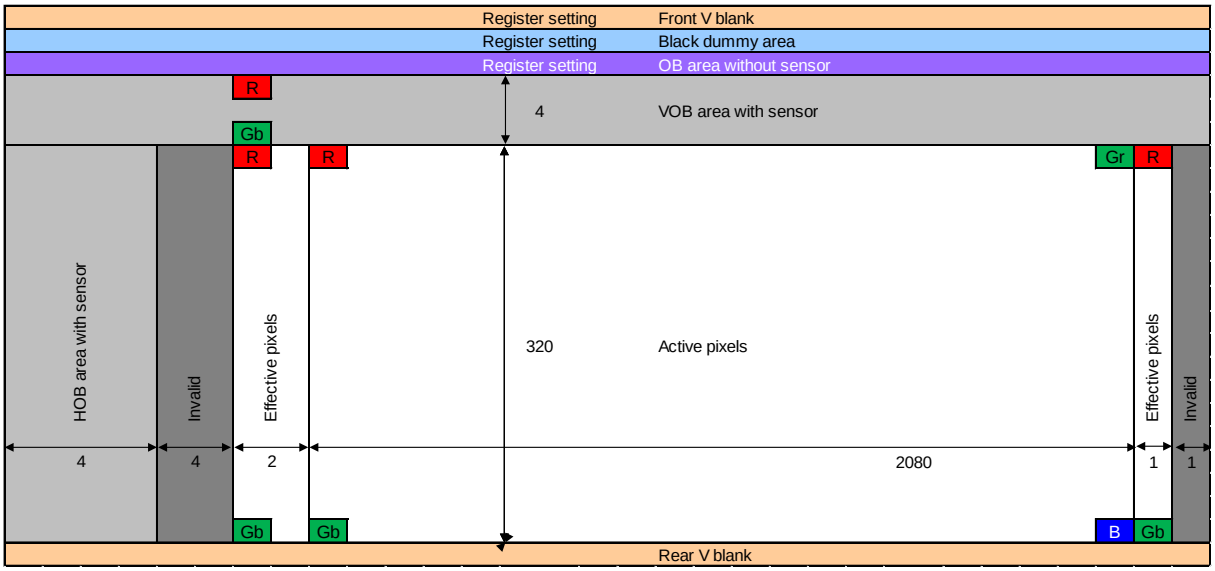


Fig. Readout Image Diagram in Mode18 Vertical 1/13 Subsampling, Horizontal 3 Weighted Binning Readout Mode

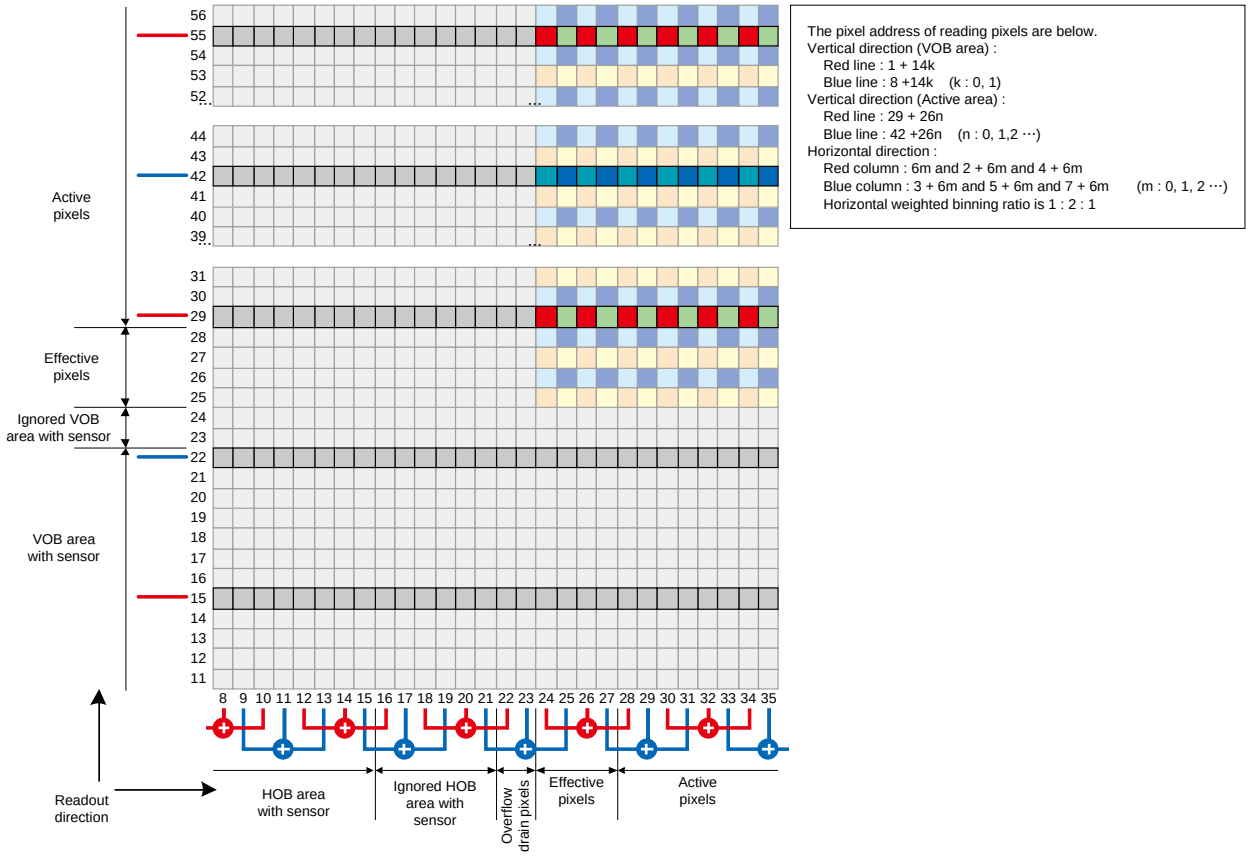


Fig. Binning Image

Timing Chart

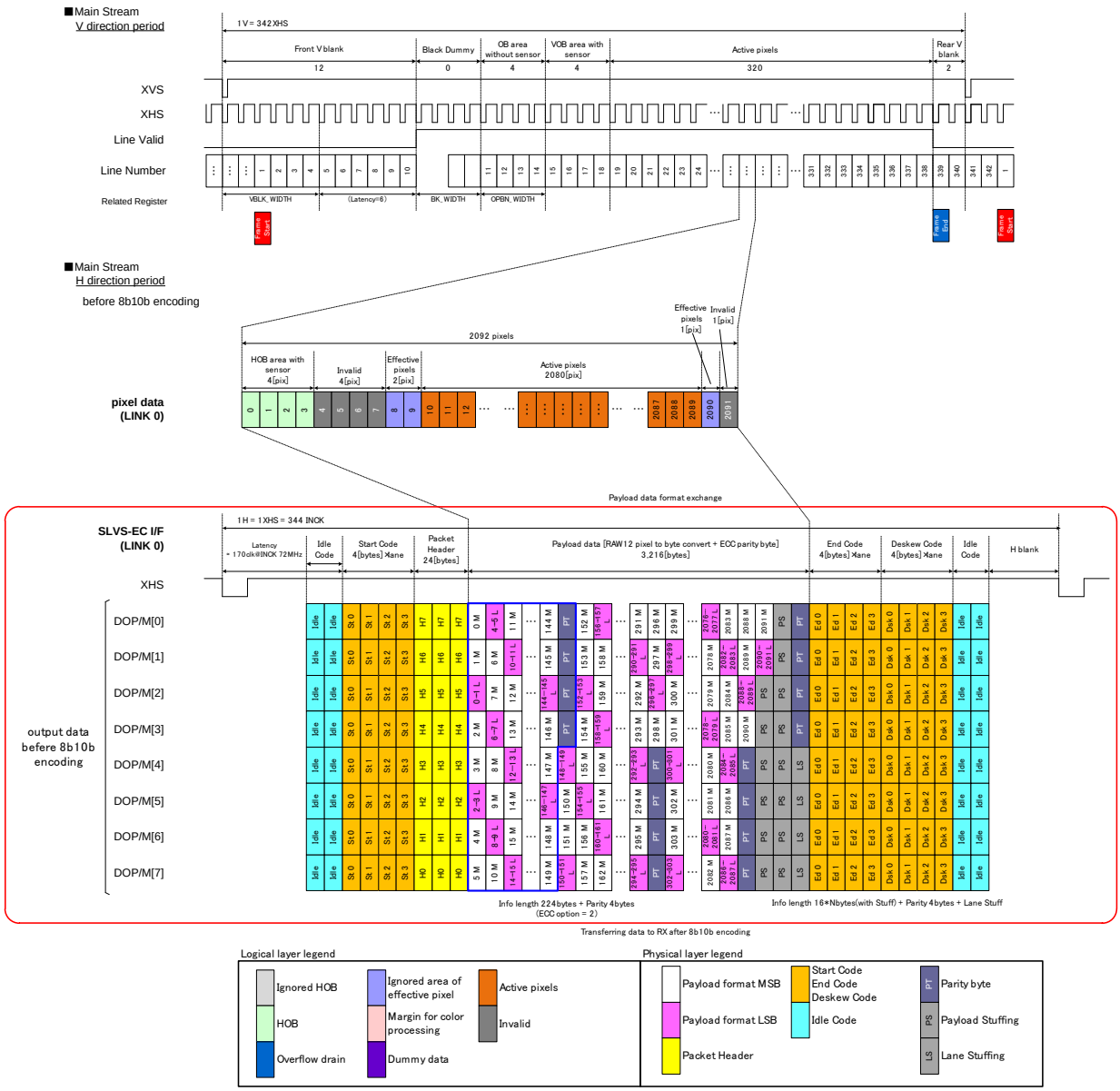


Fig. Drive Timing in Mode18 Vertical 1/13 Subsampling, Horizontal 3 Weighted Binning Readout Mode

Mode19: Vertical 3/13 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

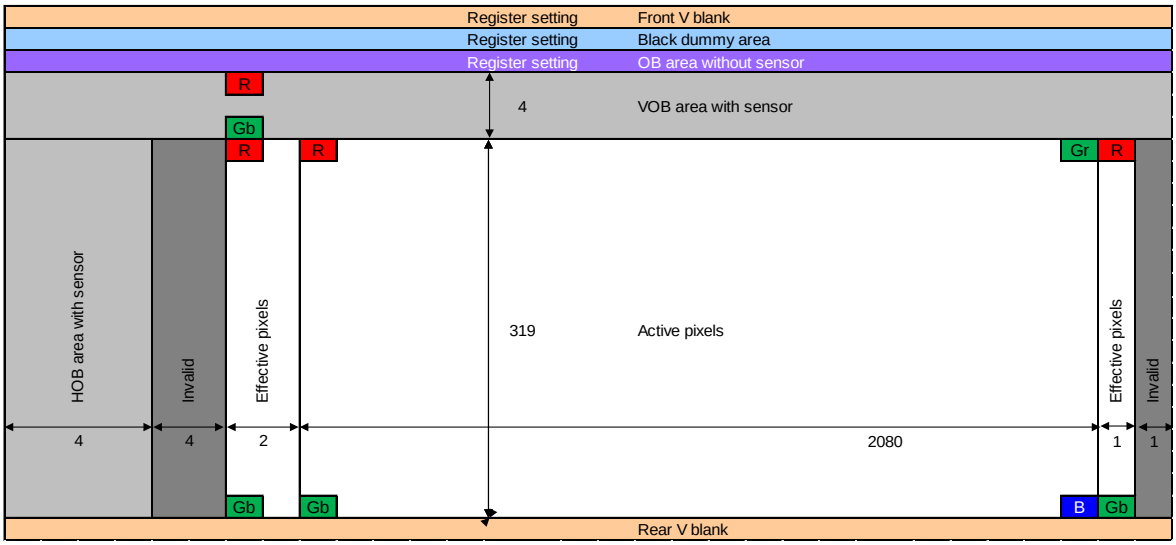


Fig. Readout Image Diagram in Mode19 Vertical 3/13 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

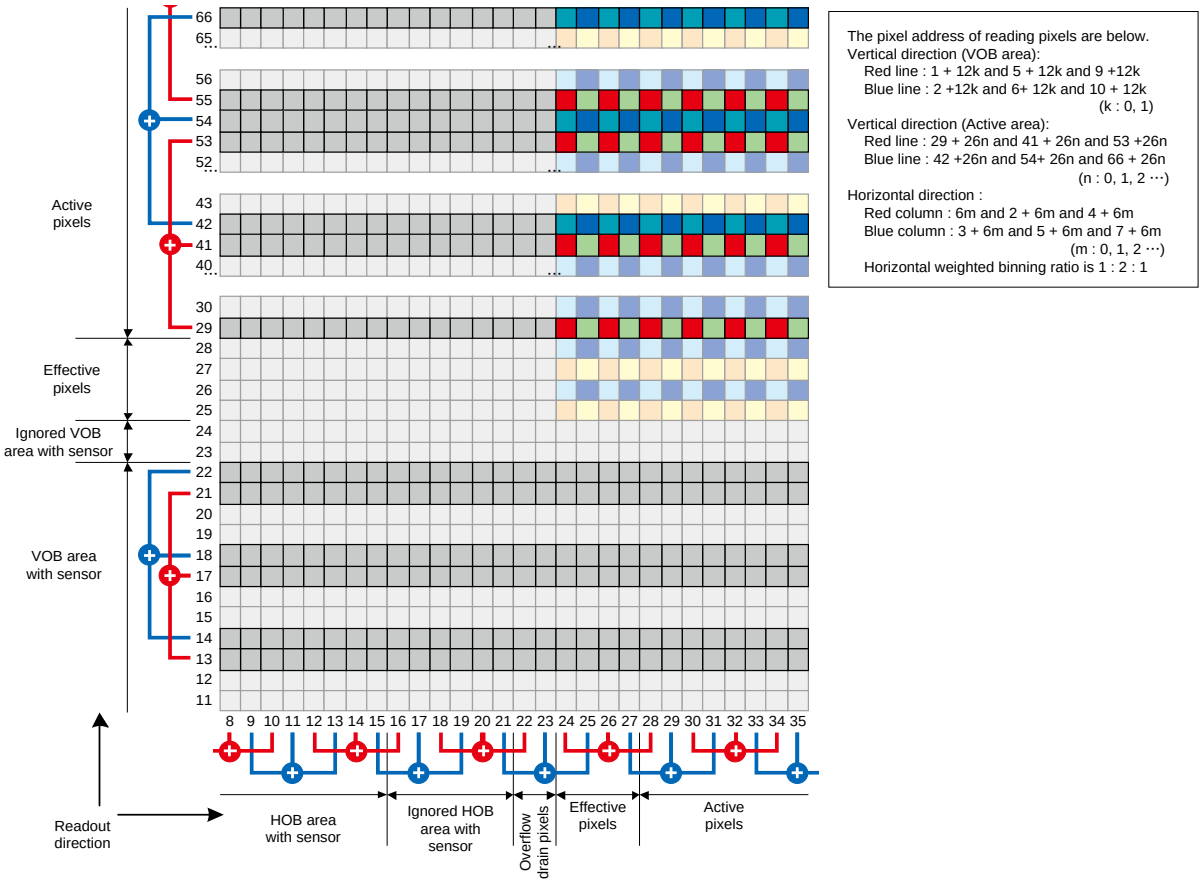


Fig. Binning Image

Timing Chart

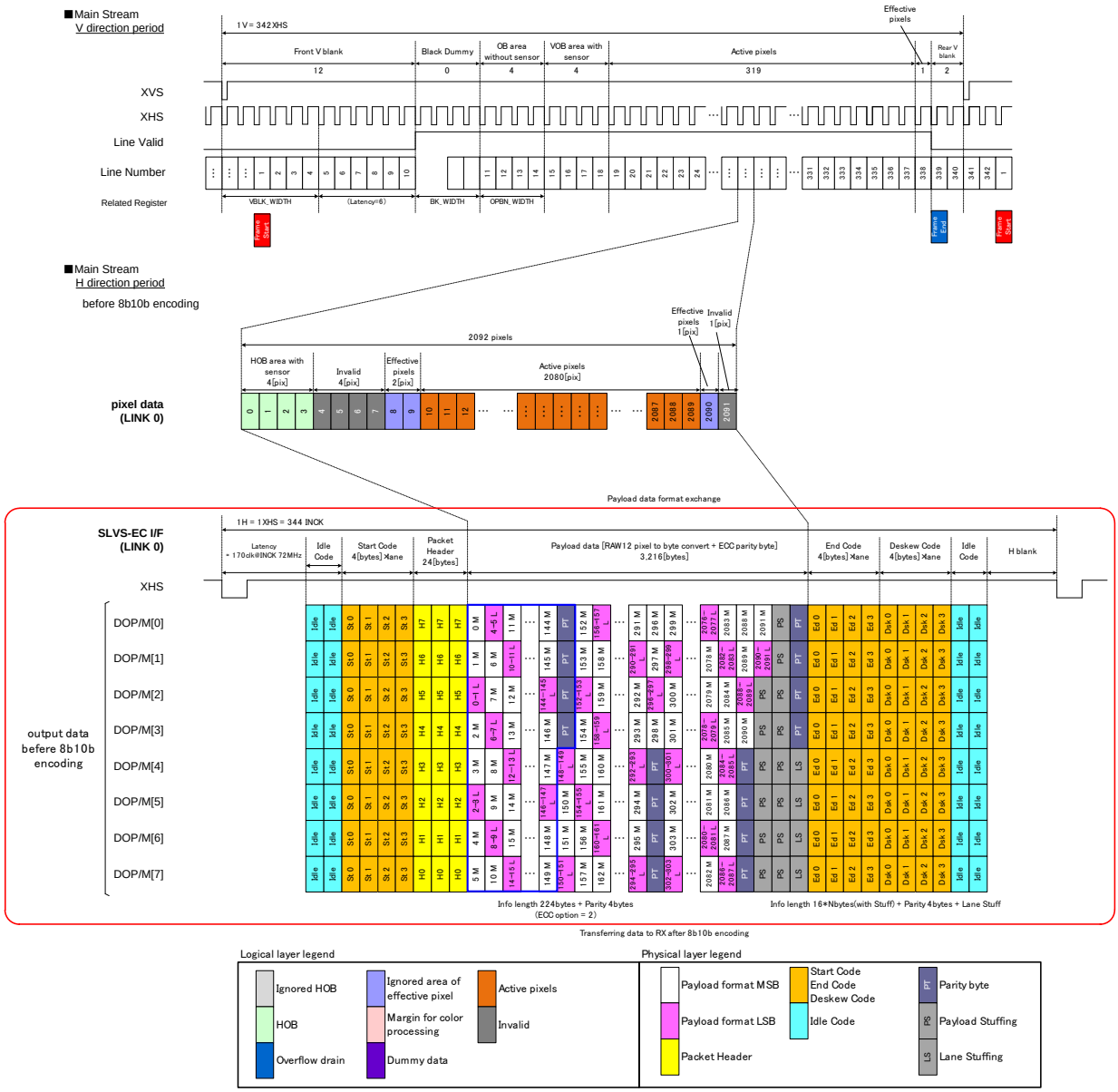


Fig. Drive Timing in Mode19 Vertical 3/13 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

Mode20: Vertical 1/25 Subsampling, Horizontal 3 Weighted Binning Readout Mode

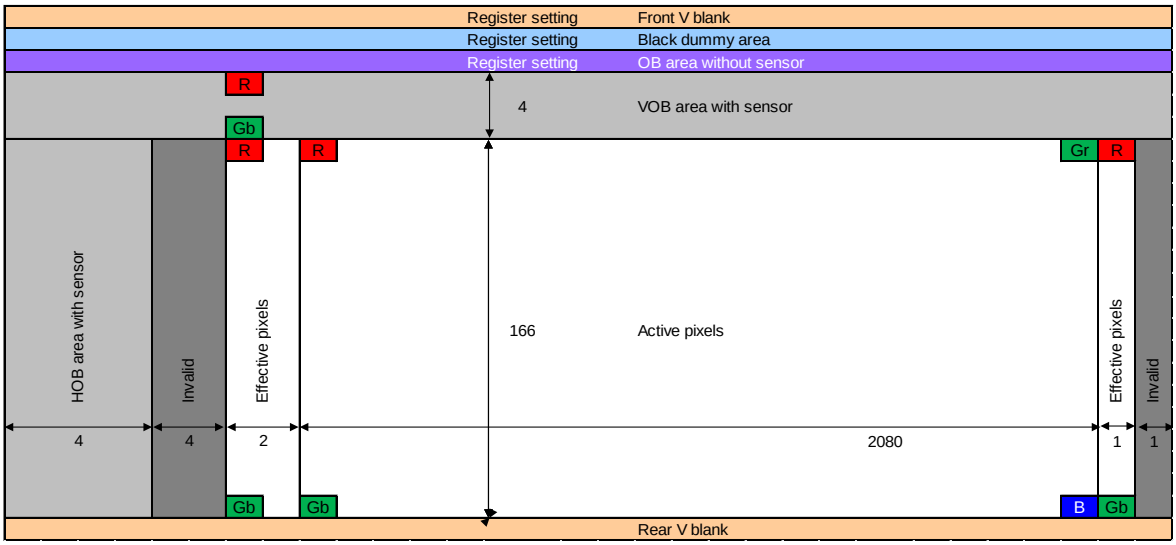


Fig. Readout Image Diagram in Mode20 Vertical 1/25 Subsampling, Horizontal 3 Weighted Binning Readout Mode

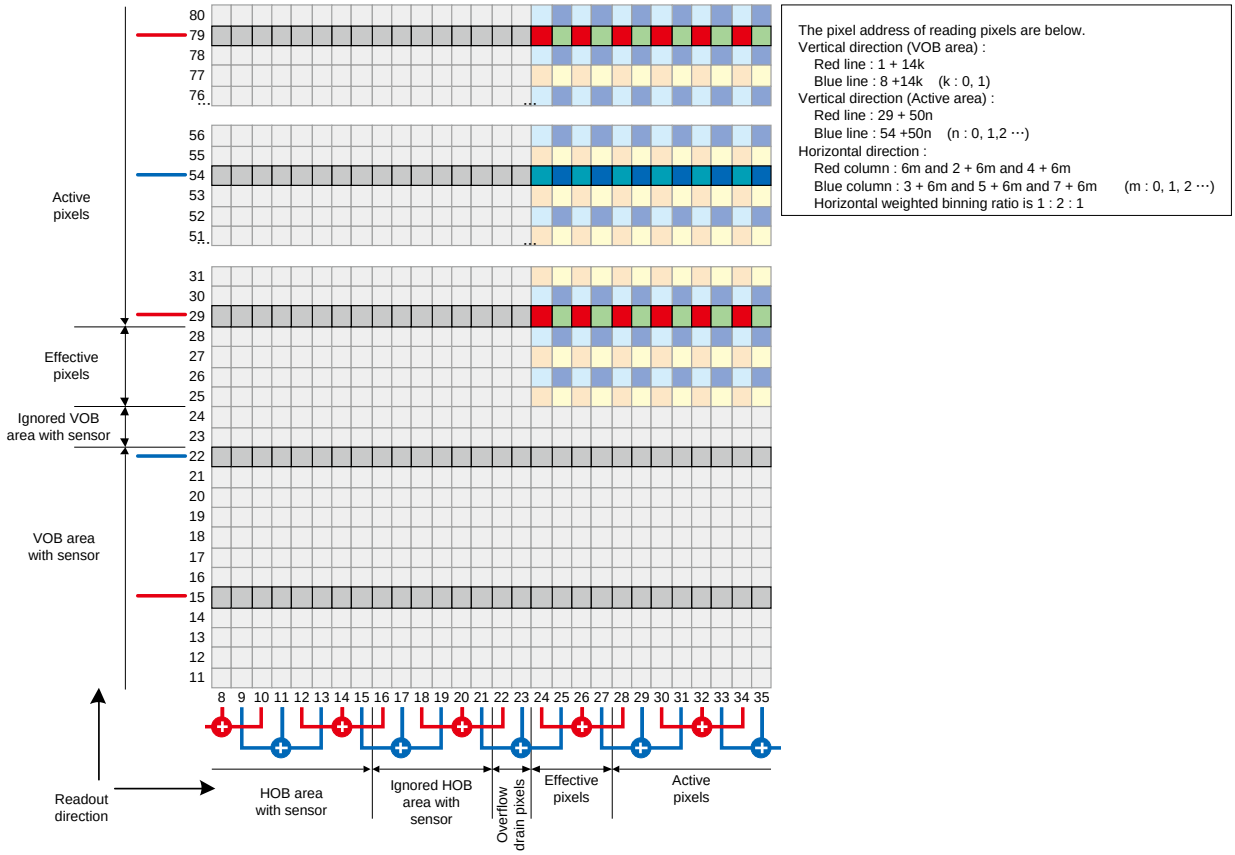


Fig. Binning Image

Timing Chart

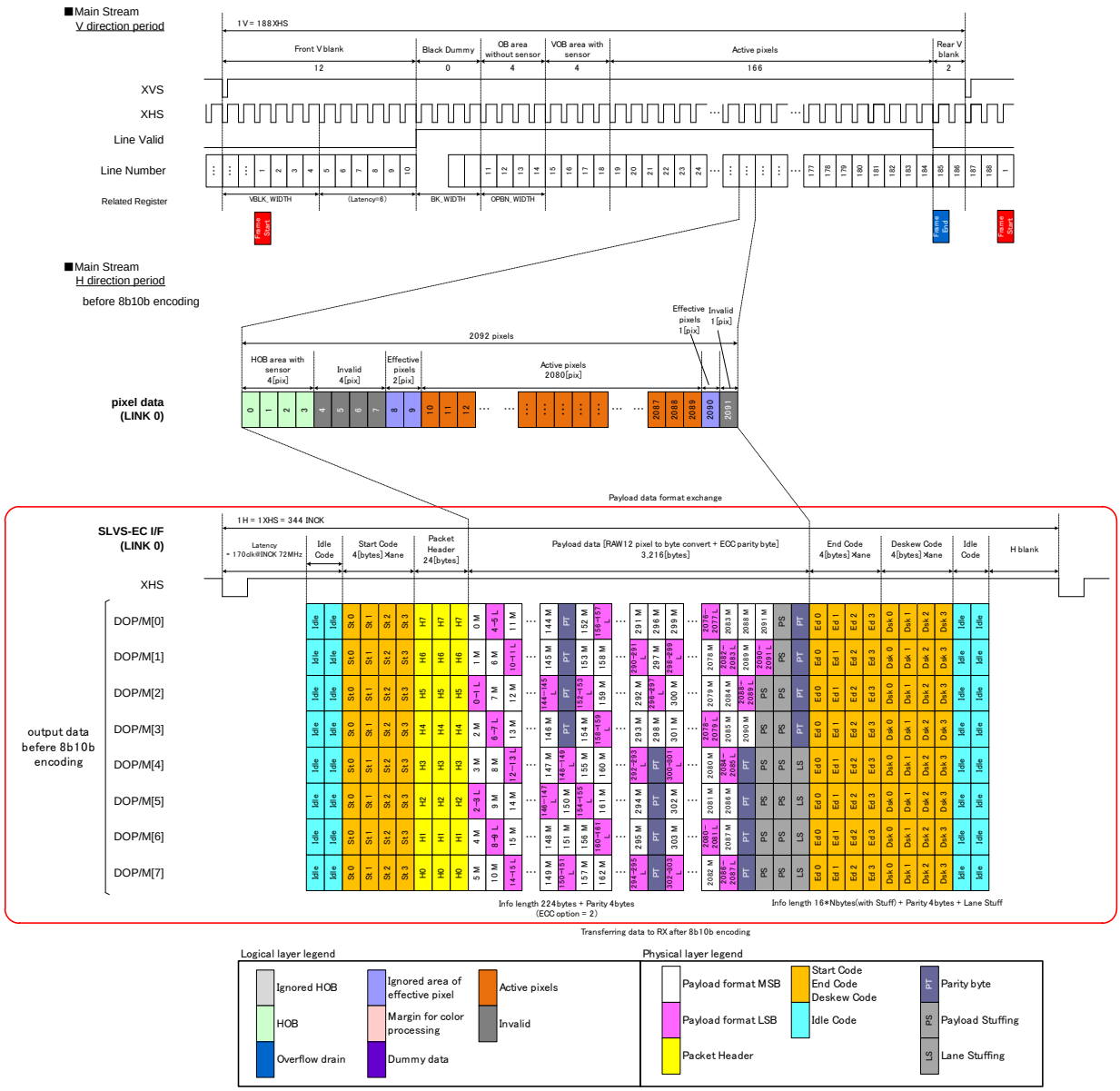


Fig. Drive Timing in Mode20 Vertical 1/25 Subsampling, Horizontal 3 Binning Readout Mode

Mode21: Vertical 3/25 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

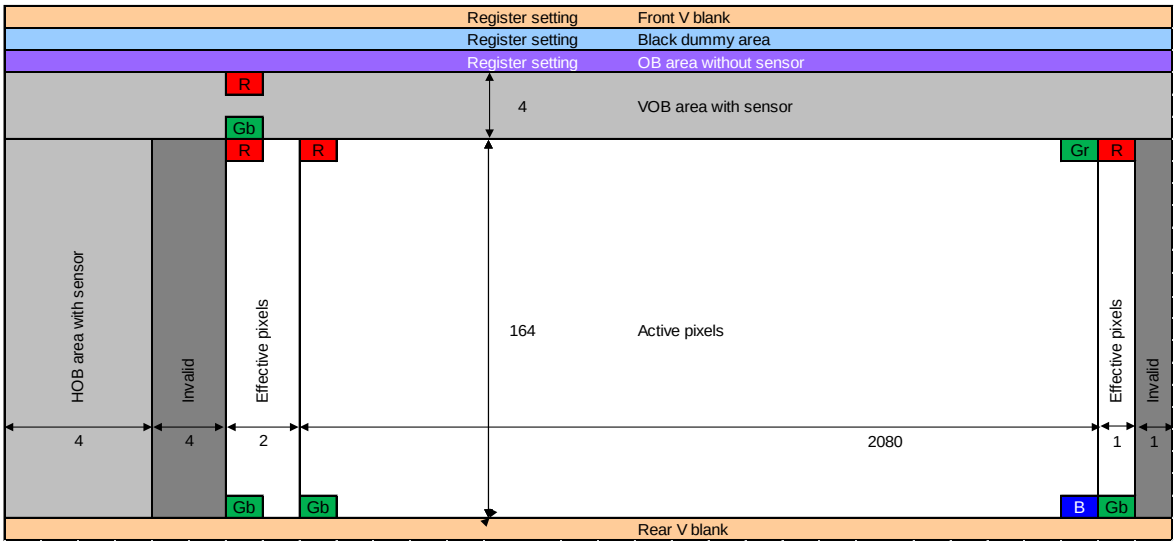


Fig. Readout Image Diagram in Mode21 Vertical 3/25 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

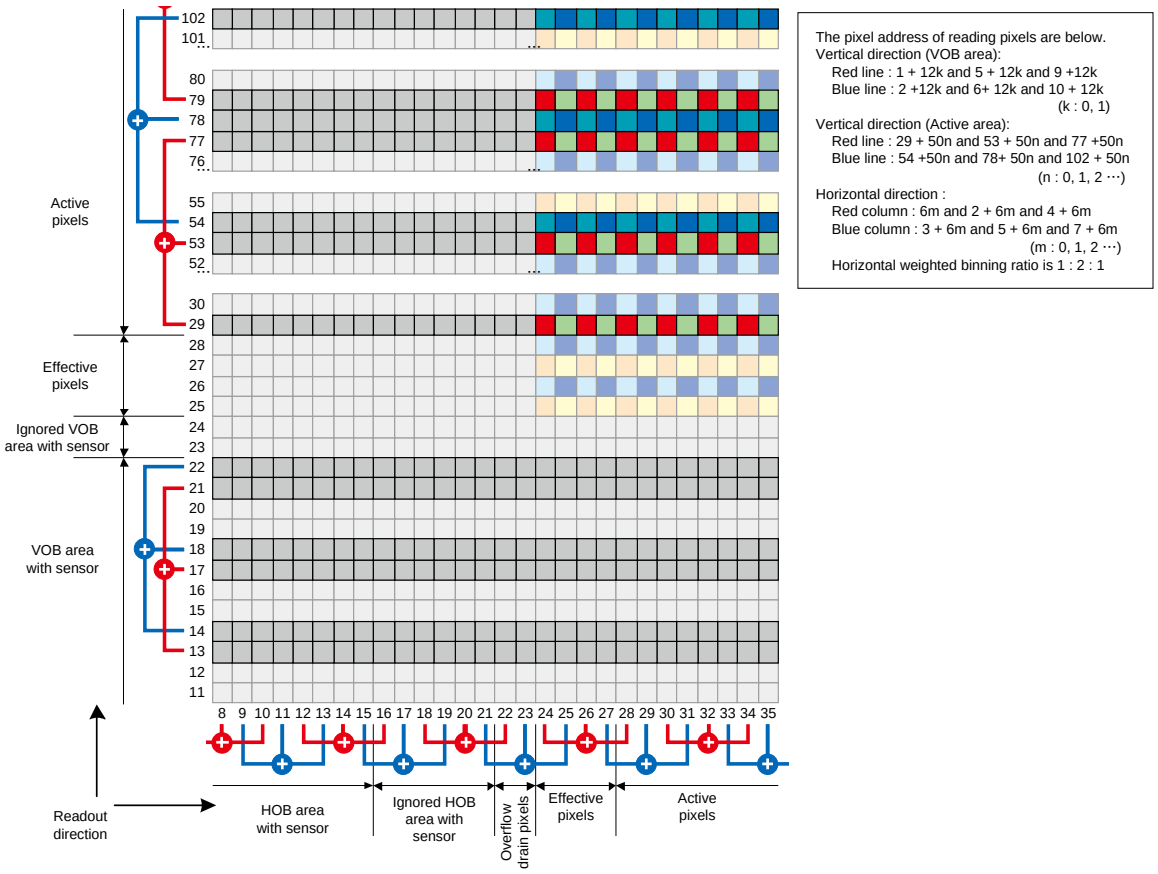


Fig. Binning Image

Timing Chart

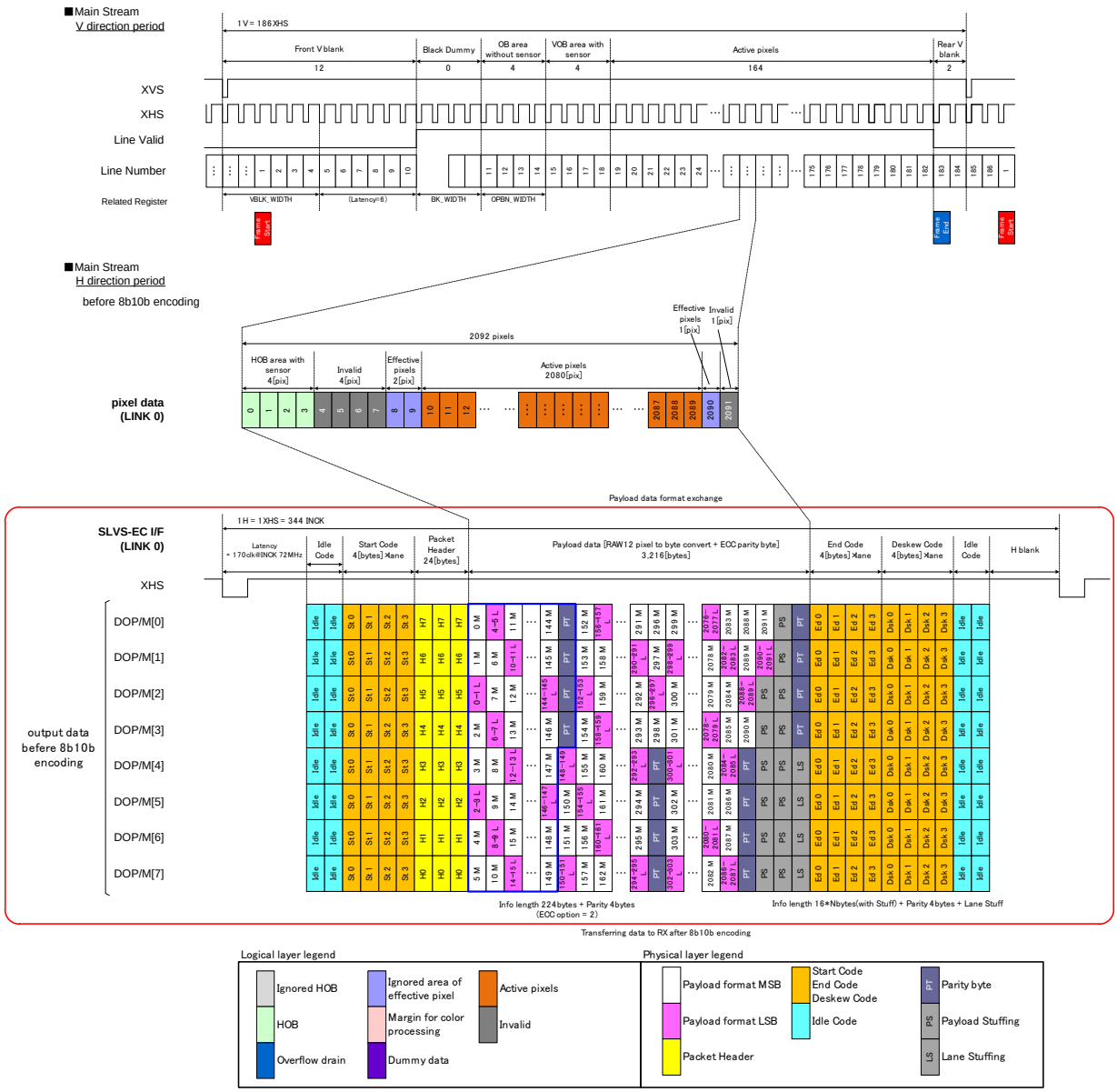


Fig. Drive Timing in Mode21 Vertical 3/25 Subsampling Binning, Horizontal 3 Weighted Binning Readout Mode

Window Readout Function

After scanning Black dummy area (register setting), VOB without sensor (register setting) and VOB with sensor pixels, the specified window area is scanned.

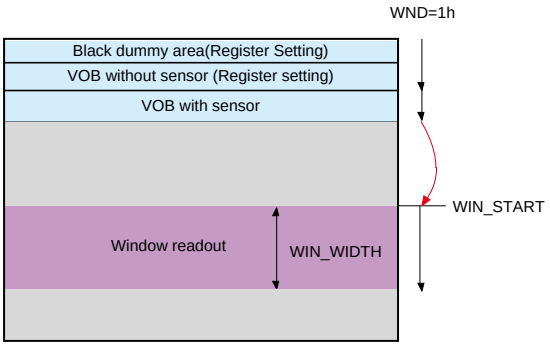


Fig. Scanning image or Window readout mode

The number of lines for Black dummy (variable) and VOB without sensor (variable) area is set by each register.
The number of lines for VOB with sensor readout changes according to drive mode. See the readout pixel image diagram of each mode described below.
The table below shows the restrictions for the readout start line and window readout area designation in each mode.

Table. Restrictions for Window Readout Setting Register in Each Mode (n = 0, 1, 2, … m = 0, 1, 2, …)

Mode No.	Readout mode	Restriction of readout start line designation [WIN_START]	Window readout area designation [WIN_WIDTH]
0	All-pixel readout mode	25 + 2 × n	2 × (m + 1)
1	All-pixel readout mode 2-parallel ADC readout	25 + 2 × n	2 × (m + 1)
3	All-pixel readout mode digital overlap drive	25 + 2 × n	2 × (m + 1)
5	Vertical 2/2-line and horizontal 2/2-line weighted binning readout mode	25 + 4 × n	2 × (m + 1)
6	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode	25 + 6 × n	2 × (m + 1)
7	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode	25 + 6 × n	2 × (m + 2) *1
10	Vertical1/3 subsampling, horizontal 3 weighted binning readout mode digital overlap drive	25 + 6 × n	2 × (m + 1)
11	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode digital overlap drive	25 + 6 × n	2 × (m + 2) *1
12	Vertical 1/5 subsampling, horizontal 3 weighted binning readout mode	31 + 10 × n	2 × (m + 1)
13	Vertical 3/5 subsampling binning, horizontal 3 weighted binning readout mode	31 + 10 × n	2 × (m + 1)
14	Vertical 1/7 subsampling, horizontal 3 weighted binning readout mode	29 + 14 × n	2 × (m + 1)
15	Vertical 3/7 subsampling binning, horizontal 3 weighted binning readout mode	29 + 14 × n	2 × (m + 1)
16	Vertical 1/9 subsampling, horizontal 3 weighted binning readout mode	29 + 18 × n	2 × (m + 1)
17	Vertical 3/9 subsampling binning, horizontal 3 weighted binning readout mode	29 + 18 × n	2 × (m + 1)

Mode No.	Readout mode	Restriction of readout start line designation [WIN_START]	Window readout area designation [WIN_WIDTH]
18	Vertical 1/13 subsampling, horizontal 3 weighted binning readout mode	29 + 26 × n	2 × (m + 1)
19	Vertical 3/13 subsampling binning, horizontal 3 weighted binning readout mode	29 + 26 × n	2 × (m + 1)
20	Vertical 1/25 subsampling, horizontal 3 weighted binning readout mode	29 + 50 × n	2 × (m + 1)
21	Vertical 3/25 subsampling binning, horizontal 3 weighted binning readout mode	29 + 50 × n	2 × (m + 1)

Note) The window readout start line is set by the physical arrangement address.
The window readout area is set by number of lines which is actually output as data. This area must be set in the effective pixel area in each readout modes.

*1 When vertical 3/3-line binning mode, the top 2 lines of the window readout area become invalid line.

Minimum value of 1V period when using Window Readout Function

When using Window Readout Function, the minimum value of 1V period [number of XHS] can be reduced according to the number of the reduced active vertical pixels.

1. In the case of digital overlap drive (Mode No. 3, 10, 11)
   The minimum value of 1V period can be reduced by twice as much as the number of the reduced active vertical pixels.
   For example, when number of active vertical pixels is reduced by 2 pixels in mode 3, the minimum value of 1V period can be reduced by 4 [number of XHS].

2. In the case of the mode other than digital overlap drive
   The minimum value of 1V period can be reduced as same as the number of the reduced active vertical pixels.
   For example, when number of active vertical pixels is reduced by 2 pixels in mode 0, the minimum value of 1V period can be also reduced by 2 [number of XHS].

Horizontal Freely Cropping Function

In horizontal all-pixel scan mode (mode0, 1, 3), horizontal cropping region of this sensor can be changed freely by the registers. Set the horizontal copping start position and number of horizontal output pixel.

Register Explanation

◆ HCROP_START_EN

It is a register enabled horizontal cropping start position setting register “HCROP_START” setting.

Name	Address	Bit	Register value	Function
HCROP_START_EN	00A7h	[0]	0h	Horizontal cropping start position setting disable
			1h	Horizontal cropping start position setting enable

◆ HCROP_WIDTH_EN

It is a register enabled horizontal cropping output width setting register “HCROP_WIDTH” setting.

Name	Address	Bit	Register value	Function
HCROP_WIDTH_EN	01D8h	[2]	0h	Horizontal cropping output width setting disable
			1h	Horizontal cropping output width setting enable

◆ HCROP_START

It is a register to set horizontal cropping start pixel position.

Name	Address	Bit	Register value	Remarks
HCROP_START [7:0]	00A8h	[7:0]	Horizontal cropping start position setting Start position = setting value × 16 [pixel width] (Reference position is after HOB area with sensor)	Setting range: 0d to 391d
HCROP_START [8]	00A9h	[0]		

◆ HCROP_WIDTH

It is a register to set horizontal cropping output width.

Name	Address	Bit	Register value	Remarks
HCROP_WIDTH [7:0]	01DDh	[7:0]	Horizontal cropping output width setting Output pixel width = setting value Setting value should be multiple of 4	Setting range: 4d to (6276 – HCROP_START × 16)
HCROP_WIDTH [14:8]	01DEh	[6:0]		

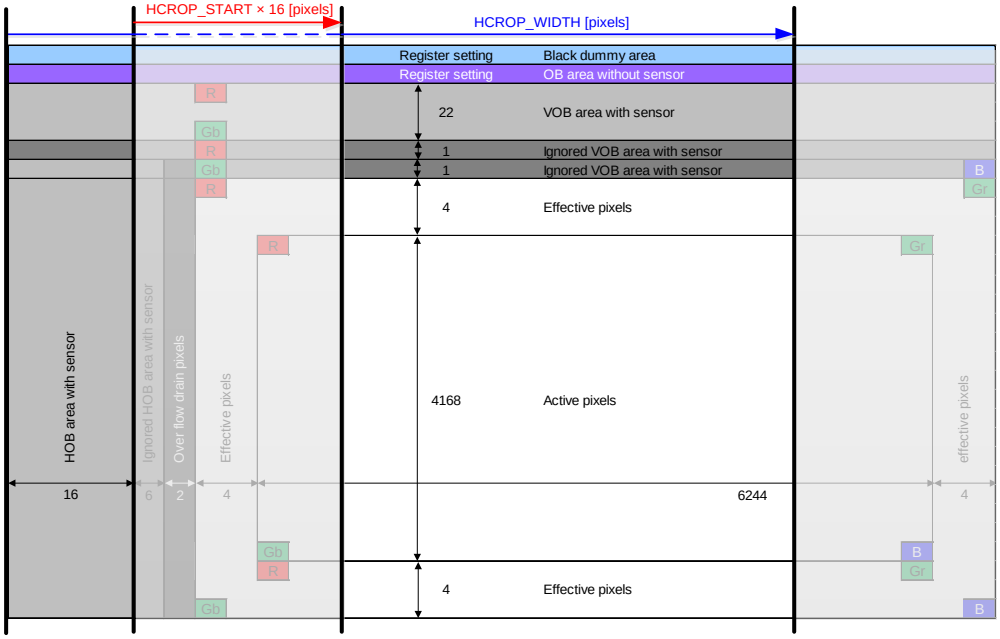


Fig. Output Image Diagram of Horizontal Freely Cropping

Black Level Setting

The Relation between BLKLEVEL_N / S registers and black level is shown below.

Table. Relation between BLKLEVEL _N / S Register and Black Level

AD bit	Word length	BLKLEVEL_N/ S setting default value	Output black level (Clamp level)	Remarks
16-bit	16-bit	0FFFh	FFFh	Same as register setting value
14-bit	14-bit		3FFh	1/4 of register setting value
12-bit	12-bit		FFh	1/16 of register setting value
11-bit	12-bit		FEh	1/16 of register setting value - 1
	10-bit		3Fh	1/64 of register setting value

Clamp Level Setting

A rough internal clamp works in this sensor to secure the dynamic range of the AD converter movement. It is recommended to process the clamp data by camera DSP in case of adjustment black level.

The clamp areas of this sensor are set in the black dummy area, the VOB area with sensor. The clamp level is set by the BLKLEVEL_N register and the BLKLEVEL_S register.

When the black dummy clamp operation is executed, set the CLPBKOFF register to 0h.
When the VOB clamp operation is executed, set the CLPOPBOFF register to 0h.

Note) Setting both CLPBKOFF and CLPOPBOFF to 0h is prohibited.

When the clamp function is not required, stop the function by setting the CLPOFF register to 1h.
The clamp function is available for still mode only.

The table below shows the setting method and restrictions for the CLPBK_VST and CLPOB_VST registers which set the clamp start line, and the CLPBK_V and CLPOB_V registers which set the clamp area of black dummy clamp and OB clamp

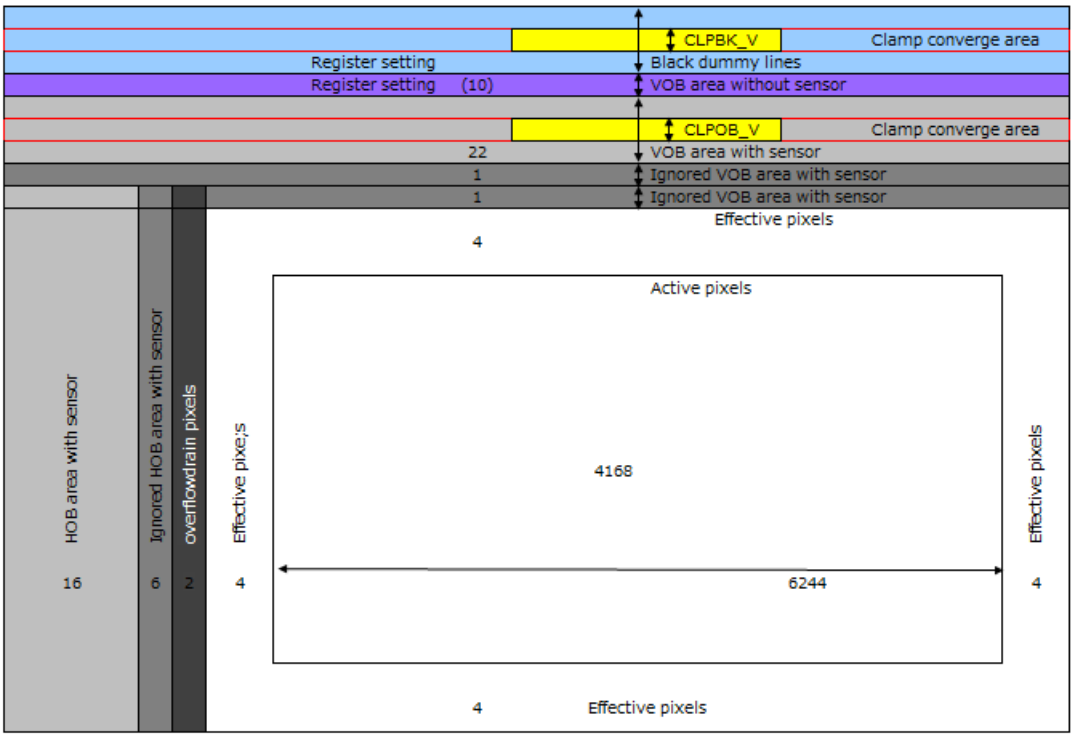


Fig. Clamp Area (for example: All-pixel readout mode)

Table. Restrictions of black dummy clamp area setting register in each mode

MODE register	Readout mode	Restrictions of clamp start line designation [CLPBK_VST]	Clamp area designation restriction [CLPBK_V]	The upper limit of CLPBK_VST and CLPBK_V
0h	All-pixel readout mode 16 bit to 11bit ADC	n (n=0, 1, ...)	4m (m=3, 4...)	2n + 4m ≤ BK_WIDTH-6
1h	All-pixel readout mode / 2-parallel ADC readout 16bit to 12bit ADC			
3h	All-pixel readout mode / digital overlap drive 16bit to 11bit ADC			

Black dummy clamp operation timing chart

■Black dummy clamp (Mode 0/1/3)

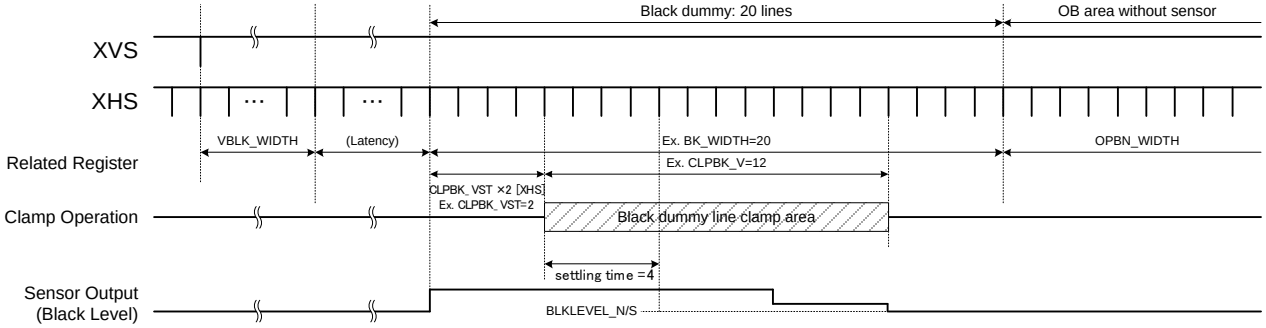


Fig. Black dummy clamp operation (for example: Mode0, Mode1, Mode3)

Table. Restrictions of OB clamp area setting register in each mode

MODE register	Readout mode	Restrictions of clamp start line designation [CLPOB_VST]	Clamp area designation restriction [CLPOB_V]	The upper limit of CLPOB_VSTand CLPOB_V
0h	All-pixel readout mode 16 bit to 11bit ADC	n (n=0, 1, ... , 3)	4m (m=3, 4)	2n + 4m ≤ 18
1h	All-pixel readout mode / 2-parallel ADC readout 16bit to 11bit ADC			
3h	All-pixel readout mode / digital overlap drive 16bit to 11bit ADC			

Clamp Operation Timing Chart

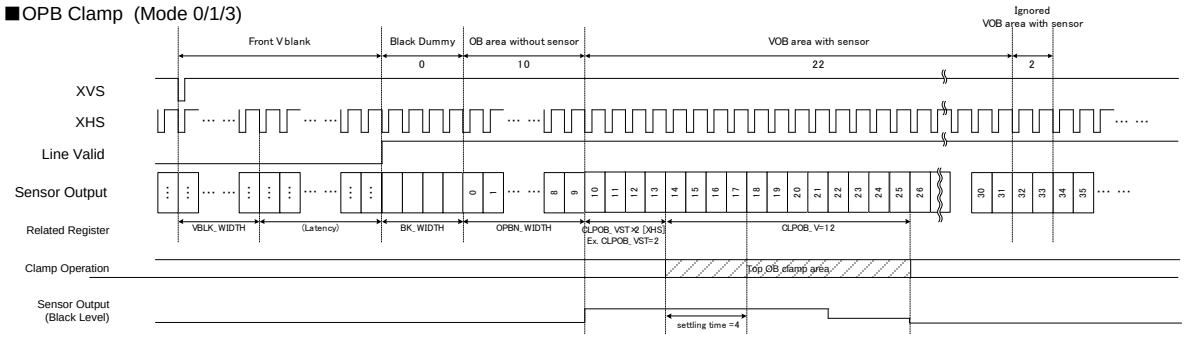


Fig. Top OB clamp operation (for example: Mode0, Mode1, Mode3)

Notes on Mode Transitions

Image Data

The 1st frame of moving picture after changing mode is invalid because of the invalid integration time.
The invalid image is output in the following cases.

- When the MODE register is changed.
- When the number of vertical output pixel lines or output timing is changed. (e.g. When V blank period, numbers of lines for black dummy and others are changed.)

Note) When the SHR is only changed, the ignored image is not required. However, the one frame immediately after the change is reflected is the image shot in the exposure time before the SHR change.

Transmission Timing of Immediate Reflection Registers with Mode Transitions

Address 067Eh and 00A1h registers are immediate reflection registers. So these registers should be transmitted in the V blank period after transmitting the other mode registers or during invalid frame period of next XVS period. After transmitting these immediate reflection registers and 150 us passed, input next XVS pulse or set the SLP_CTRL register for long time exposure.

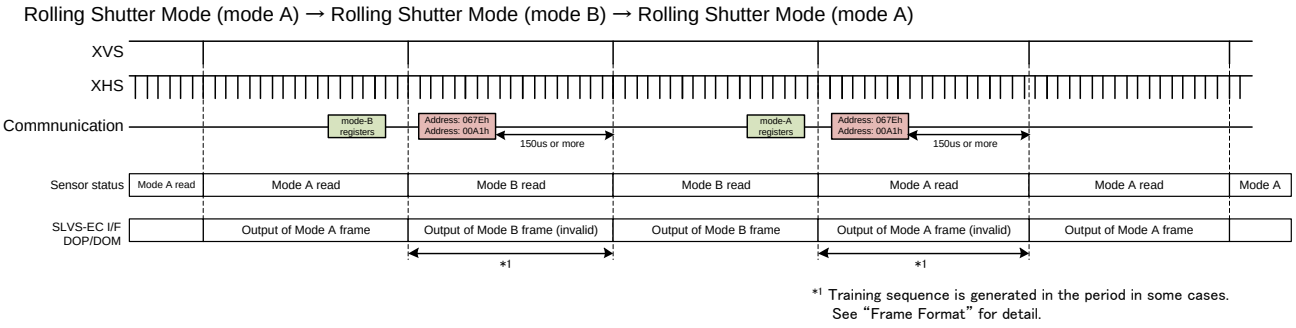


Fig. Mode Change Timing Chart (1)

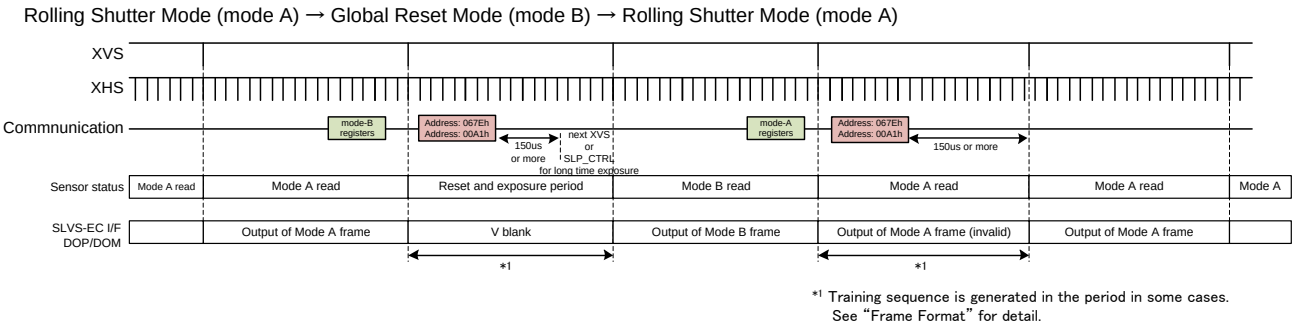


Fig. Mode Change Timing Chart (2)

Clamp Control

The clamp function in this sensor is for using the dynamic range of the internal circuit effectively. Clamp should be performed again for the set.

Mode Transition and Training Sequence

When mode transition in case of following situations, training sequence is generated after XVS input.

1. Output word bit length is changed.
2. Number of horizontal output pixels is changed. (Including horizontal freely cropping function)
3. Any SLVS-EC setting registers[*1] are changed.

[*1] CRC_EN, ECC_EN, INIT_LENGTH, SYNC_LENGTH, DESKEW_LENGTH, DESKEW_INTERVAL, STANDBY_LENGTH, SYNC_SYMBOL, DESKEW_SYMBOL, IDLE_CODE1 to 4, STANDBY_SYMBOL

After training sequence, valid frame is output from next frame.

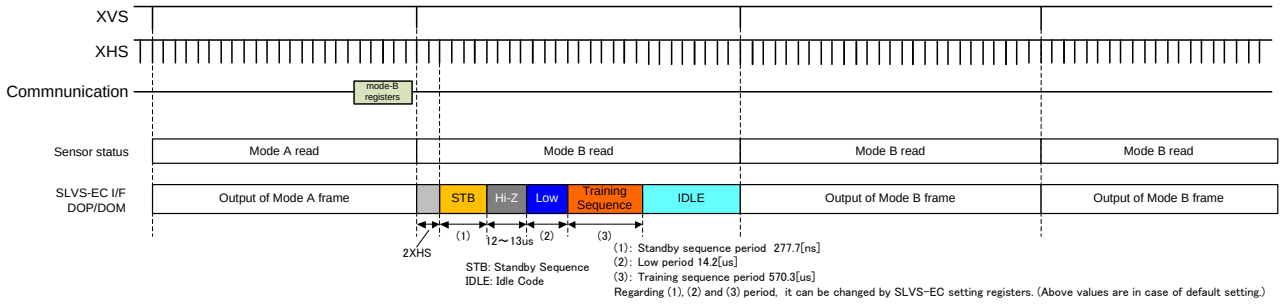


Fig. Training Sequence Generated Timing when Mode Transition

(1) Standby Sequence Period

Standby sequence period can be changed by STANDBY_LENGTH register.
Formula of standby sequence period is as below.

Standby sequence period = STANDBY_LENGTH × 4 × SI[*2]

[*2] SI: Symbol Interval (1/230.4MHz)

In case of STANDBY_LENGTH = 10h (default)
Standby sequence period = 16 × 4 × 1/230.4MHz = 277.77⋯[ns]

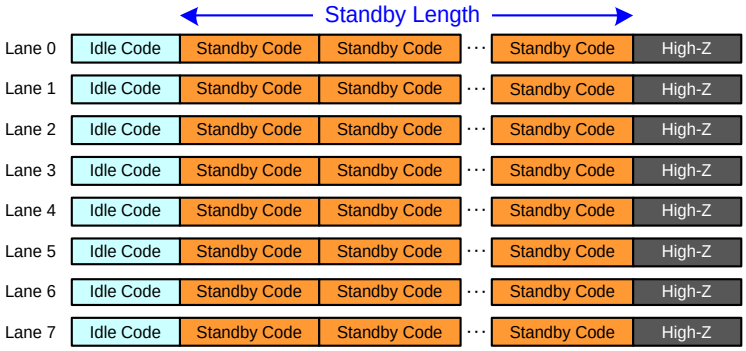


Fig. Standby Sequence

(2) Low Period

Low period can be changed by INIT_LENGTH register.
Formula of low period is as below.

Low period = 2^(INIT_LENGTH) [clk@72MHz]

In case of INIT_LENGTH = 0Ah (default)
Low period = (2^10)/72MHz = 14.22⋯[µs]

(3) Training Sequence Period

Training sequence period can be changed by SYNC_LENGTH, DESKEW_INTERVAL and DESKEW_LENGTH registers. Formula of training sequence period is as below.

Training sequence period = {(SYNC_LENGTH×4)+((DESKEW_INTERVAL+4) × DESKEW_LENGHT)} × SI

In case of SYNC_LENGTH = 007FFFh (default), DESKEW_INTERVAL = 10h (default), DESKEW_LENGTH = 10h (default)

Training sequence period = {(32767 × 4)+((16+4) × 16)}/230.4MHz = 570.2604⋯[μs]

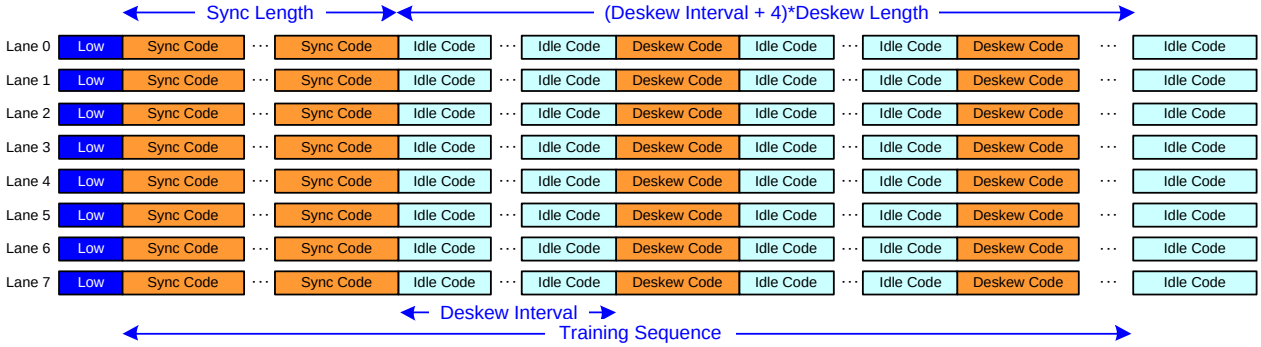


Fig. Training Sequence

Initial Setting

Refer to “IMX571BQR-C_Initial_Register_Setting” document which is separate sheet.

Fixed Pattern Output Test Mode

Fixed pattern output test mode becomes enabled by setting the register FIXDTON = 1h.
The register FIXDTSEL selects the output patterns. Each pattern is described below.
It is compatible only in 16 bits output mode (BK_WIDTH must be 0h).

Shading mode (FIXDTSEL = 0h)
To use this mode, other registers setting (MODE = 0h and BK_WIDTH = 0h) are also needed.
However, when AD 16 bits is not used, the lower bit is deleted.
The sensor outputs the value which increases by the number selected by FIXDTSFT each column and row.

FIXDTSFT register	Increment value
0h	1d
1h	2d
2h	4d
3h	8d

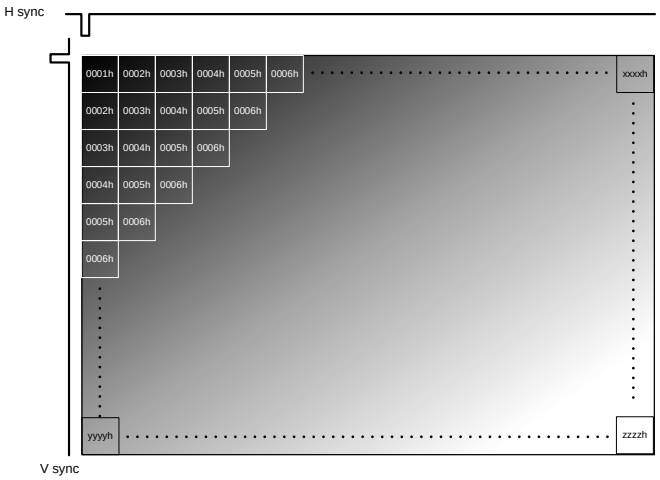


Fig. Shading mode output image

Color bars mode (FIXDTSEL = 1h)
To use this mode, other registers setting (MODE = 0h and BK_WIDTH = 0h) are also needed.
It corresponds only to AD 16 bits. Select sensor output direction of color bars by COLORBARSEL register setting.

COLORBARSEL register	Direction of color bars
0d	Vertical
1d	Horizontal

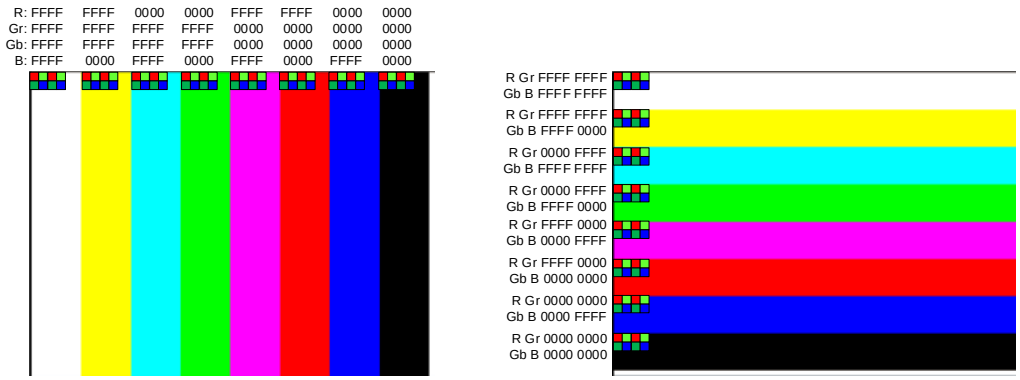


Fig. Color bars mode output image

Each color channel fixed pattern mode (FIXDTSEL = 2h)
To use this mode, other registers setting (MODE = 0h and BK_WIDTH = 0h) are also needed.
However, when AD 16 bits is not used, the lower bit is deleted.
Each color channel (R/Gr/Gb/B) of the sensor outputs the fixed value.
The sensor outputs the value which fixed value shift by the number selected by FIXDTSFT.

FIXDTSFT register	Fixed value shift setting
0h	No shift
1h	1bit (×2)
2h	2bits (×4)
3h	3bits (×8)

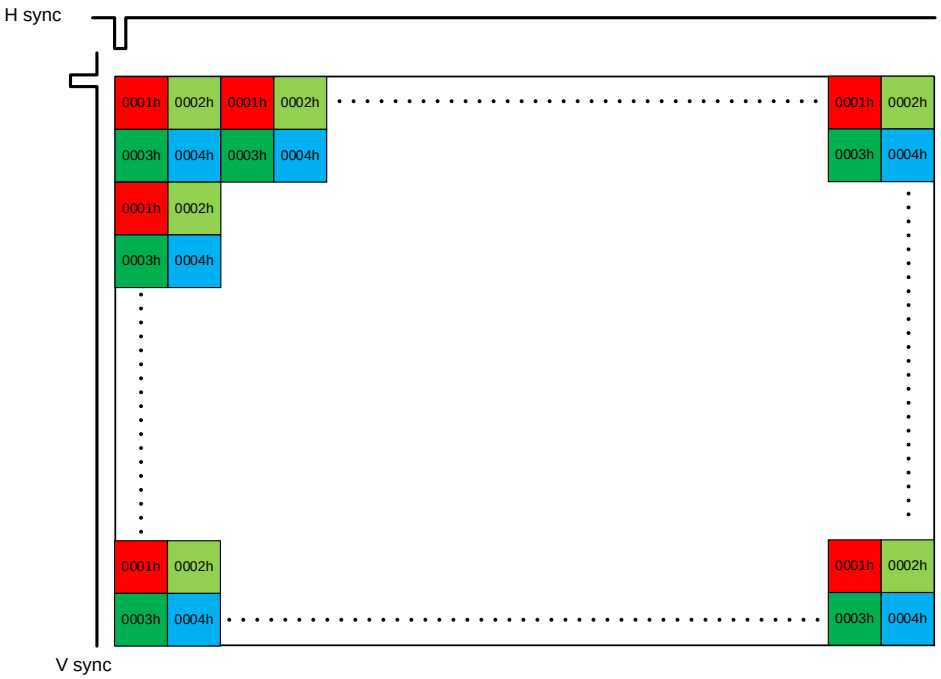
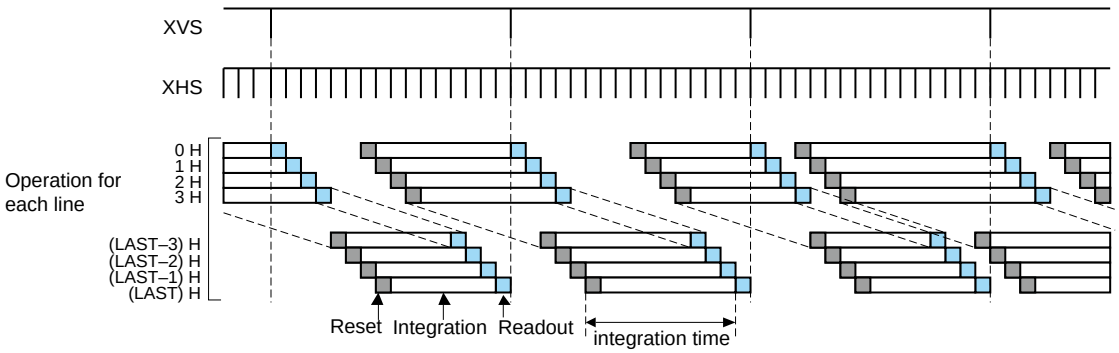


Fig. Each color channel fixed pattern mode output image

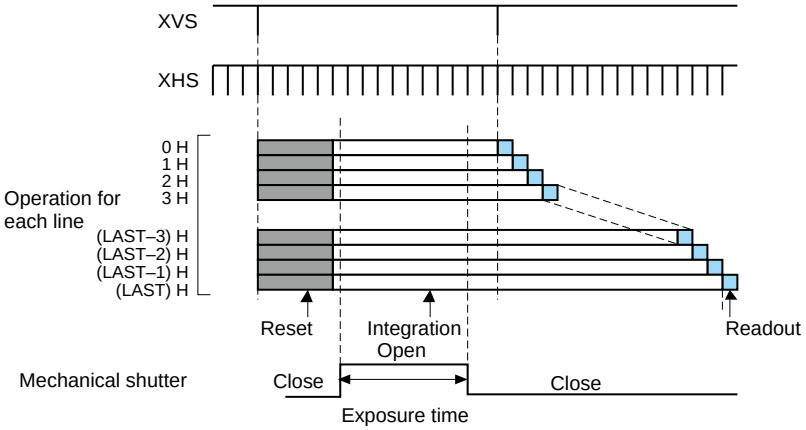
Integration Time Control

SMD (Shutter Mode)

The sensor shutter operation switching is required between still picture mode and moving picture mode. Set global reset shutter operation in still picture mode and rolling shutter operation in moving picture mode.
Rolling shutter operation performs reset for successive pixels every H in sync with XHS. Global reset shutter operation performs reset and starts integration for all pixels at once. In global reset shutter operating mode, the mechanical shutter must also be used for alignment of the exposure time for each pixel.



(a) Rolling shutter operation (SMD = 0h)



(b) Global reset shutter operation (SMD = 1h)

Fig. Rolling Shutter and Global Reset Shutter Operation

Internal Time Setting

The integration time for rolling shutter operation is calculated with the following formula.

When Mode1 and Mode5

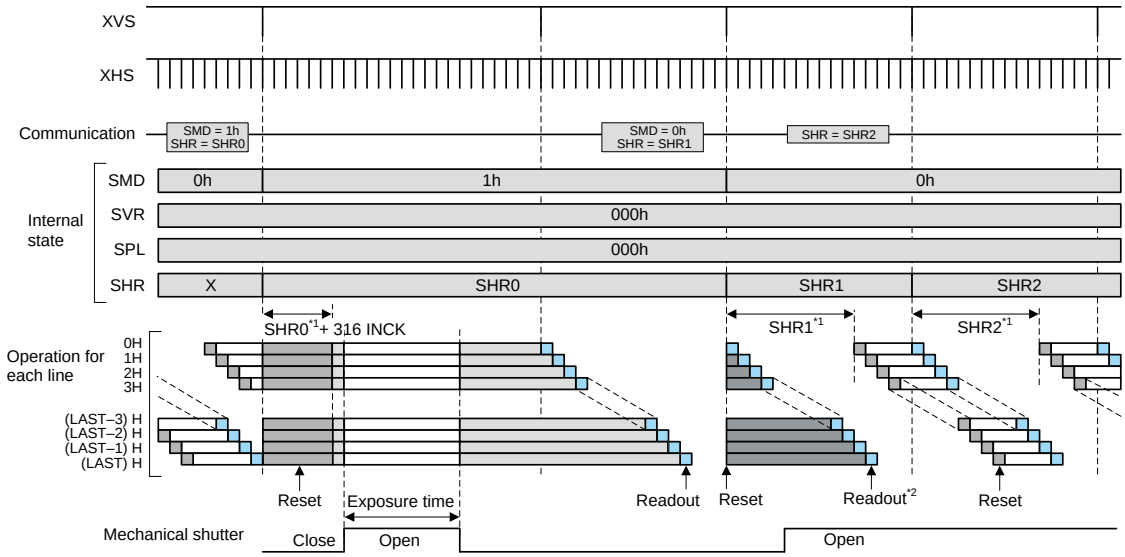
[{XHS number per 1 V period × (SVR value – SPL value + 1)} – SHR value] × INCK number per 1 XHS period/INCK frequency

When other than Mode1 and Mode5

[{XHS number per 1 V period × (SVR value – SPL value + 1)} – 2 × SHR value] × INCK number per 1 XHS period/INCK frequency

◆ SHR

Pixel reset operation starts after number of XHS pulses designated by SHR register are input from XVS pulse is input. When global reset shutter mode is set, pixel reset operation starts for all pixels at once. When rolling shutter mode is set, pixel reset operation starts for successive pixels from the first H.



*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same. Please see table of "SHR Register Setting Range and Number of XHS Pulses" for detail.
*2 All lines are reset for XVS immediately after SMD is changed from 1h to 0h. Therefore, readout image regarded as ignored image.

Fig. Integration Time Control by SHR

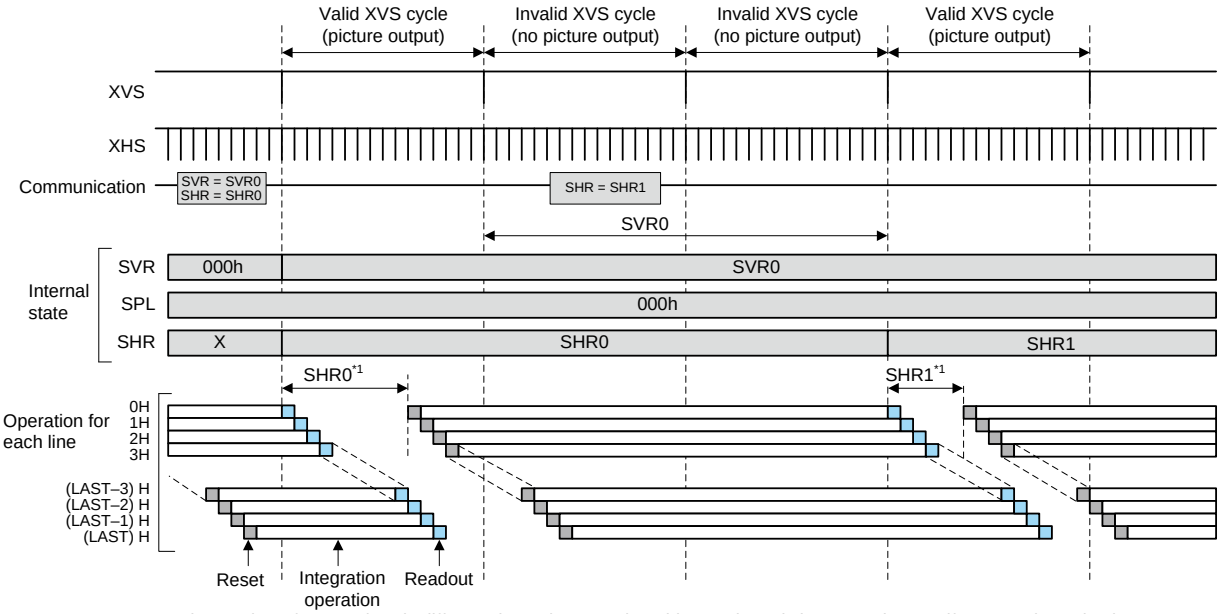
Table. SHR Register Setting Range and Number of XHS pulses

Mode No.	Shutter mode	SHR register setting range		Number of XHS pulses designated by SHR register [Number of XHS]
		Minimum	Maximum	
No.0, No.0A	Rolling	1	1V*/2 – 1	SHR setting value × 2
	Global reset	1	1V/2 – 1	SHR setting value × 2 + 4
No.1	Rolling	1	1V –1	SHR setting value
	Global reset	1	1V – 1	SHR setting value + 2
No.3, No.6, No.7, No.10, No.11, No.12, No.13, No.14, No.15, No.16, No.17, No.18, No.19, No.20, No.21	Rolling	1	1V/2 – 1	SHR setting value × 2
No.5	Rolling	1	1V – 1	SHR setting value

* 1V: Number of XHS per 1V period

◆ SVR

When SVR is set to other than “000h”, picture output is performed at the next XVS input, and then picture output is not performed for the number of XVS cycles set by SVR as shown in the figure below. This causes the frame rate to drop accordingly, but long time integration operation can be performed (slow shutter operation).

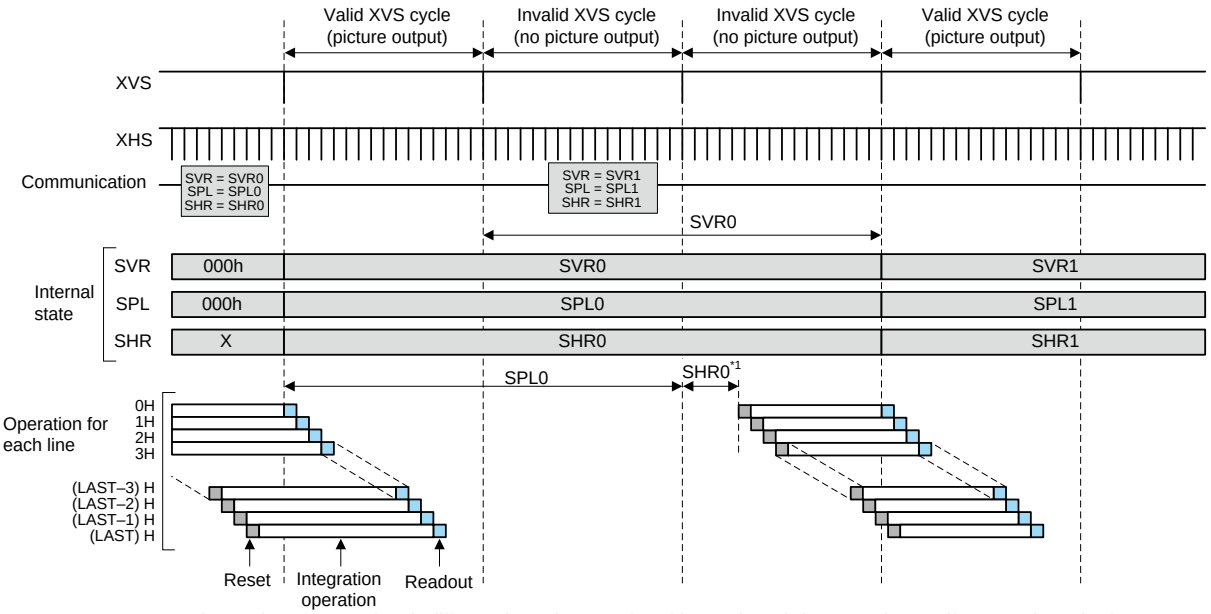


*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same. Please see table of “SHR Register Setting Range and Number of XHS Pulses” for detail.

Fig. Slow Shutter Operation by SVR (SVR0 = 002h)

◆ SPL

When SPL is set to other than “000h”, integration start is not performed for the number of XVS cycles set by SPL from the next XVS input as shown in the figure below. SPL is used together with SVR.



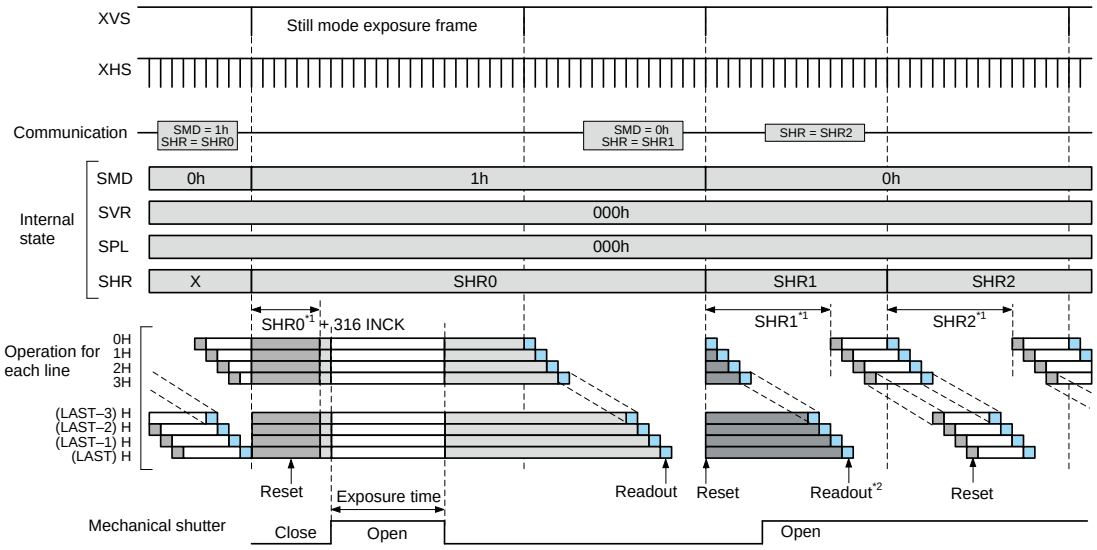
*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same. Please see table of “SHR Register Setting Range and Number of XHS Pulses” for detail.

Fig. Integration Time Control by SPL and SVR (SVR0 = 002h, SPL0 = 002h)

Global Reset Shutter Operation

Global reset shutter operation resets and starts storage for all pixels at once. The mechanical shutter must be used together with global reset shutter operation to align the exposure time for each pixel. The SHR register sets the reset start timing for all pixels at once.

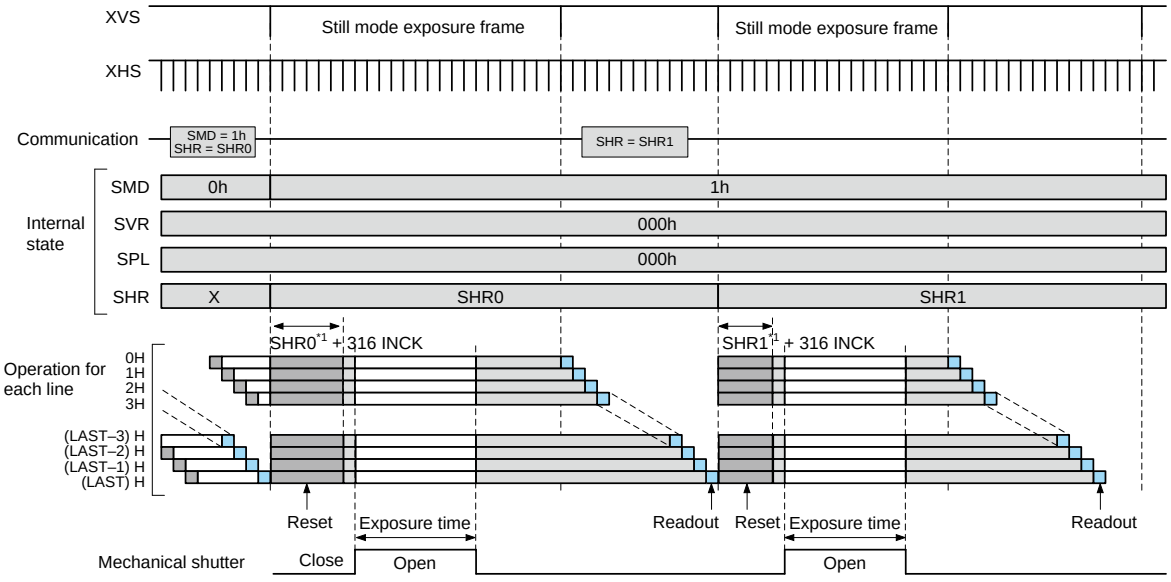
Example A. Live view → Still picture → Live view



*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same.
Please see table of "SHR Register Setting Range and Number of XHS Pulses" for detail.
*2 All lines are reset for XVS immediately after SMD is changed from 1h to 0h.
Therefore, readout image regarded as ignored image.

Fig. Global Reset Shutter Drive Example A

Example B. Live view → Continuous shooting



*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same.
Please see table of "SHR Register Setting Range and Number of XHS Pulses" for detail.

Fig. Global Reset Shutter Drive Example B

Long Time Exposure

In long time exposure mode, this sensor can be set to low power consumption (sleep setting). This setting may reduce the dark voltage in long time exposure mode. Sleep setting duration is set by register SLP_CTRL as below figure. This register SLP_CTRL is performed immediately just after transmitted.
At the semi time register SLP_CTRL, please do the control of power V_{DD}HPX.

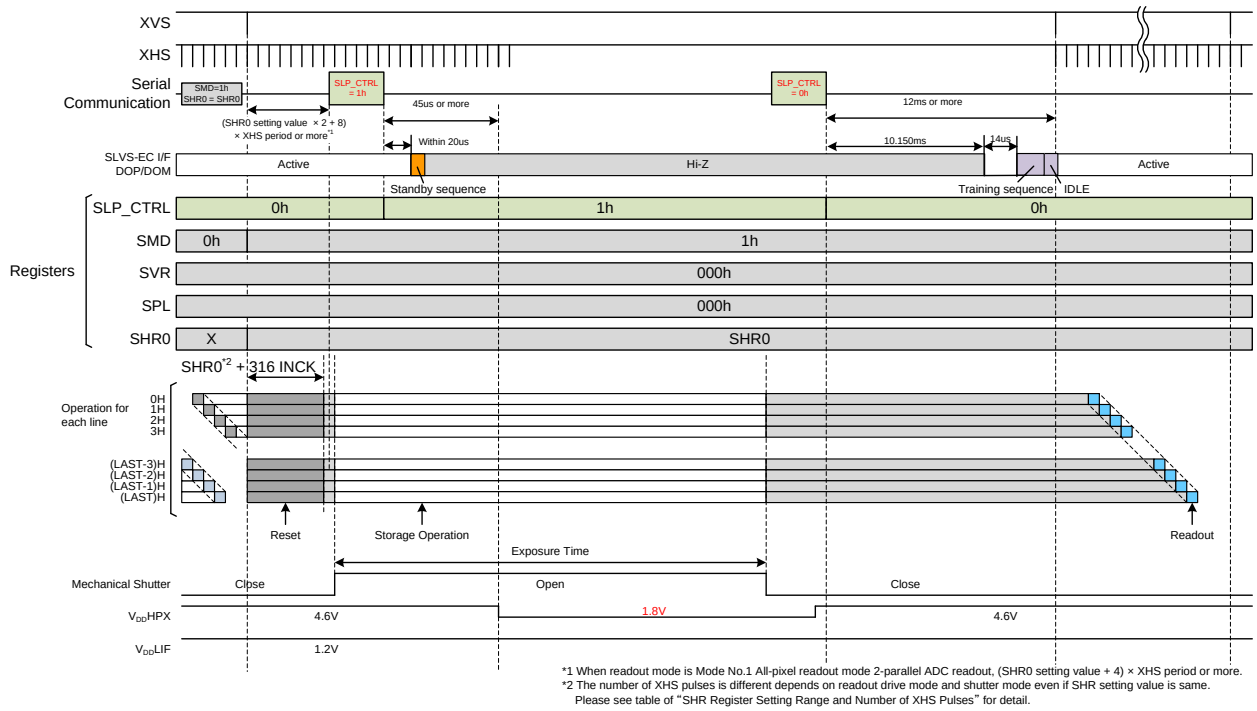


Fig. Example of Long Time Exposure Drive

Standby Mode

In standby mode, this sensor can be set to low power consumption more than sleep setting. Exposure operation is canceled in standby mode. Standby mode sequence is controlled by STANDBY and SLP_CTRL registers. Detail of standby mode sequence is shown as below.

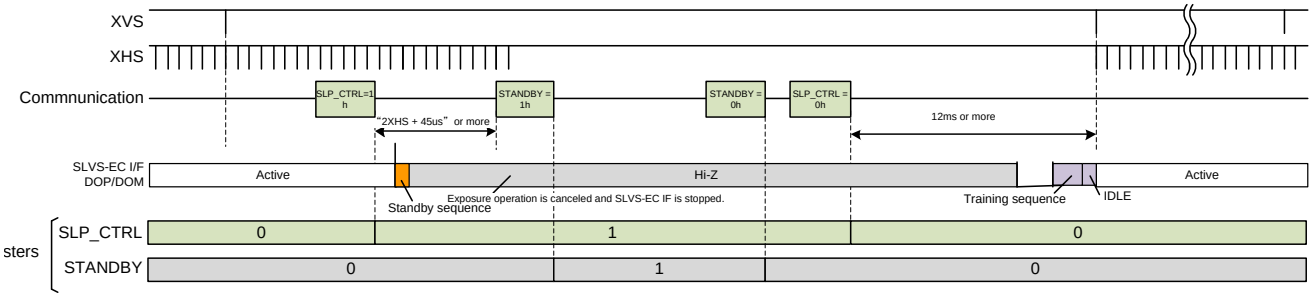


Fig. Standby Mode Sequence

Electronic First Curtain Shutter Function

In global reset shutter operation, Electronic first curtain shutter function which reset timing of each pixel line can be adjusted in accordance with the mechanical shutter speed can be used. There are two types of electronic first curtain shutter modes. One is Polygon electronic first curtain shutter mode which reset timing of each pixel line is controlled by the registers, and the other is Non-linear electronic first curtain shutter mode which reset timing of each pixel line is controlled by the external XPI pin.

Register Explanation

◆ MSMD

It is a register switched to the Electronic first curtain shutter control.

Address	Register MSMD	Description
0003h [1]	0h	All-pixel simultaneous reset mode
	1h	Electronic first curtain shutter mode

◆ OPMODE

The act mode is switched the front curtain electronic mode.

Address	Register OPMODE	Description
0003h [2]	0h	Polygon electronic first curtain shutter
	1h	Non-linear electronic first curtain shutter

◆ VSHT_DIR

The scanning direction of front curtain electronic shutter is switched.

Address	Register VSHT_DIR	Description
0003h [5]	0h	Normal (Area 1 to 48, Pixel address small to large)
	1h	Inverted (Area 48 to 1, Pixel address large to small)

Polygon Electronic First Curtain Shutter

In the use of Polygon electronic first curtain shutter function, the scanning speed of the electronic first curtain shutter of each vertical area defined by the following can be set. A vertical area is divided into 48 groups. The number from 1 to 48 is allotted from the physical address minimum to maximum regardless of the first curtain scanning direction.

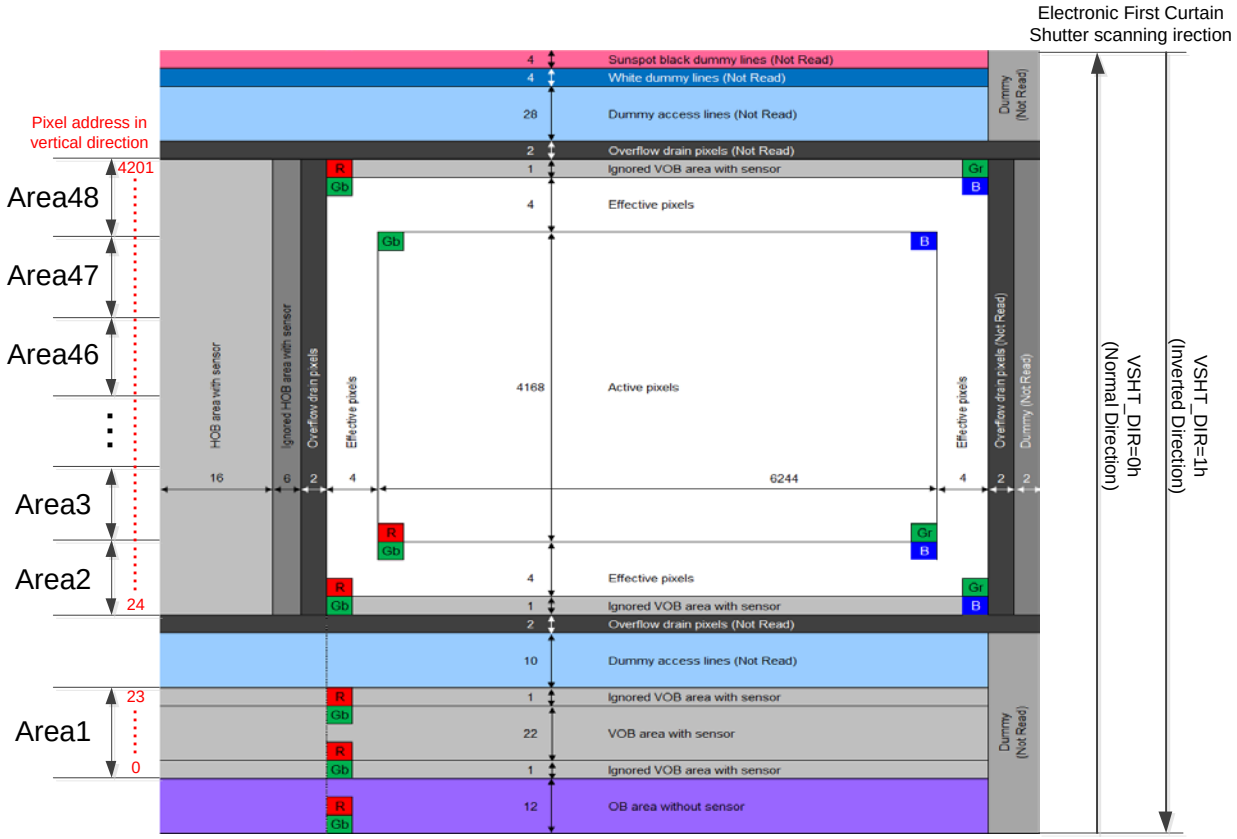


Fig. Polygon Electronic First Curtain Shutter Segmented Region

Register Explanation

◆ SINT

It is a register that combines with SHR and sets the reset start timing of the Polygon electronic first curtain shutter. Set it by a 64CLK (F_{CLK} = 36 MHz) unit. Setting 00h is prohibited.

◆ POLYGON_OP_SPEED1 to 48 [7:0]

It is a register to which curtain speed of the electronic first curtain shutter is changed each area.
Exposure time of each pixel can be made uniform by matching first curtain speed with second curtain mechanical shutter by register POLYGON_OP_SPEED1 to 48 the electron.
Set 7 or more to POLYGON_OP_SPEED1 to 48.
The relation to curtain speed of the electronic first curtain shutter is as follows with register POLYGON_OP_SPEED1 to 48.

Curtain speed [µm/µs] = 135.4 / (POLYGON_OP_SPEEDn[7:0] + 1)

*n = 1 to 48

◆ POLYGON_OP_DCMS1 to 48[1:0]

This register sets the parallel row reset function of polygon electronic first curtain shutter area.
When a setting value is 0h, curtain speed is the above mentioned.
If setting value is 1h, curtain speed becomes 2 times because of 2 row parallel reset.
If setting value is 3h, curtain speed becomes 4 times because of 4 row parallel reset.

◆ POLYGON_OP_VADR1 to 47[13:0]

The end address value of each area group when a vertical area is divided into 48 groups is specified.

(1) Because area 1 is allocated in the VOB area by fixation (POLYGON_OP_VADR1 = 0017h).

(2) Set the pixel address in order of area 2 to 47. The set values are 14'd24 or more. And these register should be set that the setting value of smaller number don't become bigger than the setting value of large number. Both even numbers and odd numbers can be set.

(3) Set a different pixel address to all registers.

(4) This register cannot be the set the number of over pixel address. (It does not operate correctly.)

(5) When the parallel row reset function is used, the setting value has to set the value of [(multiple of 4)-1].

The scanning speed of each area is set with POLYGON_OP_SPEED1 to 48 and POLYGON_OP_DCMS1 to 48.

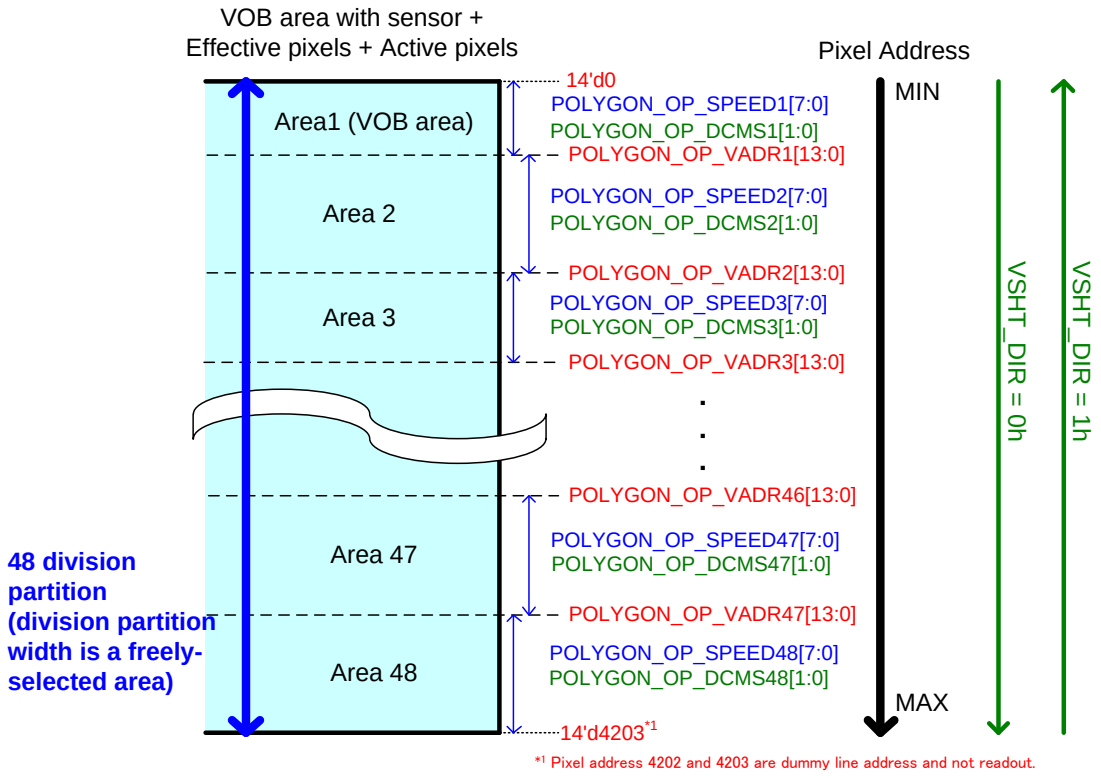
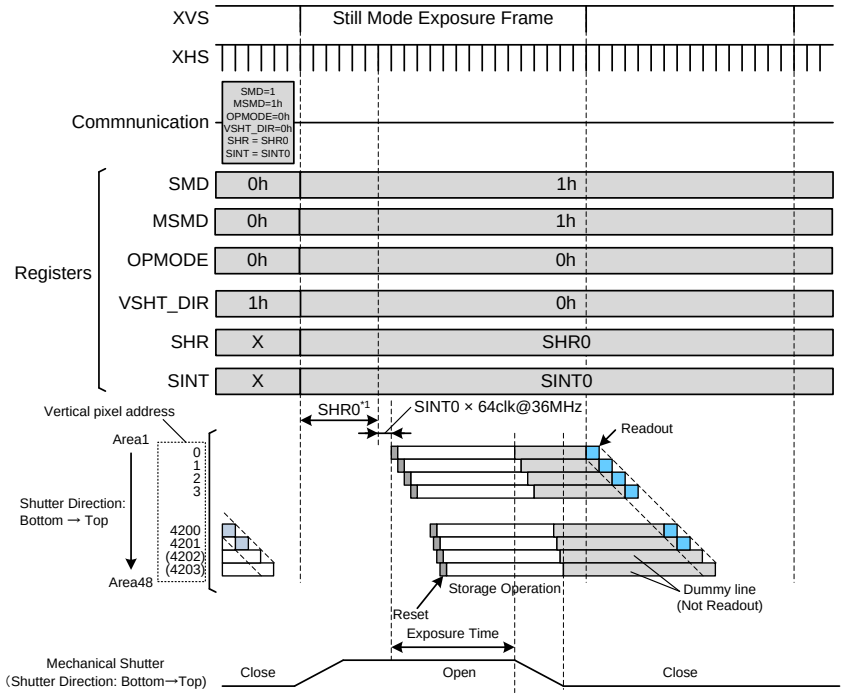


Fig. Area Groups Setting and Each Curtain Speed Setting

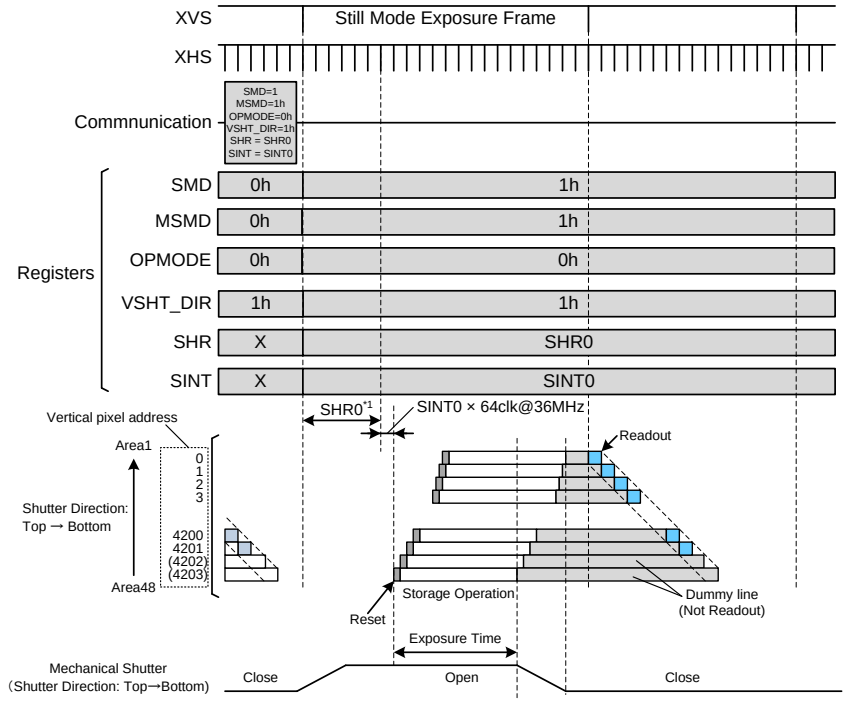
Operation Sequence

Operation sequences of Polygon electronic first curtain shutter are shown as below.



*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same. Please see table of "SHR Register Setting Range and Number of XHS Pulses" for detail.

Fig. Pixel Reset Start Timing Chart when VSHT_DIR = 0h



*1 The number of XHS pulses is different depends on readout drive mode and shutter mode even if SHR setting value is same. Please see table of "SHR Register Setting Range and Number of XHS Pulses" for detail.

Fig. Pixel Reset Start Timing Chart when VSHT_DIR = 1h

Restriction of XVS Interval at Polygon Electronic First Curtain Shutter Mode

Keep the following restriction about XVS interval at Polygon electronic first curtain shutter mode.
When it is not able to keep the restriction, the subsequent reading operation might not be correctly done.

Still image exposure frame:

XVS interval ≧ (XHS period × SHR × 2) + (64 × SINT + T)/36 MHz + 1 ms

T = (POLYGON_OP_SPEED1 + 1) × (POLYGON_OP_VADR1 + 1)
+ (POLYGON_OP_SPEED (n) + 1) × ((POLYGON_OP_VADR (n)) - (POLYGON_OP_VADR (n - 1))) *1
+ (POLYGON_OP_SPEED48 + 1) × (14'd4203 - (POLYGON_OP_VADR47))

*1 (n = 2～47) is all added.

SINT = 00h and SHR = 0000h are set prohibitions.

Non-linear Electronic First Curtain Shutter

In the use of Non-linear electronic first curtain shutter function, the scanning speed of the electronic first curtain shutter of each vertical line can be set by XPI pulse timing.

Operation Sequence

Operation sequences of Non-linear electronic first curtain shutter is shown as below.
First XPI pulse can be input after 700 INCK or more from XVS, and each vertical pixel line is reset at one line per one XPI pulse. When VSHT_DIR = 0h (normal), the order of reset vertical pixel address is from 0 to 4203. When VSHT_DIR = 1h (inverted), the order of reset vertical pixel address is from 4203 to 0. After all pixel address is reset, additional XPI pules is input (End pulse). In addition, vertical pixel address 4202 and 4203 are dummy line and reset operation is done but not readout. After 20 INCK or more from last XPI pulse (End pulse), readout XVS can be input. Total 4205 XPI pulse are needed in order to reset all vertical pixel lines.

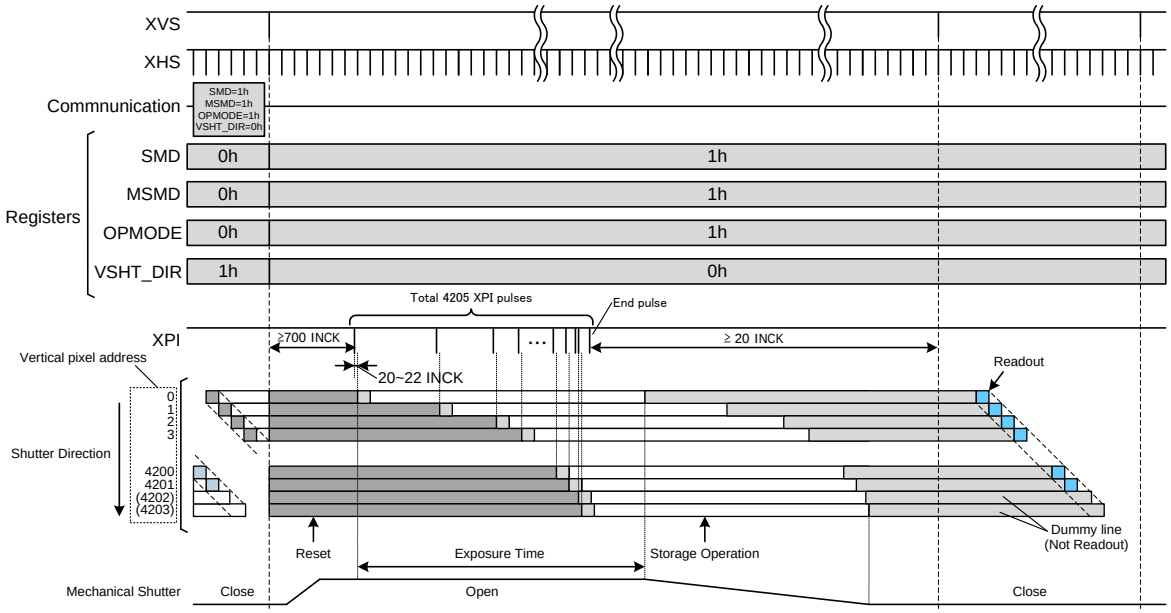


Fig. Pixel Reset Start Timing Chart when VSHT_DIR=0h

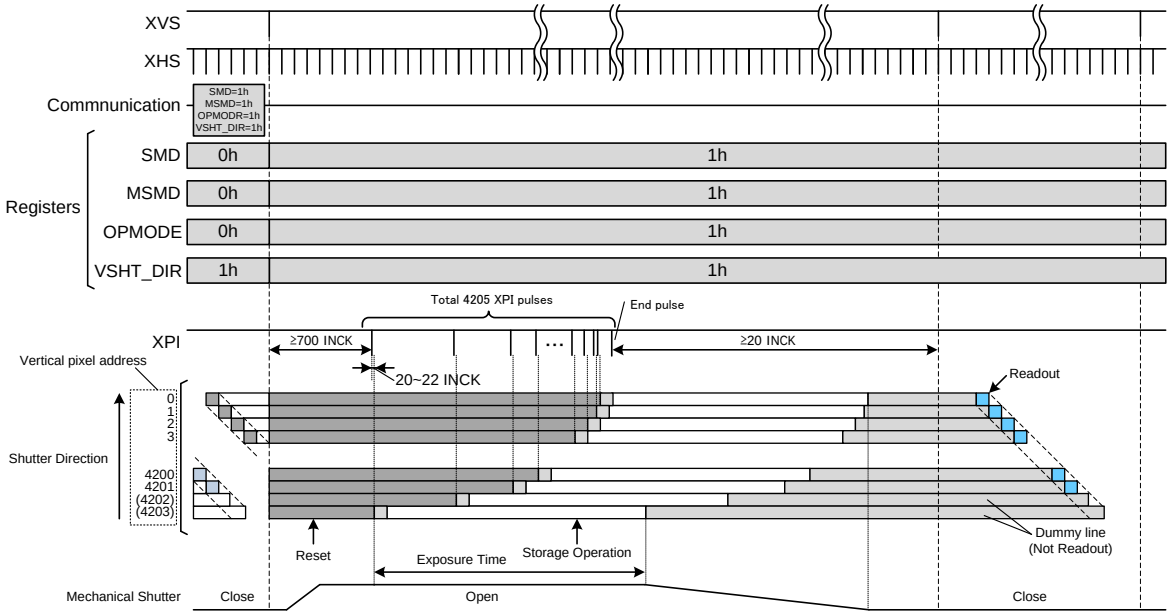


Fig. Pixel Reset Start Timing Chart when VSHT_DIR=1h

Slow Shutter Break

As previously mentioned, setting a value other than “0h” in SVR starts the slow shutter operation that performs storage operation across multiple XVS cycles. However, slow shutter operation can also be stopped to shift to the next imaging operation.

◆ Slow Shutter Break by the SSBRK Register
When operation after slow shutter break is imaging operation in rolling shutter mode, slow shutter break can be set by the SSBRK register.
When SSBRK is set to “1h” during slow shutter operation, the image stored up to the next XVS input is output at the next XVS input. The next slow shutter cannot be stopped by keeping SSBRK at “1h”. To break the slow shutter again, SSBRK must be returned to “0h” and then set to “1h” again.

◆ Slow Shutter Break by SMD
SSBRK cannot be used when operation after slow shutter break is imaging operation in global reset shutter mode.
When SMD is set to “1h”, the slow shutter is broken at the next XVS input. The image is not output at this time, and instead global reset shutter operation is immediately performed and the image corresponding to the global shutter is output at the next XVS input.

Gain Setting

Two channels of PGC (programmable gain control) function for each DAC are mounted in this sensor, and each channel can be controlled separately.
APGC_N: North side column ADC analog gain setting
APGC_S: South side column ADC analog gain setting

Note) Set all the same values to APGC_N and APGC_S.

The analog PGC image diagram is shown below.

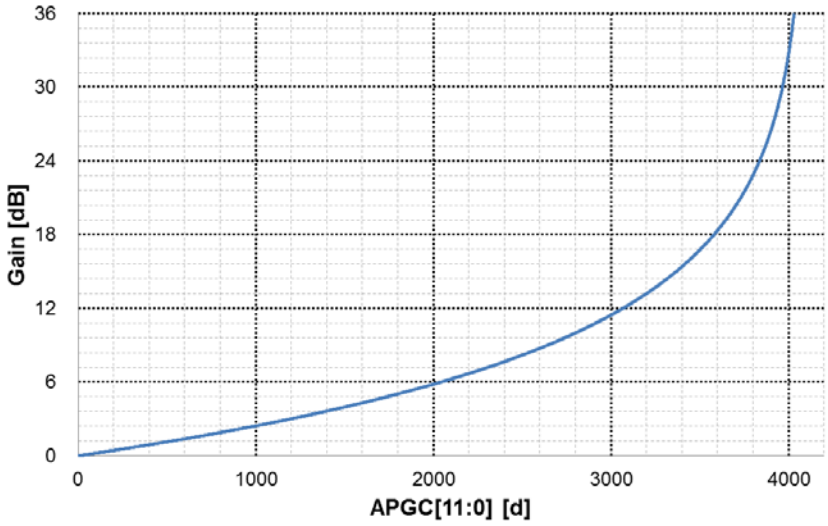


Fig. Analog Gain

Analog gain of 0 to 36 dB corresponding to each color can be set according to the setting value of the analog gain setting registers. The relational formula for the register setting value and the gain is shown below.

$$\mathrm{Gain[dB]} = -20\log\left(1 - \frac{\mathrm{APGC[11:0]}}{4095}\right)$$

Formula. Analog Gain Conversion Formula

Setting range of APGC registers for each readout mode is following table.

Table. APGC setting range for each readout mode

A/D conversion bits	Setting range of registers APGC_N/APGC_S	Setting range of analog gain [dB]
16 bits/14 bits/12 bits	000h to FBEh (0d to 4030d)	0 to 36
11 bits	000h to F7Dh (0d to 3965d)	0 to 30

In addition, change the setting value of following additional setting registers according to register value of APGC registers in all readout modes.

Table. Additional register setting of each APGC setting

Additional setting registers	Analog gain registers setting APGC_N/APGC_S		
	000h to 7FAh (0dB to 6dB)	7FBh to DFBh (6dB to 18dB)	DFCh to FBEh (18dB to 36dB)
APGC_ADD	0h	0h	1h
CLPAPGC	0h	2h	4h

And also please refer to the additional “IMX571 Gain Setting Specification” for detail.

Digital Overlap Readout Mode

Over View

Digital Overlap (DOL)

This mode operates to exposure in the order of the long exposure frame (LEF), the short exposure frame (SEF) during the time equivalent to 2 frames of normal operation, and then each exposure frame data are output in overlapped. The timing of the SEF output is delayed by setting value which is set for readout of the SEF.
The t_{LEF} as the exposure time of LEF must be set to be longer than t_{SEF} as the exposure time of SEF. For details of t_{LEF} and t_{SEF}, refer to the section “Exposure Timing Register Setting”.

About the Output

When using DOL mode in this sensor, 2 different exposure time data of the line are output each XHS period alternately. The first XHS period is the R/Gr line data of the long exposure frame, the second XHS period is the R/Gr line data of short exposure frame, the third XHS period is the Gb/B line data of long exposure frame and the forth XHS period is the Gb/B line data of short exposure period. In this case, XHS period must be twice as long as normal mode which don’t use DOL.

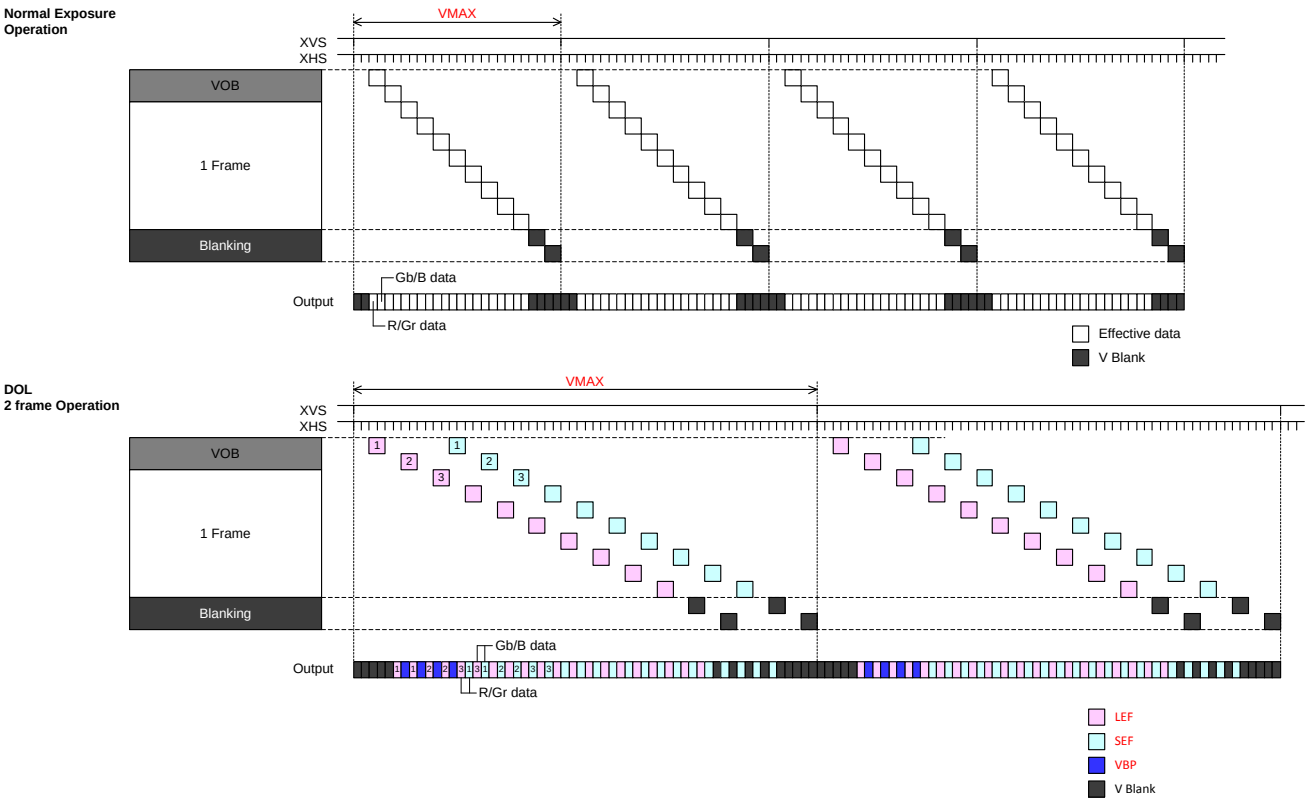


Fig. Image Drawing of DOL

Definition of Each Item

Symbol	Unit	Remarks
VMAX	H	Number of horizontal line per 1 Frame
LEF	—	Long exposure frame
SEF	—	Short exposure frame
VBP	H	Vertical blanking period in front of short exposure data
BRL	H	Number of horizontal line of SEF

The figure below shows the data output image.
During 1XHS period, LEF and SEF data are output alternately. SEF data is output with a delay which length is the exposure time of SEF. All of necessary data line of LEF and SEF (BRL) must be output in 1V period when using DOL.
For details of the restriction of XHS and XVS setting value, refer to the section below.

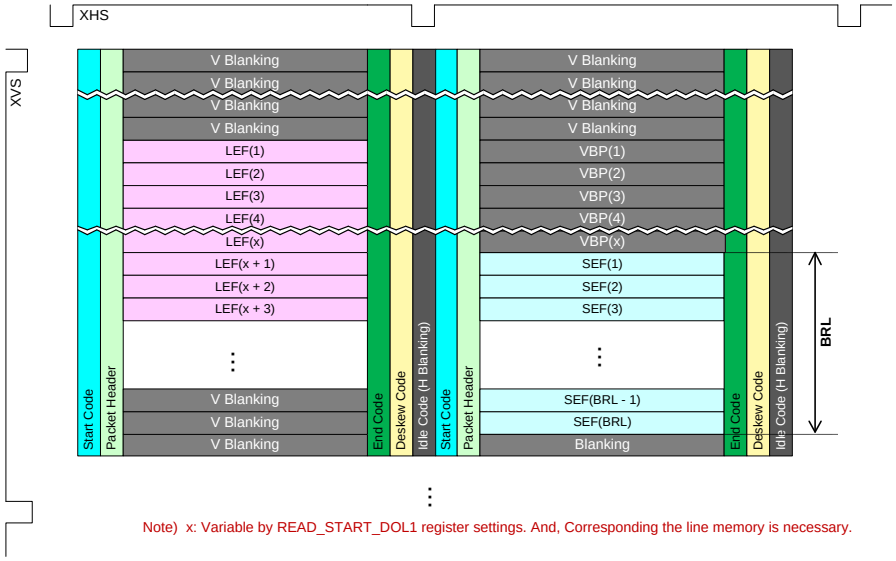


Fig. Output Image When Using DOL

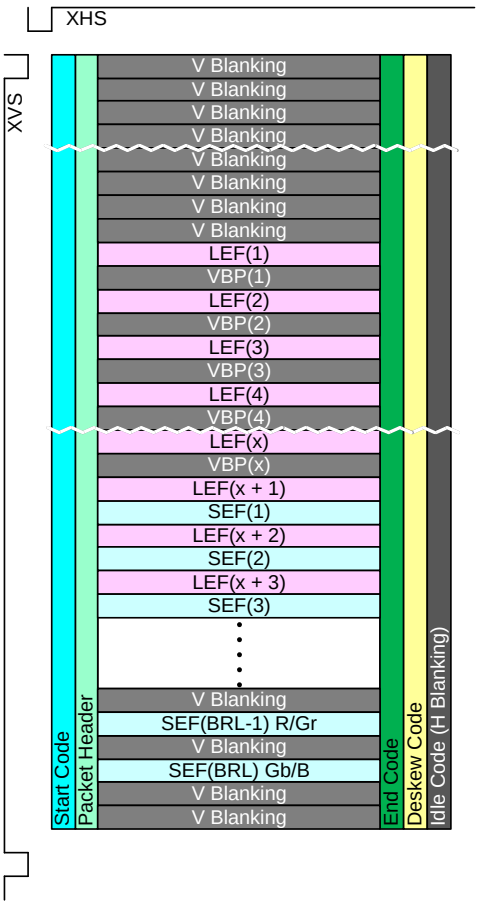


Fig. Output Image When Using DOL (arranged by XHS)

Exposure Time Setting

The electronic shutter timing of short exposure is set by the register SHR_DOL1, the electronic shutter timing of long exposure is set by the register SHR_DOL2 and the readout timing of short exposure is set by the register READ_START_DOL1.
Usually, the frame memory according to line amount of delay is necessary in backend for the combining processing because the delay of READ_START_DOL1 lines occurs between the output of long exposure data and output of short exposure data of the same line.

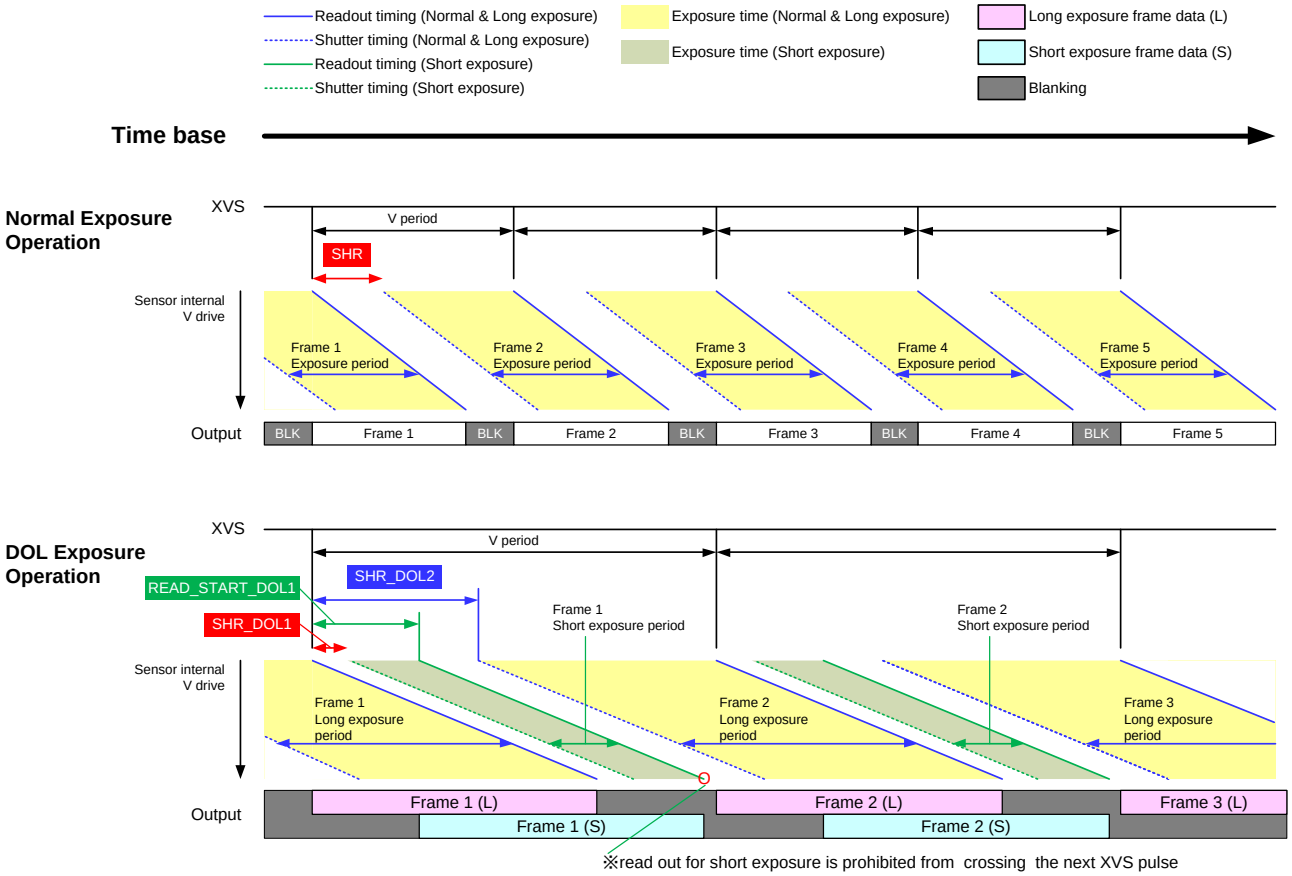


Fig. Diagram of DOL Operation

List of Register Assignment

Operation	Long exposure frame (LEF)		Short exposure frame (SEF)	
	Shutter	Readout	Shutter	Readout
Normal exposure	SHR	—*		
DOL	SHR_DOL2	—*	SHR_DOL1	READ_START_DOL1

* The readout timing of long exposure frame is fixed.

Register Setting

Registers for DOL

Set the registers shown below in addition to the registers for normal mode when using DOL.

Description of Register Setting for DOL

Address	Bit assignment	Default value	Register name	When using DOL	Readout mode other than DOL
0004h	[1]	0h	LESS_SHUT_DOL1	0h: Normal/ 1h: Shutter less	(invalid)
0004h	[2]	0h	LESS_SHUT_DOL2	0h: Normal/ 1h: Shutter less	
001Bh	[7:0]	0009h	READ_START_DOL1	According to integration time	
001Ch	[6:0]				
001Dh	[7:0]	0005h	SHR_DOL1	According to integration time	
001Eh	[6:0]				
001Fh	[7:0]	000Eh	SHR_DOL2	According to integration time	
0020h	[6:0]				
0034h	[7:0]	000h	APGC_LT_N	According to analog gain setting	
0035h	[3:0]				
0036h	[7:0]	000h	APGC_LT_S	According to analog gain setting	
0037h	[3:0]				
0038h	[7:0]	000h	APGC_ST_N	According to analog gain setting	
0039h	[3:0]				
003Ah	[7:0]	000h	APGC_ST_S	According to analog gain setting	
003Bh	[3:0]				

Gain Register Setting

Two channels of PGC (programmable gain control) function for each DAC are mounted in this sensor, and each channel can be controlled separately.

APGC_LT_N: North side column ADC analog gain setting at long exposure frame when digital overlap drive
APGC_LT_S: South side column ADC analog gain setting at long exposure frame when digital overlap drive
APGC_ST_N: North side column ADC analog gain setting at short exposure frame when digital overlap drive
APGC_ST_S: South side column ADC analog gain setting at short exposure frame when digital overlap drive

Note) Set all the same values to APGC_LT_N, APGC_LT_S, APGC_ST_N and APGC_ST_S.

The analog PGC image diagram is shown below.

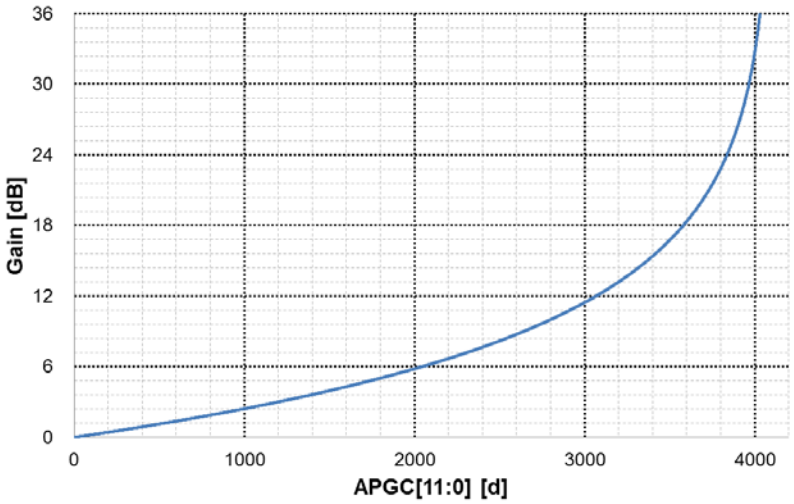


Fig. Analog Gain

Analog gain of 0 to 36 dB corresponding to each color can be set according to the setting value of the analog gain setting registers. The relational formula for the register setting value and the gain is shown below.

$$\mathrm{Gain[dB]} = -20\log\left(1 - \frac{\mathrm{APGC[11:0]}}{4095}\right)$$

Formula. Analog Gain Conversion Formula

Setting range of APGC registers for each readout mode is following table.

Table. APGC setting range for each readout mode

A/D conversion bits	Setting range of registers APGC_LT_N/APGC_LT_S/ APGC_ST_N/APGC_ST_S	Setting range of analog gain [dB]
16 bits/14 bits/12 bits	000h to FBEh (0d to 4030d)	0 to 36
11 bits	000h to F7Dh (0d to 3965d)	0 to 30

In addition, change the setting value of following additional setting registers according to register value of APGC registers in all digital overlap drive modes.

Table. Additional register setting of each APGC setting

Additional setting registers	Analog gain setting APGC_LT_N/APGC_LT_S/APGC_ST_N/APGC_ST_S		
	000h to 7FAh (0dB to 6dB)	7FBh to DFBh (6dB to 18dB)	DFCh to FBEh (18dB to 36dB)
APGC_ADD	0h	0h	Ch
CLPAPGC	0h	2h	4h

And also please refer to the additional “IMX571 Gain Setting Specification” for detail.

Exposure Timing Register Setting

These timings are set by register: (1) the electronic shutter timing of short exposure (SEF), (2) the readout timing of short exposure (SEF), (3) the electronic shutter timing of long exposure (LEF). The readout timing of long exposure (LEF) is fixed. The each exposure time and exposure ratio (exposure time ratio of LEF and SEF: expanding part of dynamic range) are decided by these timing setting.

Setting Values When DOL

Item	Register	Setting range
Electronic shutter timing of short exposure (SEF)	SHR_DOL1	It is prohibited to set even number.
Readout timing of short exposure (SEF)	READ_START_DOL1	It is prohibited to set even number. It is prohibited that readout period of SEF is crossing next XVS pulse.
Electronic shutter timing of long exposure (LEF)	SHR_DOL2	It is prohibited to set odd number.

Setting Values of Each Mode When DOL

Mode No.	Readout mode	Register	Setting range	
			Minimum value	Maximum value
3	All-pixel readout mode digital overlap drive	SHR_DOL1	1	READ_START_DOL1 – 2
		READ_START_DOL1	SHR_DOL1 + 2	The smaller of 4173[*1] and (SHR_DOL2 – 1)
		SHR_DOL2	READ_START_DOL1 + 1	1V/2 - 2
10	Vertical 1/3 subsampling, horizontal 3 weighted binning readout mode digital overlap drive	SHR_DOL1	1	READ_START_DOL1 – 2
		READ_START_DOL1	SHR_DOL1 + 2	The smaller of 1389[*1] and (SHR_DOL2 – 1)
		SHR_DOL2	READ_START_DOL1 + 1	1V/2 – 2
11	Vertical 3/3-line binning, horizontal 3 weighted binning readout mode digital overlap drive	SHR_DOL1	1	READ_START_DOL1 – 2
		READ_START_DOL1	SHR_DOL1 + 2	The smaller of 1385[*2] and (SHR_DOL2 – 1)
		SHR_DOL2	READ_START_DOL1 + 1	1V/2 – 2

Note) 1V: Number of XHS per 1 V period
[*1]: When using window cropping function (WND = 1h), WIN_WIDTH – 3
[*2]: When using window cropping function (WND = 1h), WIN_WIDTH – 5

Calculation Formulas for Exposure Time

Item	Symbol	Formula
Exposure time of LEF	t_{LEF}	{(Number of XHS per 1V period – SHR_DOL2 value × 2) × XHS period [CLK@72MHz]}/(72 × 10^6)
Exposure time of SEF	t_{SEF}	{(READ_START_DOL1 value – SHR_DOL1 value) × XHS period [CLK@72MHz] × 2}/(72 × 10^6)

Number of Front Blanking Line of Short Exposure Frame

The timing of the short exposure frame is set by the readout start timing of short exposure frame (READ_START_DOL1). When the image synthesis is performed in the backend processing, the line memory is necessary for holding the long exposure data (LEF) until the short exposure data is output. The number of line for delay is shown below.

Item	Symbol	Unit	Formula
Number of line from head of LEF to SEF	VBP	H	READ_START_DOL1 × 2 - 1

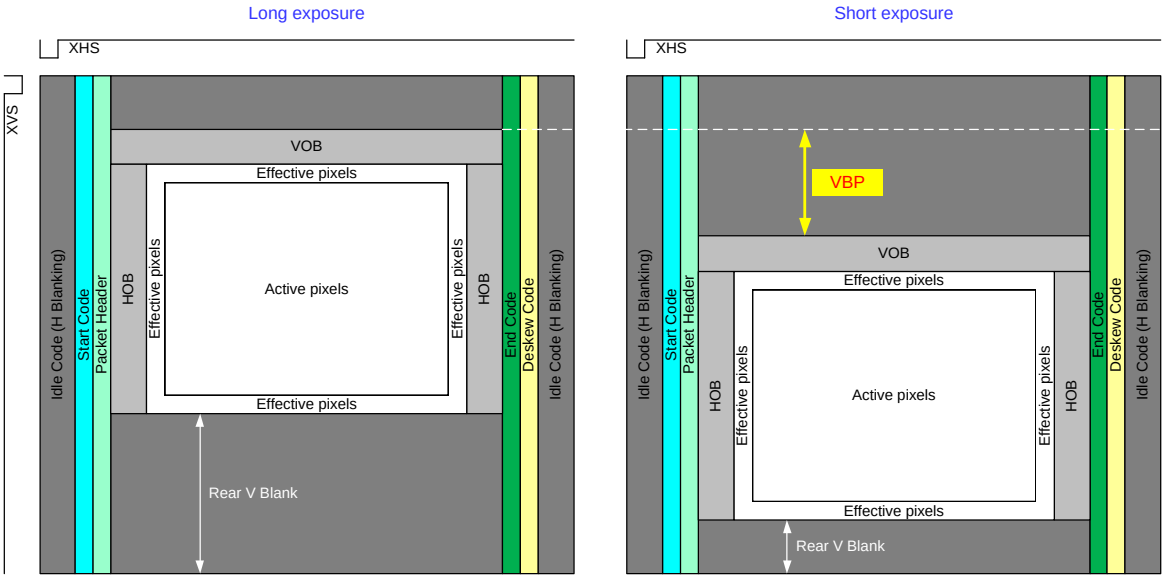


Fig. Number of Front Blanking Line in Front of Short Exposure Frame

Mode Transition

When Changing Mode to DOL

When changing from other readout mode to DOL and from DOL to other readout mode, set the registers according to following figure. In both changing the data of the first frame is invalid.

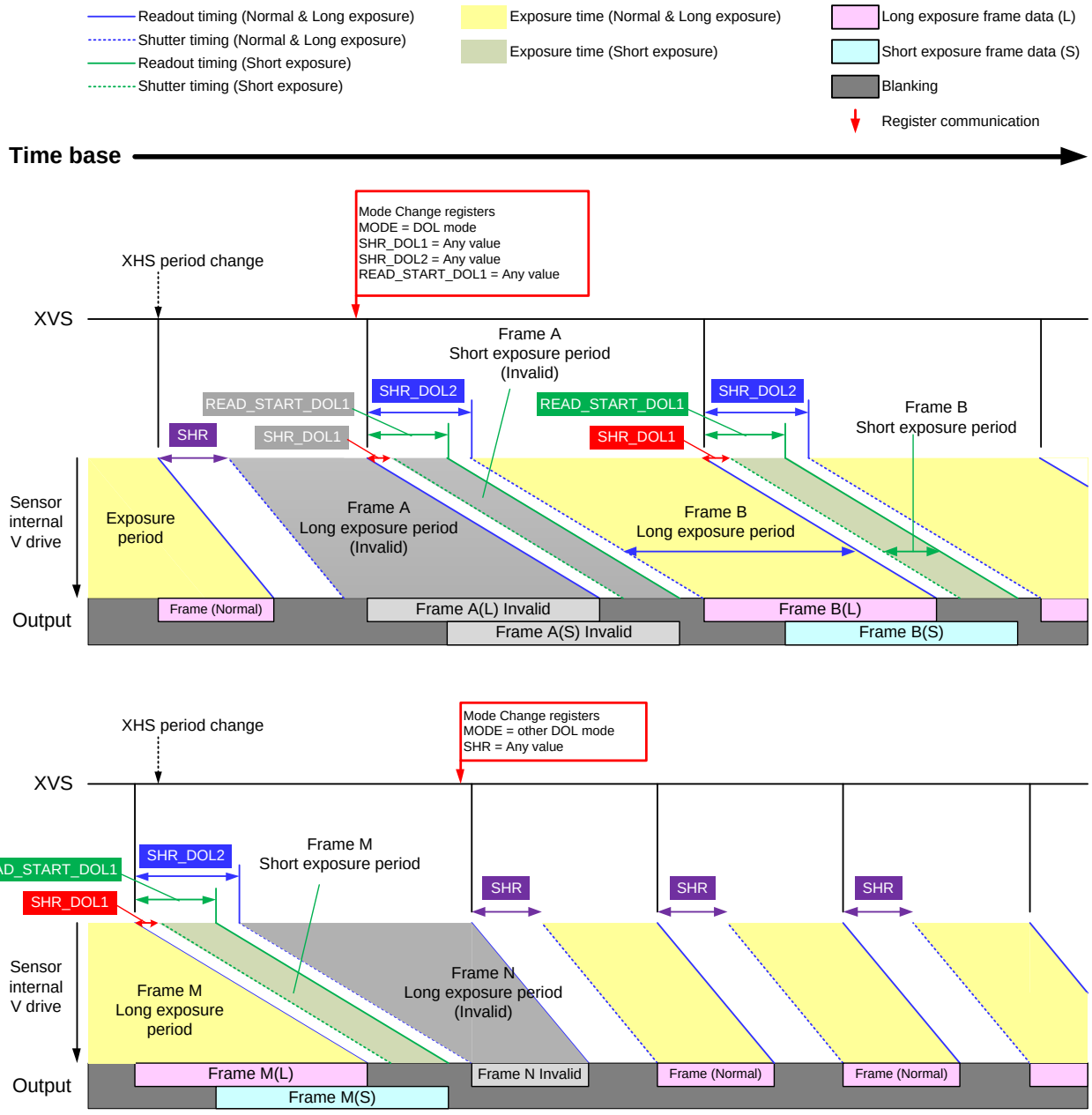


Fig. DOL Mode Transition

Reflection Timing When the Exposure Time Is Changed

Hereinafter, Frame A, B, C and D are continuous frames. In DOL operation, the registers are reflected as shown below when the exposure time is changed.
For example, if the register SHR_DOL1, SHR_DOL2 and READ_START_DOL1 are changed in communication period of frame C, these registers are reflected to output of frame D.
To avoid the invalid frame, the register settings should satisfy the formulas described on the table below, in addition to the usual limitation that each setting before and after changing should satisfy aforementioned limitation between SHR_DOL1, READ_START_DOL1 and SHR_DOL2 respectively.

List of Symbols

Item	Register name	Symbol
The register setting value before transition	SHR_DOL1	a1
	SHR_DOL2	a2
	READ_START_DOL1	a3
	APGC_LT_N/S APGC_ST_N/S	a
The register setting value after transition	SHR_DOL1	b1
	SHR_DOL2	b2
	READ_START_DOL1	b3
	APGC_LT_N/S APGC_ST_N/S	b

Additional Limitation to Avoid Invalid Frame When the Exposure Time Is Changed

Formulas
a3 + 1 ≤ b2

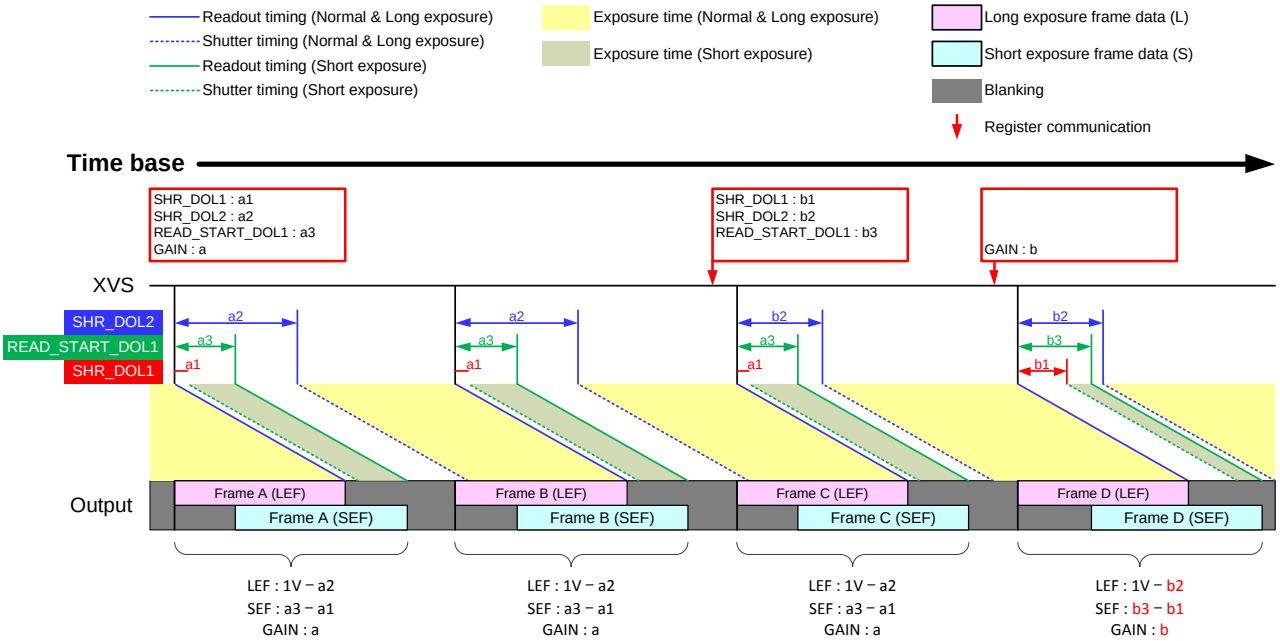


Fig. Example of Changing Exposure Time without Invalid Frameset

If the additional limitation cannot be satisfied, the communicated frameset and the next frameset will be invalid frameset.

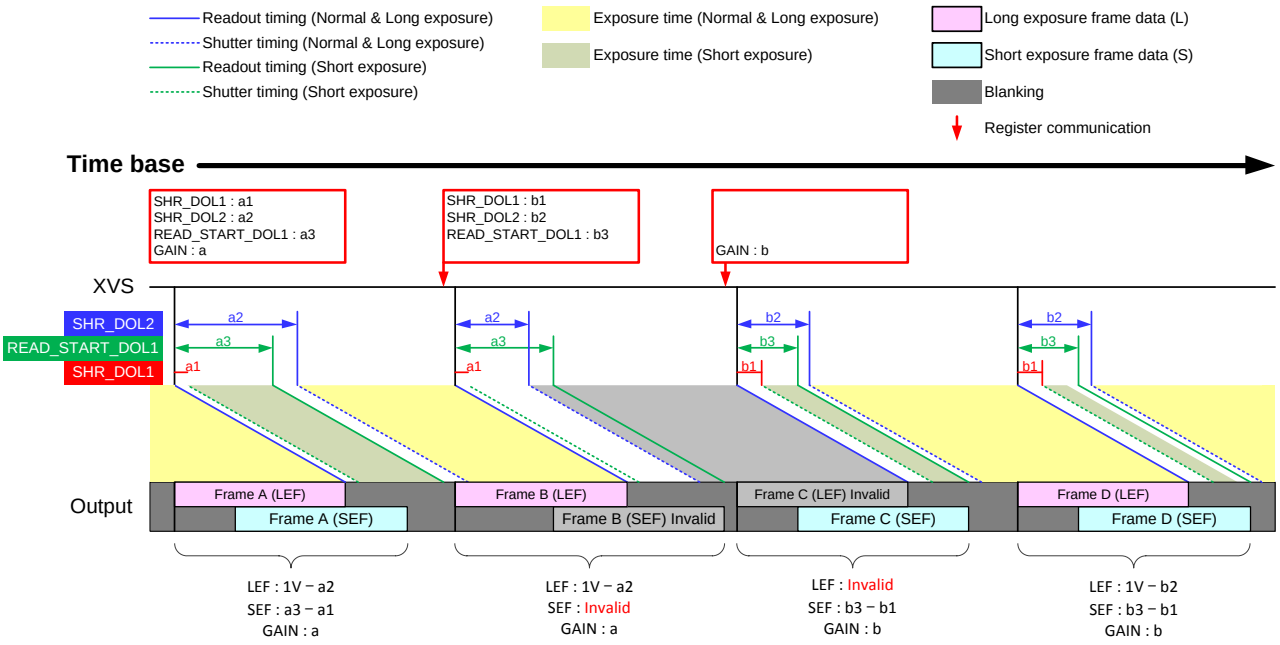


Fig. Example of Changing Exposure Time with Invalid Frameset

Black Level

Sensor internal clamp of this sensor is rough one for only keeping range for AD conversion.
LEF and SEF can have different black level under high gain because of the different integration times.
To solve this it is recommended to use external clamp in the camera ISP, and use VOB in LEF to clamp effective pixels in LEF, and VOB in SEF to clamp SEF effective pixels in SEF.

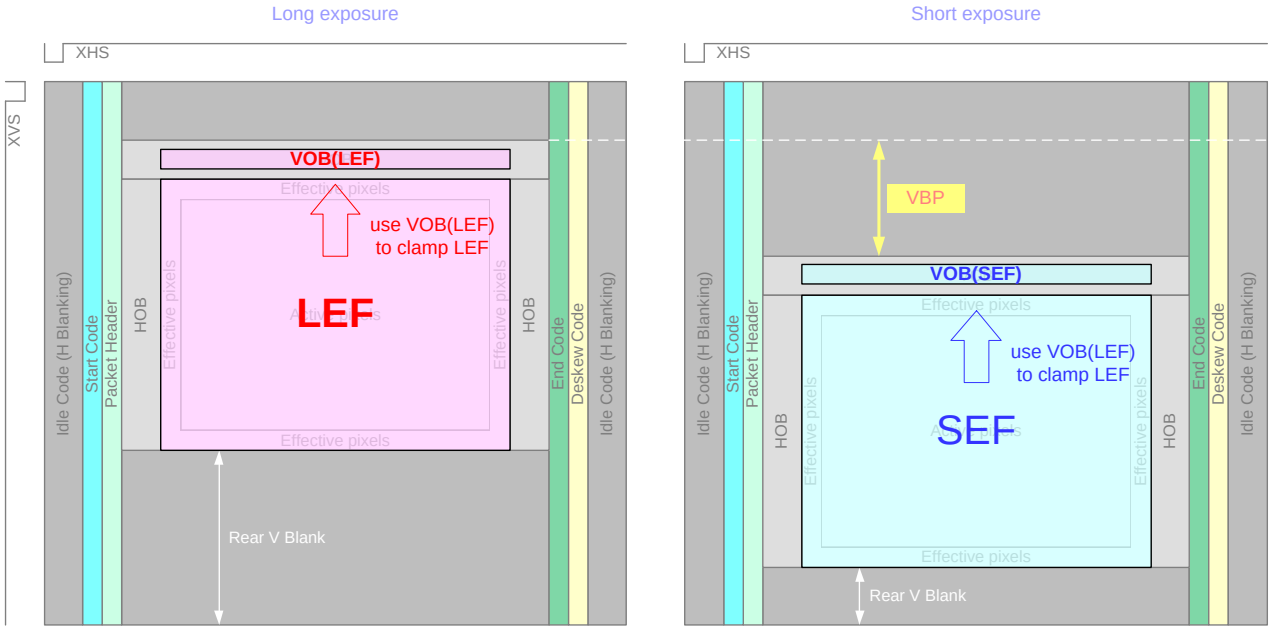


Fig. External Clamp and VOB

Global 4 Field Readout Function

Over View

Global 4 field readout function is that all-pixel readout frame is divided into 4 of vertical 1/4 subsampling frames and readout in order when readout frame of global reset shutter operation. All-pixel still image can be made by combining 4 of vertical 1/4 subsampling frames. This function can be expected to reduce the blackout period between capturing still image and displaying capture image result.

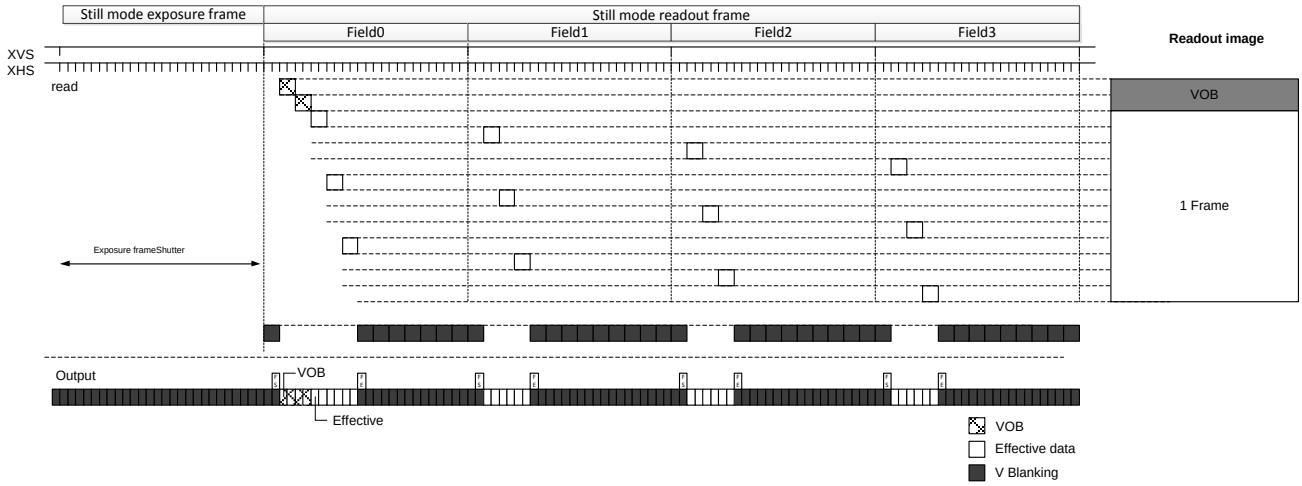


Fig. Image Drawing of Global 4 Field Readout

Setting Register and Modes which can be used the function

Global 4 field readout drive can be enabled by GLB4FLD register

◆ GLB4FLD

Address	Register GLB4FLD	Description
0005h [0]	0h	Normal operation
	1h	Global 4 field readout drive

Global 4 field readout drive can be enabled in following modes and shutter mode.
In addition, this function cannot be used when using window readout function.

Mode No.	Readout mode	Shutter Mode	Note
0	All-pixel readout mode	Global reset shutter (SMD = 1h)	Global 4 field readout drive can be used in combination with following shutter mode. - All-pixel simultaneous reset mode (MSMD = 0h) - Polygon electronic first curtain shutter mode (MSMD = 1h, OPMODE = 0h) - Non-linear electronic first curtain shutter mode (MSMD = 1h, OPMODE = 1h)
1	All-pixel readout mode 2-parallel ADC readout		

Exposure Operation and Readout

In Global 4 field readout operation, exposure is operated in the first frame (exposure frame), and readout is operated after 4 frames (readout frame). When the first readout frame (Field0), not only effective pixels but also other than effective pixels (VOB without sensor, VOB with sensor) are output. After second readout frame (Field1, 2, 3), only effective pixels are readout.
Clamp is operated in the first readout frame (Field0), and reflected all readout frames.
In case of interrupting Global 4 field readout function during half way of exposure frame or readout frames, slow shutter break function can be used. See “Slow Shutter Break” for detail.

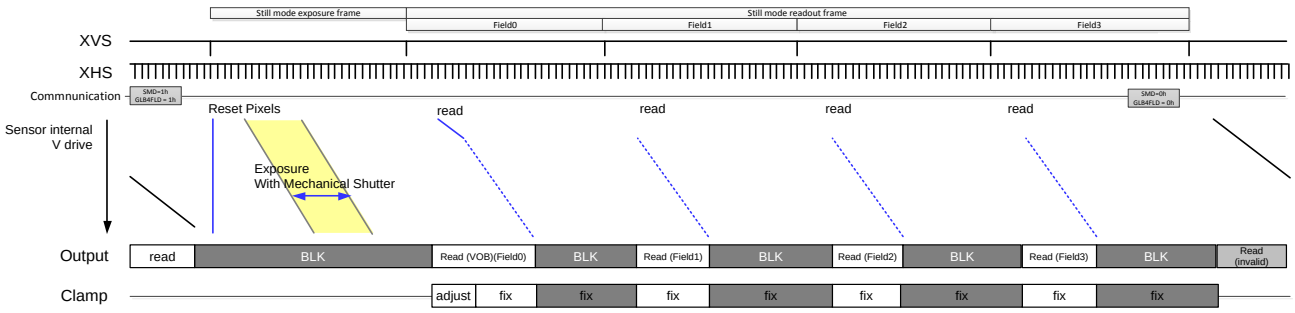


Fig. Diagram for Global 4 Field Readout Operation

Readout Pixel Address at Each Field

Readout vertical pixel address at each field is shown as below.
VOB lines are readout only Field0. In effective lines, R, Gr line and the next Gb, B line are regarded as one pair, and output at 4 pair intervals each field.

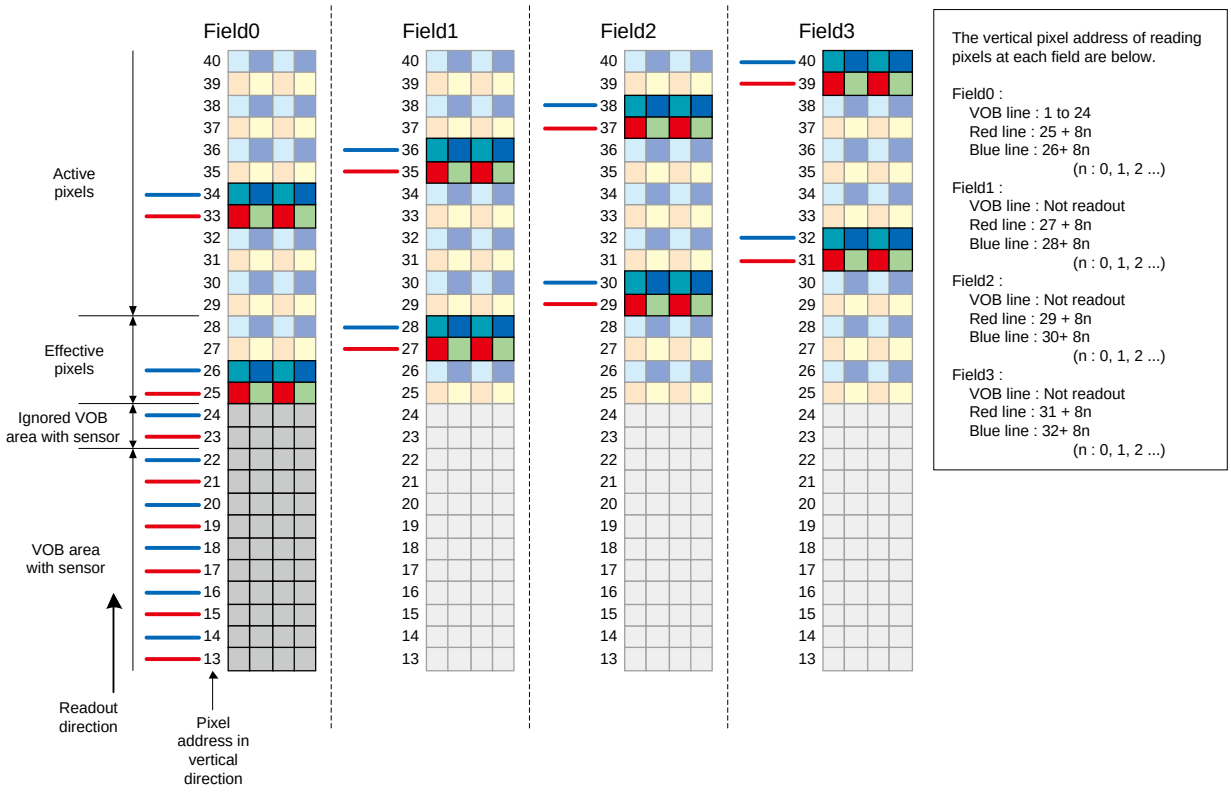


Fig. Readout Pixel Address at Each Field

Vertical Conditions of Each Field

Vertical conditions and 1XVS period of each field are shown following table.
In addition, horizontal condition of Global 4 field readout is same as normal readout operation.

Table. Vertical Conditions for Global 4 Field Readout Operation

Mode No.	Readout mode	Field	Number of OB without sensor lines *1	Number of VOB with sensor lines *3	Number of effective vertical pixels	1XVS period of each field [number of XHS] *4*5
0	All-pixel readout mode	Field0	10	24	1044	1092
		Field1/2/3	—*2	—*2	1044	1060
1	All-pixel readout mode 2-parallel ADC readout	Field0	10	24	1044	1092
		Field1/2/3	—*2	—*2	1044	1060

*1 Number of OB without sensor line can be set by OPBN_WIDTH register.
*2 OB without sensor lines and VOB with sensor lines are not output in Field1/2/3, output in only Field0.
*3 Ignored VOB with sensor lines are included.
*4 Number of XHS pulse per 1XVS period must be even number in every mode.
*5 XVS period of each field shown above table is in the case that VBLK_WIDTH = 6h, BK_WIDTH = 0h and OPBN_WIDTH = Ah.

High Speed AD Mode

Over View

This sensor can be output 5596 × 3148 pixels at 30 frame/s with 14 bits output word length or 60 frame/s with 12 bits output word length by changing high speed AD mode which AD speed is higher than normal operation.

Readout Drive Mode

The table below describes the readout drive modes that can be used to operate this sensor.
See the following section for the detailed output format of each mode.

Description of Readout Drive Mode

Table. Description of Readout Drive Modes

Mode No.		Readout mode	ADC	Word length	Mode description
0A	-b	All-pixel readout 16:9 cropping high speed AD mode	14 bits	14 bits	All pixels are read out. (16:9 cropping) This mode can be used together with the global reset shutter function according to the SMD register setting.
	-c		12 bits	12 bits	

Imaging Conditions in Each Readout Drive Mode

Table. Conditions for Readout Mode

Mode No.		Readout mode	Number of active horizontal pixels	Number of active vertical pixels	Number of OB without sensor lines *1	1XHS period [number of INCK] *2 *3	1V period [number of XHS] *3	Max frame rate [frame/s]
0A	-b	All-pixel readout 16:9 cropping high speed AD mode	5596	3148	4	756	3174	30.00
	-c					378	3174	60.01

*1 Number of OB without sensor line can be set by OPBN_WIDTH register.
*2 Number of INCK pulse required to output the data for one line.
*3 The number of XHS pulse per 1V period and number of INCK per 1XHS must be even number in every mode.

Note)
The values in the table are the minimum 1XHS and 1V cycle values. When XHS and XVS have longer intervals than these, the sensor outputs a blank code signal. The data is output once per 1 XHS inputs.
The V period and the frame rate shown above is in the case that “Number of OB without sensor line” is the value in the above table and VBLK_WIDTH = 6h and BK_WIDTH = 0h.
The maximum frame rate varies depending on the number of readout lines in window readout mode.

Image Data Output Format

Mode0A: All-pixel Readout 16:9 Cropping High Speed AD Mode

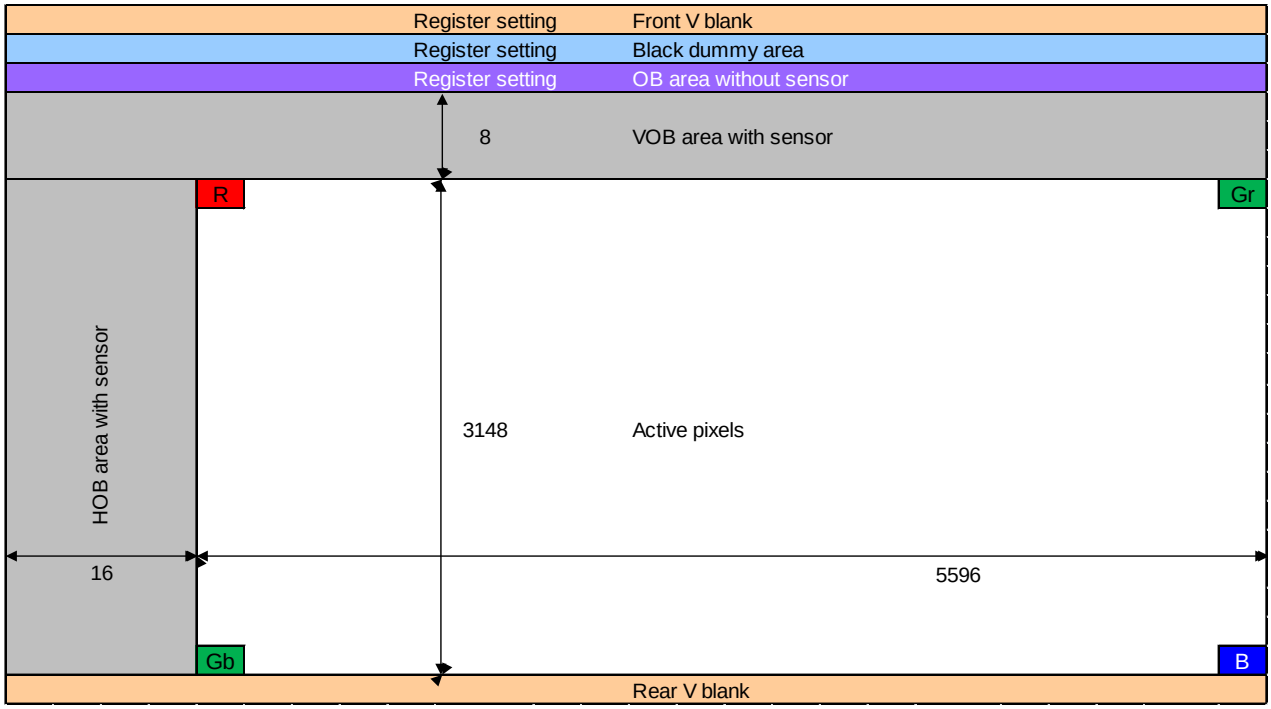


Fig. Readout Image Diagram in Mode0A All-pixel Readout 16:9 Cropping High Speed AD Mode

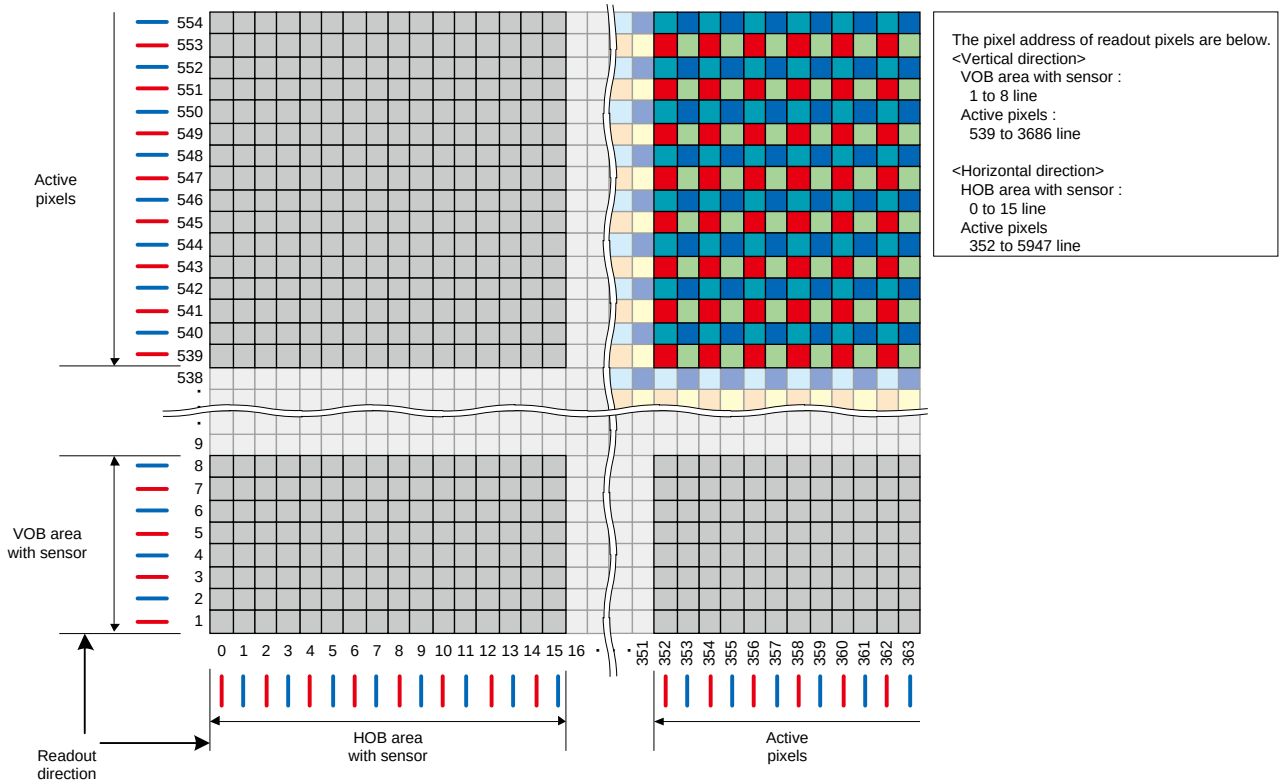
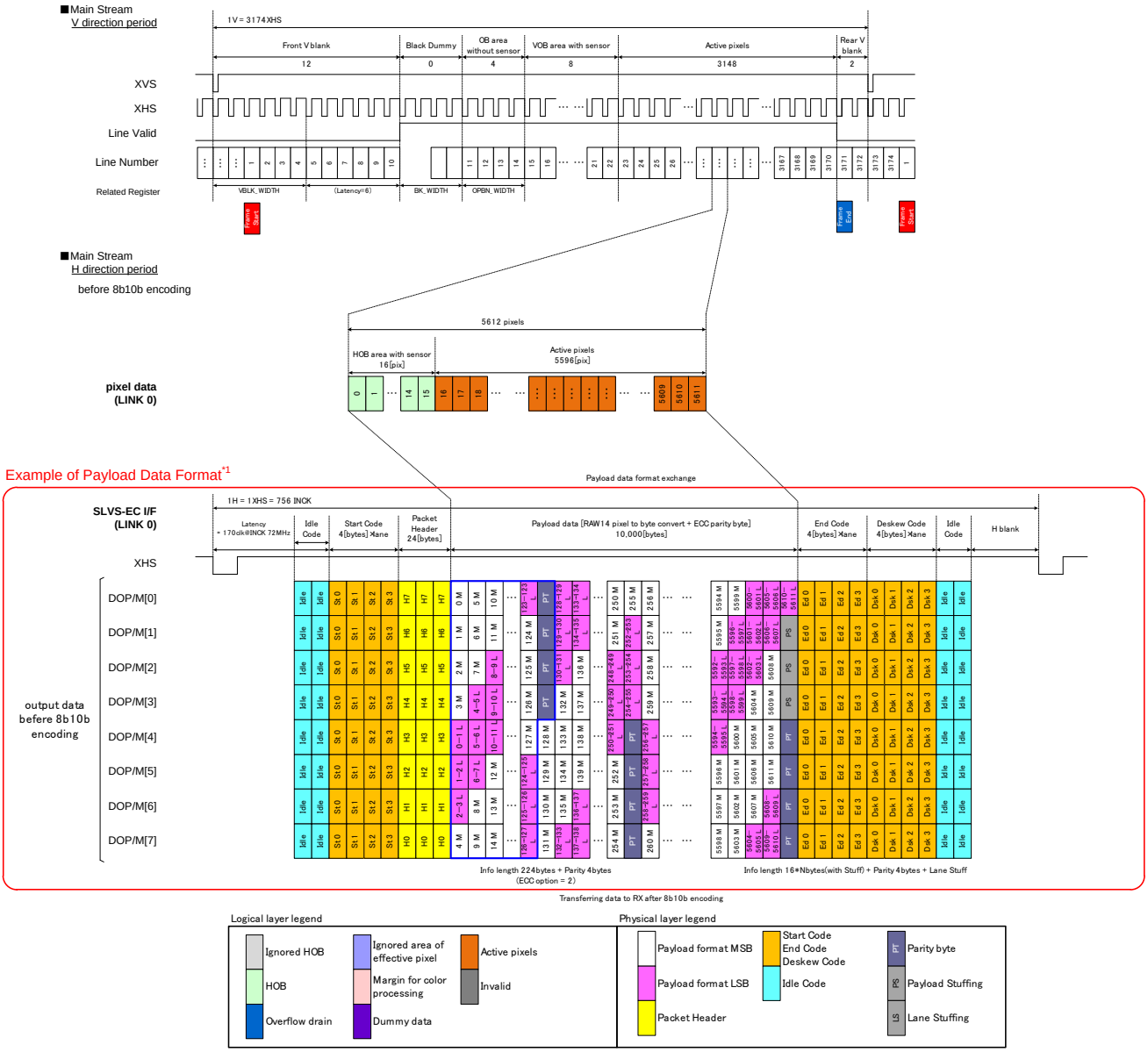


Fig. Binning Image

Timing Chart



*1 Payload Data Format varies each AD bit and word length.
This Payload Data Format is example of Mode0A-b All-pixel Readout Mode 16:9 Cropping (AD 14 bits, Word Length 14 bits).
See "SLVS-EC Specification Version 1.2" for detail of Payload Data Format of other mode.

Fig. Drive Timing in Mode0A All-pixel Readout 16:9 Cropping High Speed AD Mode

Mode Transitions

In case of mode transition from normal AD mode to high speed AD mode, change the AD speed to high by sending following (A) and (B) registers during next invalid frame after sending high speed AD mode (mode-B) registers.
And in case of mode transition from high speed AD mode to normal AD mode, change the AD speed to normal by sending following (C) and (D) registers during next invalid frame after sending normal AD mode (mode-A) registers.
In addition, following AD speed change sequence is unnecessary in case of mode transition between high speed AD modes.

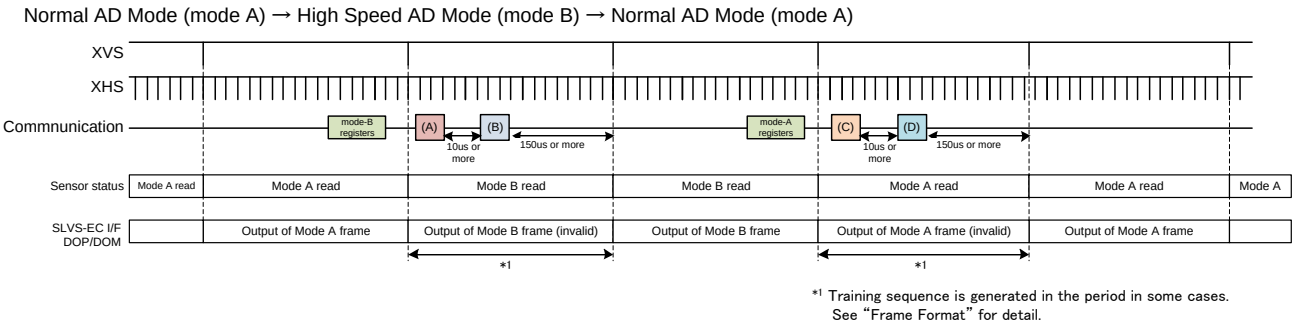


Fig. AD Speed Change Sequence

Table. Setting Registers in AD Mode Chang Sequence

Items	Setting order	Address	Bit	Name	Setting value	Remarks
(A)	1	01F0h	[7:0]	PLL_AD_STB	06h	PLL AD standby off
	2	01F0h	[7:0]	PLL_AD_STB	00h	PLL AD standby on
	3	0366h	[7:0]	PLL_AD_SETTING	0Eh	Setting high speed AD mode
(B)	1	01F0h	[7:0]	PLL_AD_STB	06h	PLL AD standby off
(C)	1	01F0h	[7:0]	PLL_AD_STB	06h	PLL AD standby off
	2	01F0h	[7:0]	PLL_AD_STB	00h	PLL AD standby on
	3	0366h	[7:0]	PLL_AD_SETTING	0Ch	Setting normal AD mode
(D)	1	01F0h	[7:0]	PLL_AD_STB	06h	PLL AD standby off

In addition, PLL_AD_STB register is left 06h setting regardless of AD mode after changing PLL_AD_STB register.

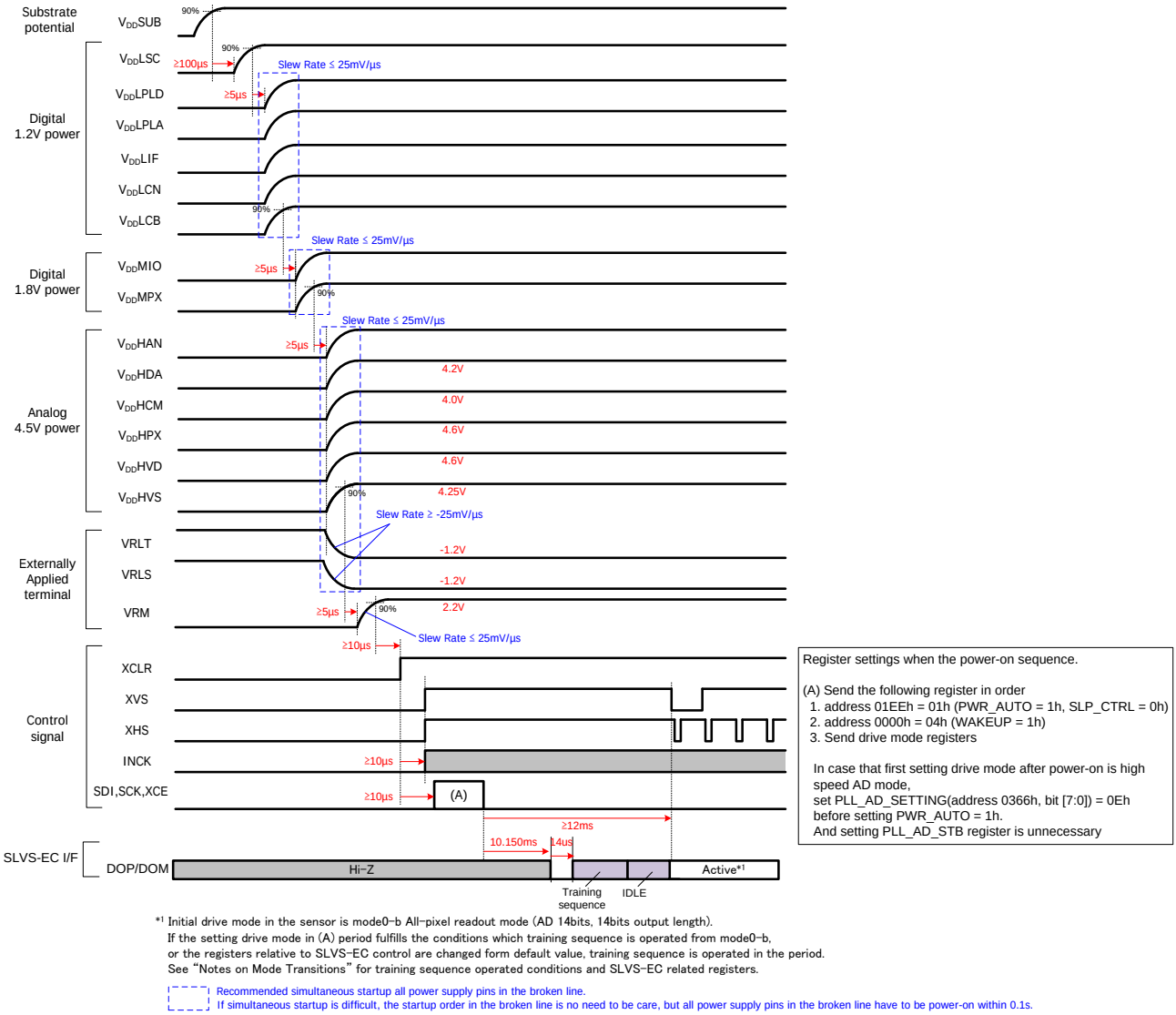
Notes on High Speed AD Mode

- Integration time control and calculation of exposure time are same as normal AD mode.
- Upper limit of analog gain is 24[dB] (EFCh) in high speed AD mode. And additional register setting is same as normal AD mode.
- Window readout function and horizontal freely cropping function are already applicate in the high speed AD mode for 16:9 cropping based on mode0 all-pixel readout. At the same time, cropping area and cropping size can be changed by changing register values of window readout function and horizontal freely cropping function. Restrictions of window readout function and horizontal freely cropping function are same as mode0 and horizontal and vertical pixel size after cropping have to be 5596 × 3148 or less.

Power-ON/OFF Sequence

This sensor is a multi-power supply device, so care must be taken for the power-on sequence.

Power-ON Sequence



Register settings when the power-on sequence.

(A) Send the following register in order
1. address 01EEh = 01h (PWR_AUTO = 1h, SLP_CTRL = 0h)
2. address 0000h = 04h (WAKEUP = 1h)
3. Send drive mode registers

In case that first setting drive mode after power-on is high speed AD mode,
set PLL_AD_SETTING(address 0366h, bit [7:0]) = 0Eh
before setting PWR_AUTO = 1h.
And setting PLL_AD_STB register is unnecessary

*1 Initial drive mode in the sensor is mode0-b All-pixel readout mode (AD 14bits, 14bits output length).
If the setting drive mode in (A) period fulfills the conditions which training sequence is operated from mode0-b,
or the registers relative to SLVS-EC control are changed form default value, training sequence is operated in the period.
See "Notes on Mode Transitions" for training sequence operated conditions and SLVS-EC related registers.

Recommended simultaneous startup all power supply pins in the broken line.
If simultaneous startup is difficult, the startup order in the broken line is no need to be care, but all power supply pins in the broken line have to be power-on within 0.1s.

Fig. Power-ON Sequence

Power-OFF Sequence

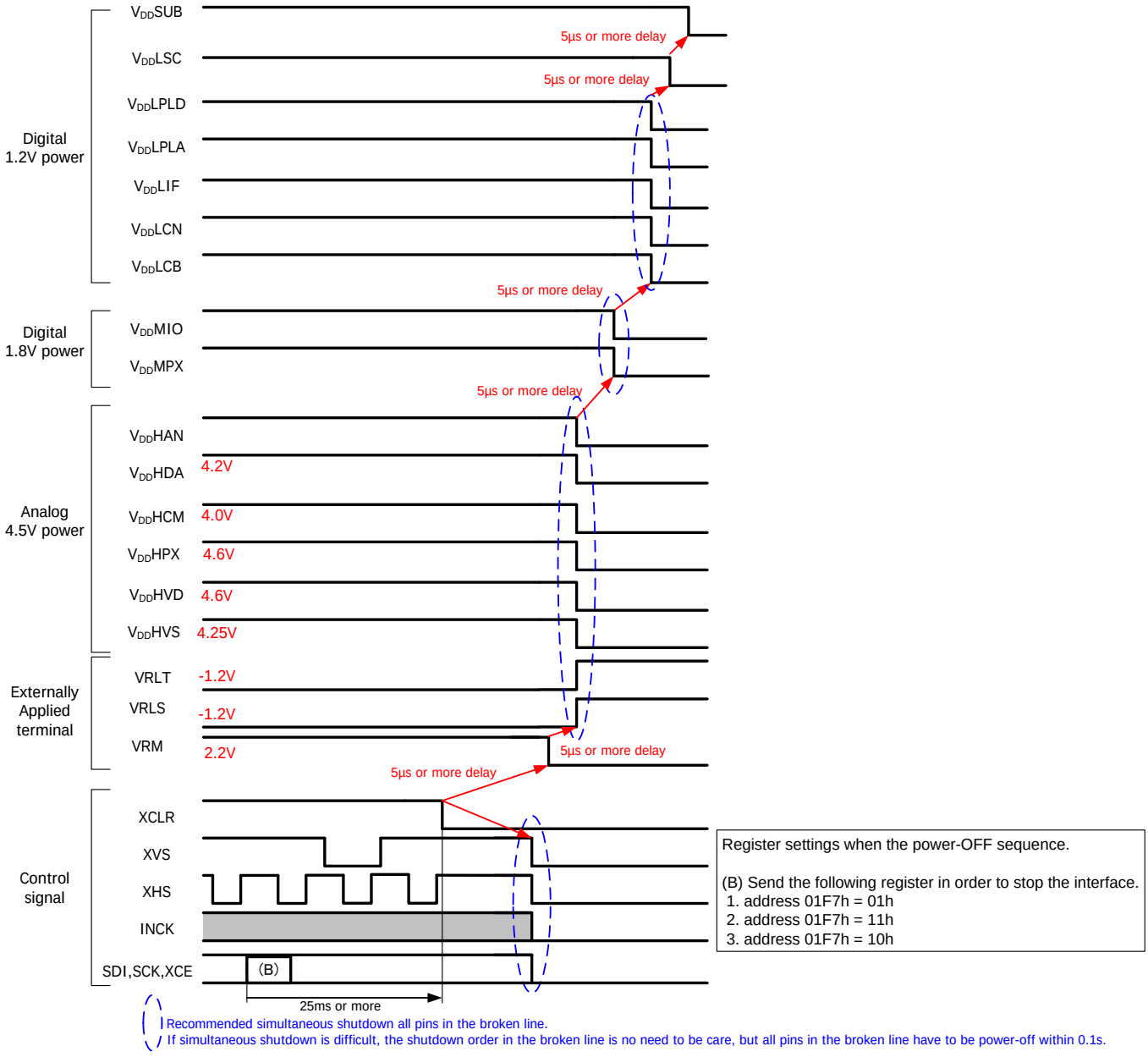


Fig. Power-OFF Sequence

Spot Pixel Specifications

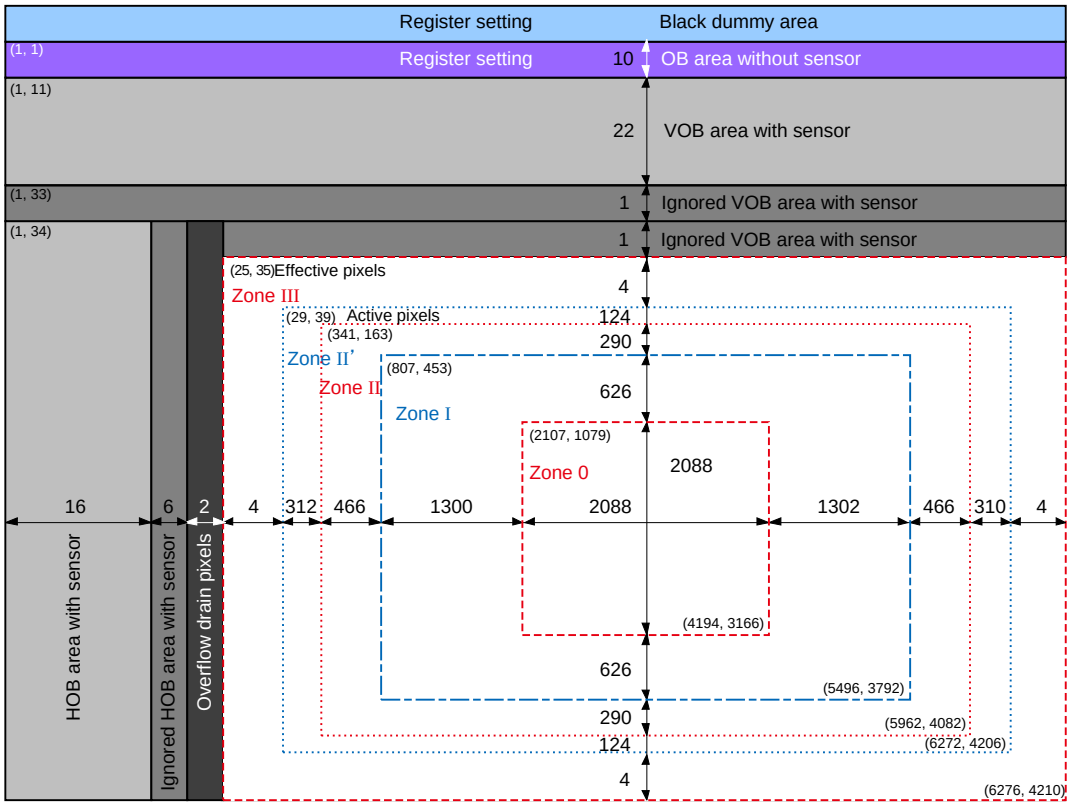
(Sensor signal, Tj = 25 °C)

Type of distortion	Level	Maximum distorted pixels in each zone					Measure-ment method	Remarks
		0, I	II	II'	III	OB		
Black or white pixels at high light	10 % ≤ D	*1			No evaluation criteria applied		1	—
White pixels at low light	60.9 LSB ≤ D	*2			No evaluation criteria applied		2	—
Large white pixels	16382 LSB ≤ D	*3					2	—
White pixels in the dark	75.5 LSB ≤ D ≤ 16381 LSB	*4			No evaluation criteria applied		3	Tj = 60 ˚C Note 3)
Black pixels at signal saturated	D ≤ 13000 LSB	*5			No evaluation criteria applied		4	—
White pixels during long time integration	286 LSB ≤ D	51600			No evaluation criteria applied		3	Tj = 60 ˚C 8 s integration

The total of *1, *2, *3, *4 and *5 should be 6500 or less.
Values above indicate those when analog gain PGC = 0 dB: 1 LSB is converted with 0.08606 mV (14-bit).

Note) 1 D ... Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
2. Zone definition is illustrated in the figure below.
3. After 1/30 s integration, the signal after readout for 1/16.3s is judged.

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	69 pcs
10 mV or higher	38 pcs
24 mV or higher	16 pcs
50 mV or higher	8 pcs
72 mV or higher	5 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

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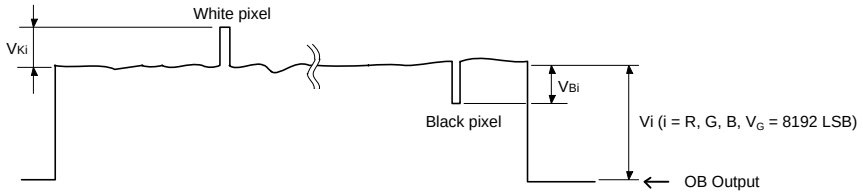
Measurement Method for Spot Pixel

After setting the measurement condition to the standard imaging condition II, the device drive conditions should be within the bias and clock voltage conditions.
Configure the drive circuit according to the example and measure.

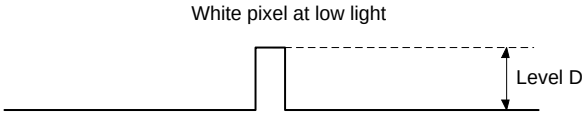
1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value of the G signal output is 8192 LSB, measure the local dip point (black pixel at high light, V_{BR}, V_{BG}, V_{BB}) and peak point (white pixel at high light, V_{KR}, V_{KG}, V_{KB}) in each channel signal output. Substitute the values into the following formula.

   Spot pixel level D = (V_{Ki} (or) V_{Bi})/Vi × 100 [%] (i = R, G, B)



Signal Output Waveform of R/G/B Channels

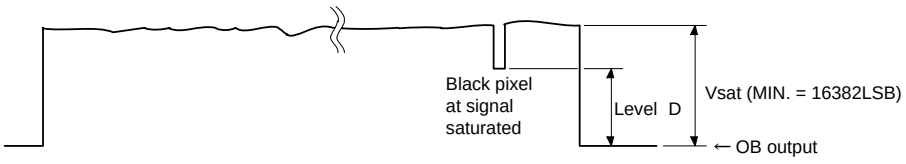
2. White pixels at low light / Large white pixels
   Set the device in dark state and eliminate enough the effect of dark voltage. Then measure the local bright spot value for the signal output after pixel reset.



Signal Output Waveform of R/G/B Channels

3. White pixels in the dark / White pixels during long time integration
   Set the device to a dark setting and measure the local peak point of the signal output waveform in the state where random noise is eliminated using the average value of the dark signal output as a reference.

4. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point in each channel of R/G/B using the OB output with sensor as a reference.



Signal Output Waveform of R/G/B Channels

Spot Pixel Pattern Specifications

The sensor with the following spot pixel patterns is rejected.
Spot pixel patterns other than these patterns should be compensated with camera system.

(1) Pattern of 3 or more adjacent pixels occurring in the horizontal direction with the same color

Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B
R	Gr	**R**	Gr	**R**	Gr

Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr
Gb	B	**Gb**	B	**Gb**	B
R	Gr	R	Gr	R	Gr

Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr
Gb	**B**	Gb	**B**	Gb	**B**
R	Gr	R	Gr	R	Gr

(2) Pattern of 3 or more spot pixels occurring in the horizontal direction with the same color
or in the vertical direction with the same color in the 7 × 7 (= 49) pixel area

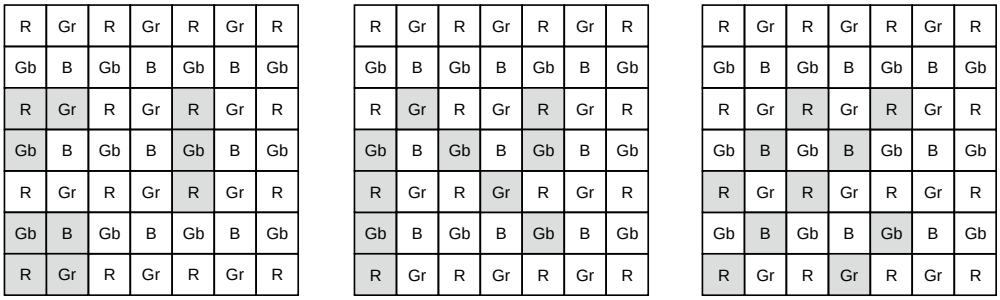
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	**R**	Gr	R	Gr	**R**	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr

Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	**R**	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	R	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	**R**	Gr	R	Gr
Gb	B	Gb	B	Gb	B	Gb	B
R	Gr	R	Gr	**R**	Gr	R	Gr

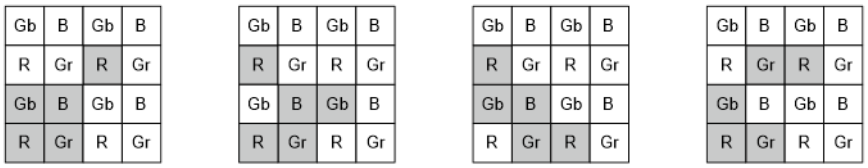
Spot Pixel Pattern Specifications during long time integration

When more patterns than specified are found in the two types of the following spot pixel patterns, the sensor is rejected. Spot pixel patterns other than these patterns should be compensated with camera system.

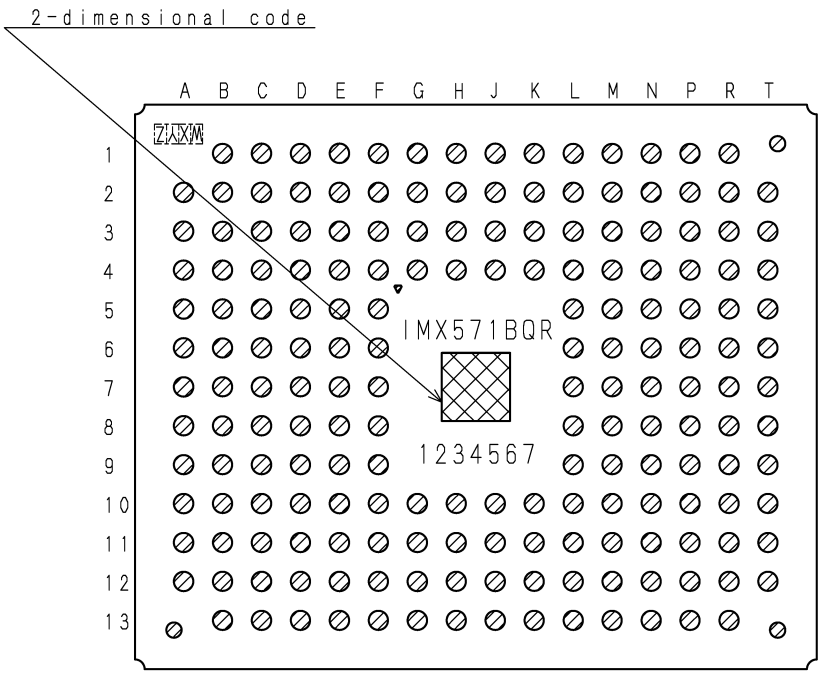
(1) 1 or more patterns with 10 or more spot pixels occurring in the 5 × 5 pixel area



(2) 12 or more patterns with 5 or more spot pixels occurring in the 3 × 3 pixel area



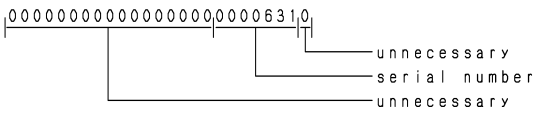
Marking



The 2-dimensional code format for serial number

1. Code Format:Data Matrix(ECC200)
2. Matrix size(2-dimensional code):18×18
3. The details of serial number for the 2-dimensional code
   The serial number for the 2-dimensional code uses the 7 digits between 18 digits and 24 digits.
   (the full digits of serial number is 25 digits.)
4. Serial number consists of numbers only.

(EX.)In the case of No.631(serial number),describe'0000631'.

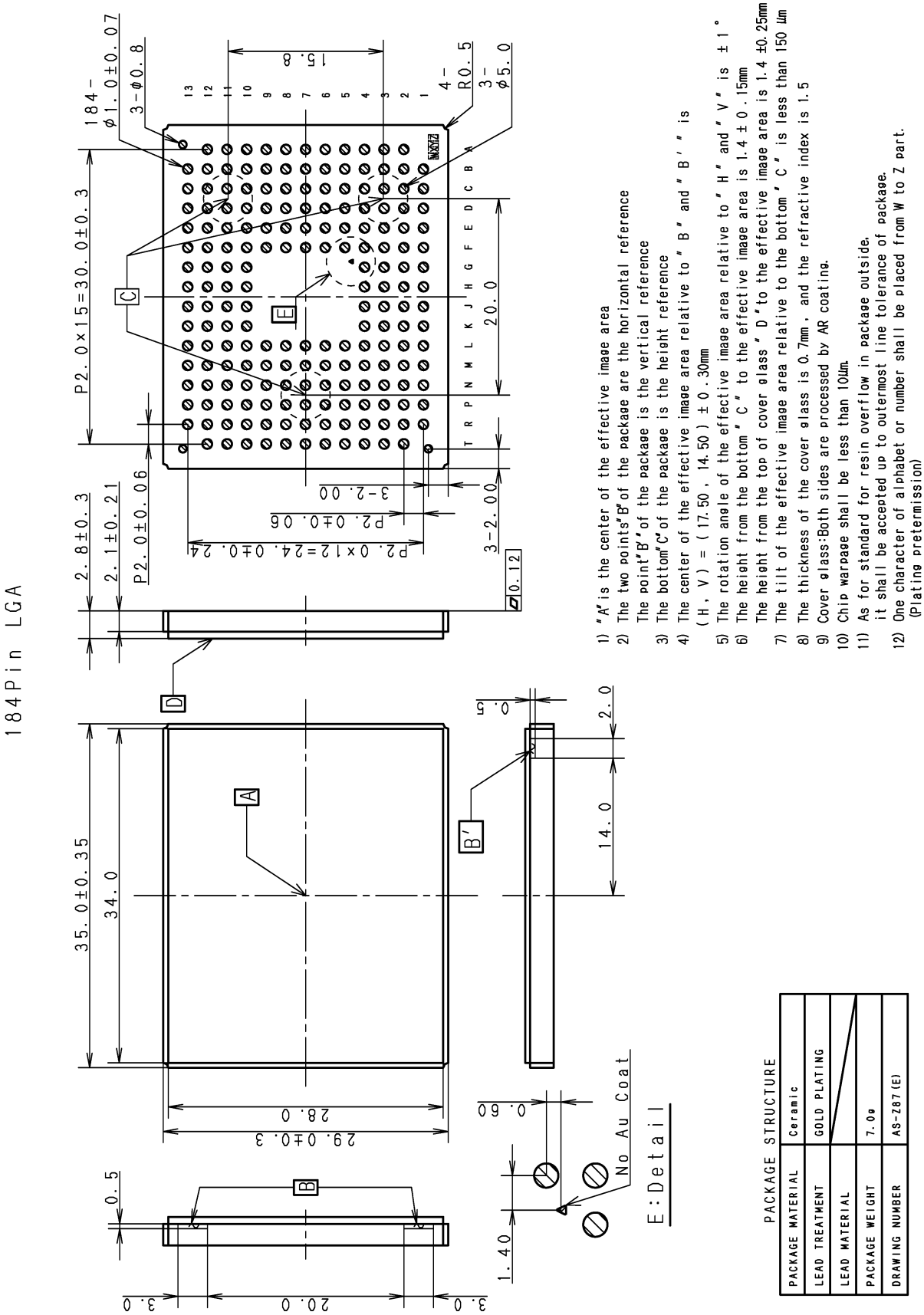


5. Alphanumeric one character is put to the W-Zpart.(no plating)

DRAWING No. AM-Z571BQR(2D)

Package Outline

(Unit: mm)



1) "A" is the center of the effective image area
2) The two points"B"of the package are the horizontal reference
   The point"B'"of the package is the vertical reference
3) The bottom"C"of the package is the height reference
4) The center of the effective image area relative to " B " and " B ' " is
   (H , V) = (17.50 , 14.50) ± 0 .30mm
5) The rotation angle of the effective image area relative to " H " and " V " is ± 1 °
6) The height from the bottom " C " to the effective image area is 1.4 ± 0 .15mm
   The height from the top of cover glass " D "to the effective image area is 1.4 ±0.25mm
7) The tilt of the effective image area relative to the bottom " C " is less than 150 Um
8) The thickness of the cover glass is 0.7mm , and the refractive index is 1.5
9) Cover glass:Both sides are processed by AR coating.
10) Chip warpage shall be less than 10Um.
11) As for standard for resin overflow in package outside,
    it shall be accepted up to outermost line tolerance of package.
12) One character of alphabet or number shall be placed from W to Z part.
    (Plating pretermission)

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT	7.0g
DRAWING NUMBER	AS-Z87(E)

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

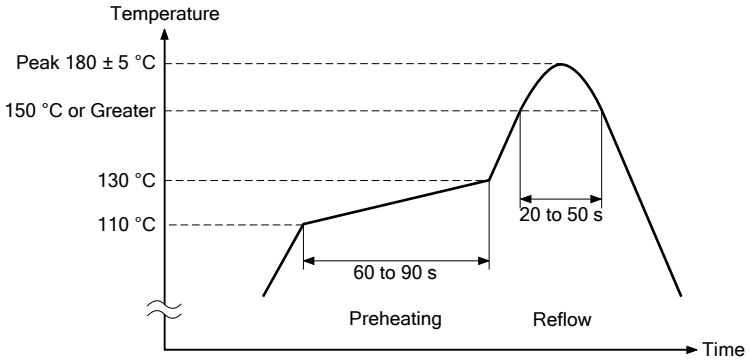
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	110 to 130 °C 60 to 90 s
2. Temperature up (down)	±4 °C/s or less
3. Reflow temperature	150 °C or Greater 20 to 50 s Max. 5 °C/s
4. Peak temperature	Max. 180 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 185 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.
(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) The paste residue of protective tape should be ignored except remarkable one.
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infraredcut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.13-0.0.8