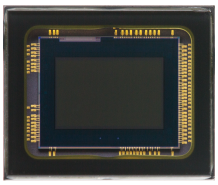
SONY



Diagonal 8.58 mm (Type 1/1.9) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX185LQJ-C

Description

The IMX185LQJ-C is a diagonal 8.58 mm (Type 1/1.9) CMOS active pixel type solid-state image sensor with a square pixel array and 2.38 M effective pixels. This chip operates with analog 3.3 V, digital 1.2 V, and digital 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Input frequency: 27 MHz / 54 MHz / 37.125 MHz / 74.25 MHz
- Number of recommended recording pixels: 1920 (H) × 1200 (V) approx. 2.31 M pixels
- Readout mode
  All-pixel scan mode
  Horizontal / vertical 2/2-line bining readout mode
  1080p-HD readout mode
  Vertical direction normal/inverted readout mode
  Horizontal direction normal/inverted readout mode
  Window cropping mode
- Readout rate
  Maximum frame rate in 1080p-HD readout mode: 120 frame/s
- Variable-speed shutter function (resolution 1H units)
- 10/12-bit A/D converter
- CDS/PGA function
  0 dB to 24 dB: Analog Gain 24 dB (step pitch 0.3 dB)
  24.3 dB to 48 dB: Analog Gain 24 dB + Digital Gain 0.3 to 24 dB (step pitch 0.3 dB)
- Supports I/O switching
  Low voltage LVDS (150 mVp-p) parallel DDR output
  Low voltage LVDS (150 mVp-p) serial (2 ch / 4 ch switching) DDR output
  CSI-2 serial data output (2 Lane / 4 Lane, RAW10/RAW12 output)
- Recommend lens F number: 2.8 or more
- Recommended exit pupil distance: –30 mm to –∞

Exmor™

* “Exmor” is a trademark of Sony Corporation. The “Exmor” is a version of Sony's high performance CMOS image sensor with high-speed processing, low noise and low power dissipation by using column-parallel A/D conversion.

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 8.58 mm (Type 1/1.9)
- ◆Total number of pixels
  1952 (H) × 1241 (V) approx. 2.42 M pixels
- ◆Number of effective pixels
  1945 (H) × 1225 (V) approx. 2.38 M pixels
- ◆Number of active pixels
  1937 (H) × 1217 (V) approx. 2.36 M pixels (WUXGA) Diagonal 8.58 mm
  1937 (H) × 1097 (V) approx. 2.12 M pixels (1080p-HD) Diagonal 8.35 mm
- ◆Number of recommended recording pixels
  1920 (H) × 1200 (V) approx. 2.31 M pixels (WUXGA)
  1920 (H) × 1080 (V) approx. 2.07 M pixels (1080p-HD)
- ◆Chip size
  10.10 mm (H) × 8.05 mm (V)
- ◆Unit cell size
  3.75 µm (H) × 3.75 µm (V)
- ◆Optical black
  Horizontal (H) direction: Front 4 pixels, rear 0 pixels
  Vertical (V) direction : Front 16 pixels, rear 0 pixels
- ◆Dummy
  Horizontal (H) direction: Front 0 pixels, rear 3 pixels
  Vertical (V) direction : Front 0 pixels, rear 0 pixels
- ◆Substrate material
  Silicon

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Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 3.3 V)	AV_{DD}	-0.3	4.0	V	
Supply voltage (digital 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital 1.2 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	+75	˚C	
Storage temperature	Tstg	-30	+80	˚C	
Performance guarantee temperature	Tspec	-10	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	AV_{DD}	3.15	3.3	3.45	V
Supply voltage (digital 1.8 V)	OV_{DD}	1.7	1.8	1.9	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.1	1.2	1.3	V

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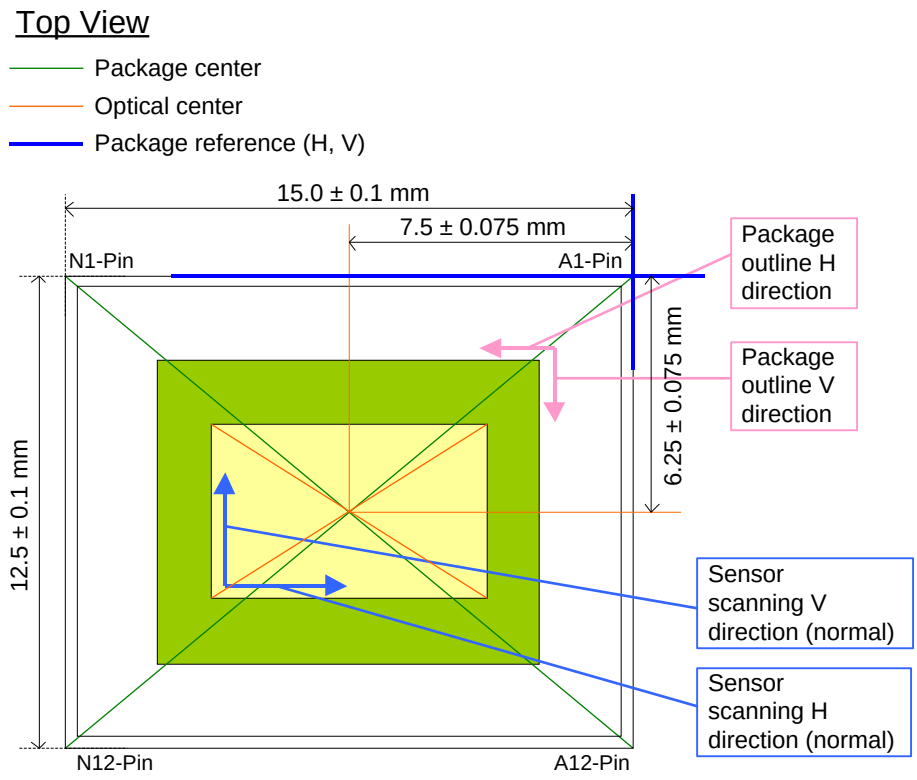
Contents

Chip Center and Optical Center



Optical Center

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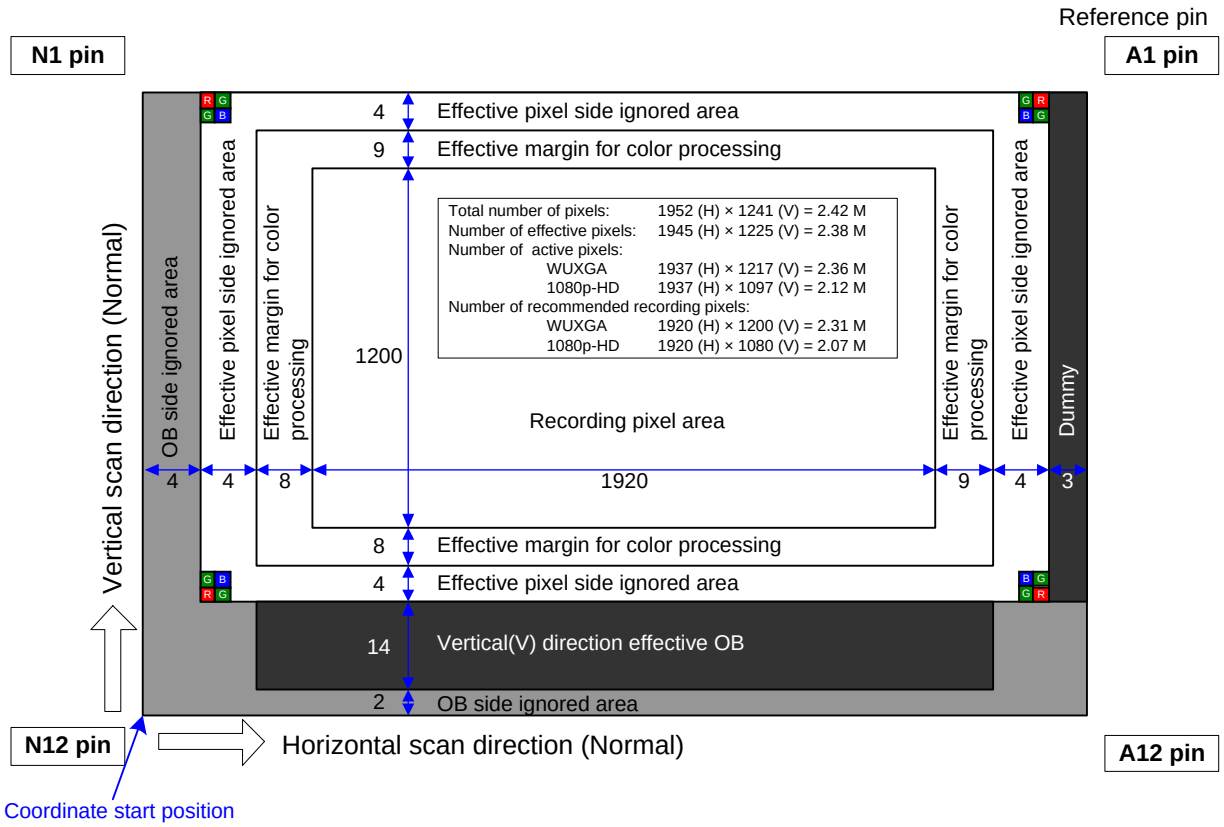
Pixel Arrangement

(Top View)



* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

Pixel Arrangement (Top View)

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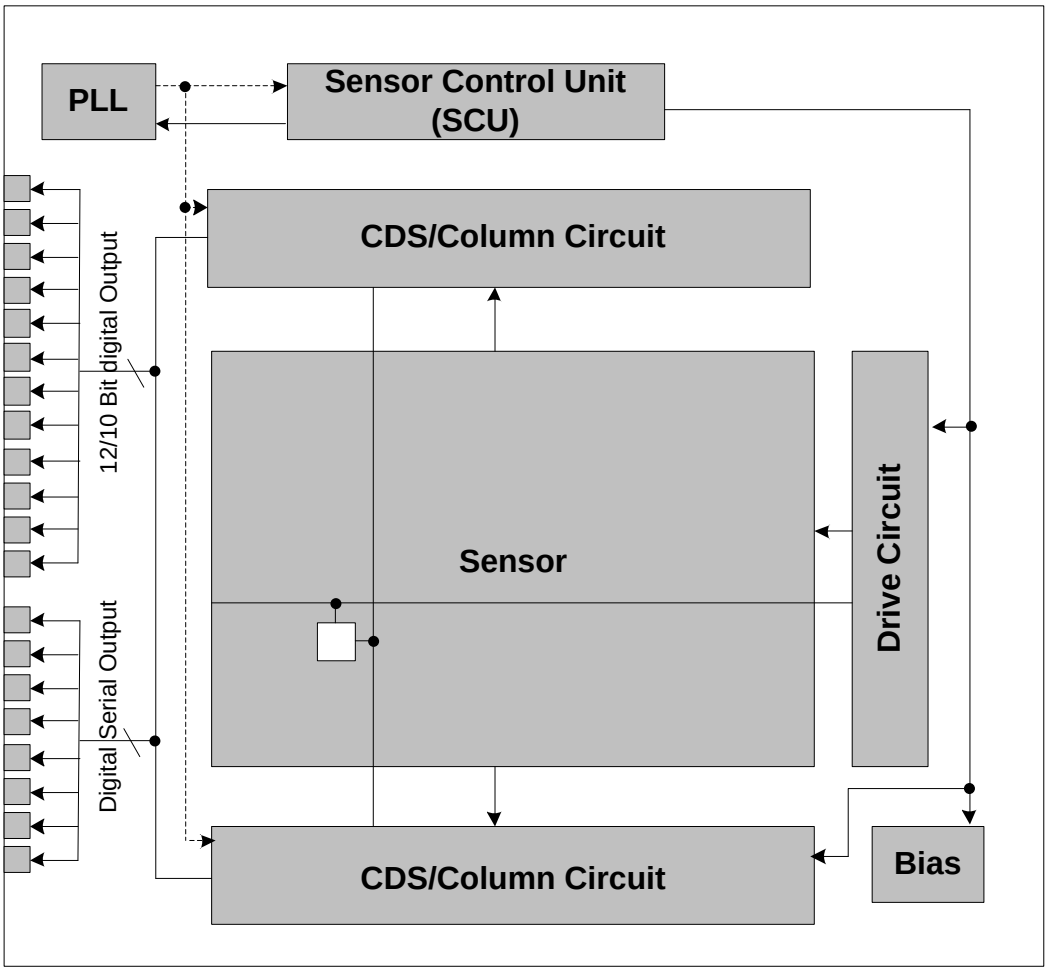
Block Diagram and Pin Configuration

(Top View)



Block Diagram

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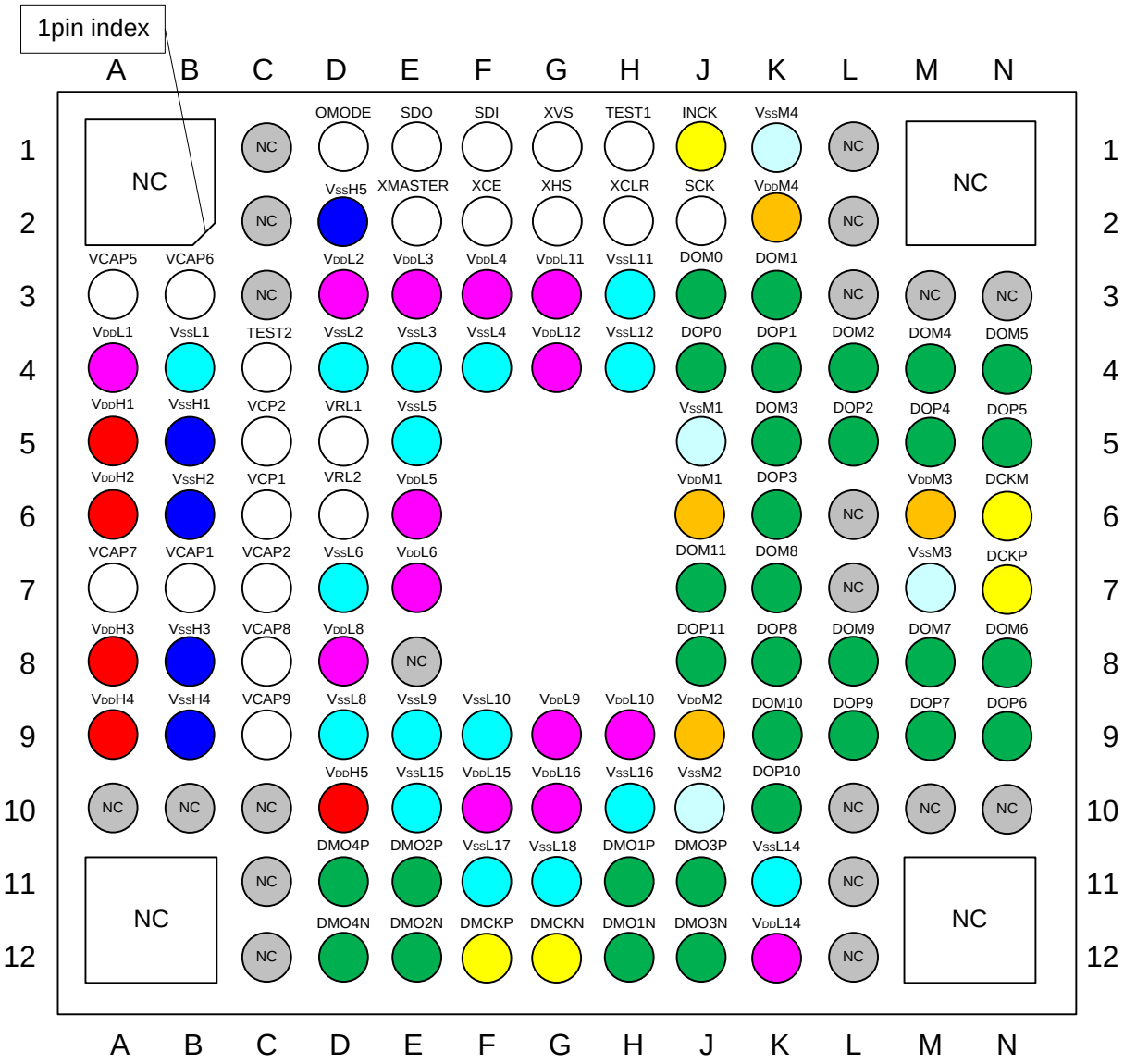

: Analog power supply (3.3 V)

: Analog GND (3.3 V)

: Digital power supply (1.8 V)

: Digital GND (1.8 V)

: Digital power supply (1.2 V)

: Digital GND (1.2 V)

: CLK

: Data output

Pin Configuration (Bottom View)

Pin Description

No.	Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
1	A3	O	A	VCAP5	Reference pin	
2	A4	Power	D	VDDL1	1.2 V power supply	
3	A5	Power	A	VDDH1	3.3 V power supply	
4	A6	Power	A	VDDH2	3.3 V power supply	
5	A7	O	A	VCAP7	Reference pin	
6	A8	Power	A	VDDH3	3.3 V power supply	
7	A9	Power	A	VDDH4	3.3 V power supply	
8	A10	—	—	N.C.		
9	B3	O	A	VCAP6	Reference pin	
10	B4	GND	D	VSSL1	1.2 V GND	
11	B5	GND	A	VSSH1	3.3 V GND	
12	B6	GND	A	VSSH2	3.3 V GND	
13	B7	O	A	VCAP1	Reference pin	
14	B8	GND	A	VSSH3	3.3 V GND	
15	B9	GND	A	VSSH4	3.3 V GND	
16	B10	—	—	N.C.		
17	C1	—	—	N.C.		
18	C2	—	—	N.C.		
19	C3	—	—	N.C.		
20	C4	O	D	TEST2	Test Output Pin	Leave open.
21	C5	O	A	VCP2	Connected to VRL2 pin.	
22	C6	O	A	VCP1	Connected to VRL1 pin.	
23	C7	O	A	VCAP2	Reference pin	
24	C8	O	A	VCAP8	Reference pin	
25	C9	O	A	VCAP9	Reference pin	
26	C10	—	—	N.C.		
27	C11	—	—	N.C.		
28	C12	—	—	N.C.		
29	D1	I	D	OMODE	LVDS/CSI-2 output mode switching (LVDS Mode: High, CSI-2 Mode: Low)	High = OV_{DD}, Low = GND
30	D2	GND	A	VSSH5	3.3 V GND	
31	D3	Power	D	VDDL2	1.2 V power supply	
32	D4	GND	D	VSSL2	1.2 V GND	
33	D5	I	A	VRL1	Connected to VCP1 pin.	
34	D6	I	A	VRL2	Connected to VCP2 pin.	
35	D7	GND	D	VSSL6	1.2 V GND	
36	D8	Power	D	VDDL8	1.2 V power supply	
37	D9	GND	D	VSSL8	1.2 V GND	
38	D10	Power	A	VDDH5	3.3 V power supply	
39	D11	O	D	DMO4P	CSI-2 output 4 Lane	
40	D12	O	D	DMO4N	CSI-2 output 4 Lane	

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No.	Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
41	E1	O	D	SDO	4-wire: Serial interface SDO (Register value output) / I^2C OPEN	
42	E2	I	D	XMASTER	Master / Slave mode switching (Slave Mode: High, Master Mode: Low)	High = OV_{DD}, Low = GND
43	E3	Power	D	VDDL3	1.2 V power supply	
44	E4	GND	D	VSSL3	1.2 V GND	
45	E5	GND	D	VSSL5	1.2 V GND	
46	E6	Power	D	VDDL5	1.2 V power supply	
47	E7	Power	D	VDDL6	1.2 V power supply	
48	E8	—	—	N.C.		
49	E9	GND	D	VSSL9	1.2 V GND	
50	E10	GND	D	VSSL15	1.2 V GND	
51	E11	O	D	DMO2P	CSI-2 output 2 Lane	
52	E12	O	D	DMO2N	CSI-2 output 2 Lane	
53	F1	I	D	SDI/SDA	4-wire: Serial interface SDI (Register value input) / I^2C Serial data input	
54	F2	I	D	XCE	4-wire: Serial interface XCE (Communication enable) / I^2C Fixed to High	High = OV_{DD}, Low = GND
55	F3	Power	D	VDDL4	1.2 V power supply	
56	F4	GND	D	VSSL4	1.2 V GND	
57	F9	GND	D	VSSL10	1.2 V GND	
58	F10	Power	D	VDDL15	1.2 V power supply	
59	F11	GND	D	VSSL17	1.2 V GND	
60	F12	O	D	DMCKP	CSI-2 output clock Lane	
61	G1	I/O	D	XVS	Vertical Sync pulse	
62	G2	I/O	D	XHS	Horizontal Sync pulse	
63	G3	Power	D	VDDL11	1.2 V power supply	
64	G4	Power	D	VDDL12	1.2 V power supply	
65	G9	Power	D	VDDL9	1.2 V power supply	
66	G10	Power	D	VDDL16	1.2 V power supply	
67	G11	GND	D	VSSL18	1.2 V GND	
68	G12	O	D	DMCKN	CSI-2 output clock Lane	
69	H1	I	D	TEST1	Test Input pin. Connect to 1.8 V power supply.	
70	H2	I	D	XCLR	Reset pulse input. (Normal: High, Reset: Low)	High = OV_{DD}, Low = GND

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No.	Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
71	H3	GND	D	VSSL11	1.2 V GND	
72	H4	GND	D	VSSL12	1.2 V GND	
73	H9	Power	D	VDDL10	1.2 V power supply	
74	H10	GND	D	VSSL16	1.2 V GND	
75	H11	O	D	DMO1P	CSI-2 output 1 Lane	
76	H12	O	D	DMO1N	CSI-2 output 1 Lane	
77	J1	I	D	INCK	Master clock input	
78	J2	I	D	SCK/SCL	4-wire: Serial interface SCK (Communication clock input) / I^2C Serial communication clock	
79	J3	O	D	DOM0	When low voltage parallel LVDS: DOM0 When low voltage serial LVDS: Hi-Z	
80	J4	O	D	DOP0	When low voltage parallel LVDS: DOP0 When low voltage serial LVDS: Hi-Z	
81	J5	GND	D	VSSM1	1.8 V GND	
82	J6	Power	D	VDDM1	1.8 V power supply	
83	J7	O	D	DOM11	When low voltage parallel LVDS: DOM11 When low voltage serial LVDS: Hi-Z	
84	J8	O	D	DOP11	When low voltage parallel LVDS: DOP11 When low voltage serial LVDS: Hi-Z	
85	J9	Power	D	VDDM2	1.8 V power supply	
86	J10	GND	D	VSSM2	1.8 V GND	
87	J11	O	D	DMO3P	CSI-2 output 3 Lane	
88	J12	O	D	DMO3N	CSI-2 output 3 Lane	
89	K1	GND	D	VSSM4	1.8 V GND	
90	K2	Power	D	VDDM4	1.8 V power supply	
91	K3	O	D	DOM1	When low voltage parallel LVDS: DOM1 When low voltage serial LVDS: Hi-Z	
92	K4	O	D	DOP1	When low voltage parallel LVDS: DOP1 When low voltage serial LVDS: Hi-Z	
93	K5	O	D	DOM3	When low voltage parallel LVDS: DOM3 When low voltage serial LVDS: Hi-Z	
94	K6	O	D	DOP3	When low voltage parallel LVDS: DOP3 When low voltage serial LVDS: Hi-Z	
95	K7	O	D	DOM8	When low voltage parallel LVDS: DOM8 When low voltage serial LVDS: Hi-Z	
96	K8	O	D	DOP8	When low voltage parallel LVDS: DOP8 When low voltage serial LVDS: Hi-Z	
97	K9	O	D	DOM10	When low voltage parallel LVDS: DOM10 When low voltage serial LVDS: Hi-Z	
98	K10	O	D	DOP10	When low voltage parallel LVDS: DOP10 When low voltage serial LVDS: Hi-Z	
99	K11	GND	D	VSSL14	1.2 V GND	
100	K12	Power	D	VDDL14	1.2 V power supply	
101	L1	—	—	N.C.		
102	L2	—	—	N.C.		
103	L3	—	—	N.C.		
104	L4	O	D	DOM2	When low voltage parallel LVDS: DOM2 When low voltage serial LVDS: Hi-Z	
105	L5	O	D	DOP2	When low voltage parallel LVDS: DOP2 When low voltage serial LVDS: Hi-Z	

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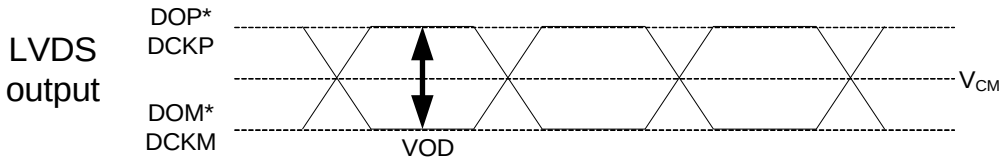
No.	Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
106	L6	—	—	N.C.		
107	L7	—	—	N.C.		
108	L8	O	D	DOM9	When low voltage parallel LVDS: DOM9 When low voltage serial LVDS: Hi-Z	
109	L9	O	D	DOP9	When low voltage parallel LVDS: DOP9 When low voltage serial LVDS: Hi-Z	
110	L10	—	—	N.C.		
111	L11	—	—	N.C.		
112	L12	—	—	N.C.		
113	M3	—	—	N.C.		
114	M4	O	D	DOM4	When low voltage parallel LVDS: DOM4 When low voltage serial LVDS: CHM3	
115	M5	O	D	DOP4	When low voltage parallel LVDS: DOP4 When low voltage serial LVDS: CHP3	
116	M6	Power	D	VDDM3	1.8 V power supply	
117	M7	GND	D	VSSM3	1.8 V GND	
118	M8	O	D	DOM7	When low voltage parallel LVDS: DOM7 When low voltage serial LVDS: CHM4	
119	M9	O	D	DOP7	When low voltage parallel LVDS: DOP7 When low voltage serial LVDS: CHP4	
120	M10	—	—	N.C.		
121	N3	—	—	N.C.		
122	N4	O	D	DOM5	When low voltage parallel LVDS: DOM5 When low voltage serial LVDS: CHM1	
123	N5	O	D	DOP5	When low voltage parallel LVDS: DOP5 When low voltage serial LVDS: CHP1	
124	N6	O	D	DCKM	When low voltage parallel LVDS: DCKM When low voltage serial LVDS: DCKM	
125	N7	O	D	DCKP	When low voltage parallel LVDS: DCKP When low voltage serial LVDS: DCKP	
126	N8	O	D	DOM6	When low voltage parallel LVDS: DOM6 When low voltage serial LVDS: CHM2	
127	N9	O	D	DOP6	When low voltage parallel LVDS: DOP6 When low voltage serial LVDS: CHP2	
128	N10	—	—	N.C.		

* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}		3.15	3.30	3.45	V
	Digital	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER OMODE SCK/SCL SDI/SDA XCE	VIH	XVS/XHS in slave mode	0.8 OV_{DD}	—	—	V
			VIL		—	—	0.2 OV_{DD}	V
Digital output voltage		DOP [11:0] DOM [11:0] DCKP DCKM	VCM	Low voltage LVDS	—	$OV_{DD}/2$	—	V
			VOD	Low voltage LVDS (Termination resistance100 Ω)	100	150	200	mV
		XHS XVS SDO	VOH	XVS/XHS In master mode	OV_{DD} -0.4	—	—	V
			VOL		—	—	0.4	V



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Power Consumption

Item	Pins	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current Low-voltage LVDS parallel output 12 bit, 50 frame/s All-pixel readout mode	VDDH	IAV_{DD}	88	88	113	113	mA
	VDDM	IOV_{DD}	25	25	34	34	mA
	VDDL	IDV_{DD}	97	124	130	180	mA
Operating current Low-voltage LVDS parallel output 12 bit, 60 frame/s 1080p-HD mode	VDDH	IAV_{DD}	88	88	113	113	mA
	VDDM	IOV_{DD}	25	25	35	35	mA
	VDDL	IDV_{DD}	97	124	130	180	mA
Operating current Low-voltage LVDS serial 4 ch output 12 bit, 60 frame/s 1080p-HD mode	VDDH	IAV_{DD}	88	88	113	113	mA
	VDDM	IOV_{DD}	14	14	23	23	mA
	VDDL	IDV_{DD}	97	124	130	180	mA
Operating current CSI-2 serial output 4 Lane 12 bit, 60 frame/s 1080p-HD mode	VDDH	IAV_{DD}	88	88	113	113	mA
	VDDM	IOV_{DD}	2	2	4	4	mA
	VDDL	IDV_{DD}	110	130	150	190	mA
Standby current	VDDH	IAV_{DD}_STB	—		0.2		mA
	VDDM	IOV_{DD}_STB	—		0.1		mA
	VDDL	IDV_{DD}_STB	—		7.0		mA

Operating current:
(Typical value condition) : Supply voltage 3.3 V / 1.8 V / 1.2 V, 1/3 quantity of light of saturation, Tj = 25 °C
(Maximum value condition) : Supply voltage 3.45 V / 1.9 V / 1.3 V, worst state of internal circuit operating current consumption, Tj = 60 °C
Standby (Maximum value condition) : Supply voltage 3.45 V / 1.9 V / 1.3 V, Tj = 60 °C, INCK = 0 V

Standard luminous intensity: luminous intensity at standard imaging condition I
Saturated luminous intensity: luminous intensity when the sensor is saturated.

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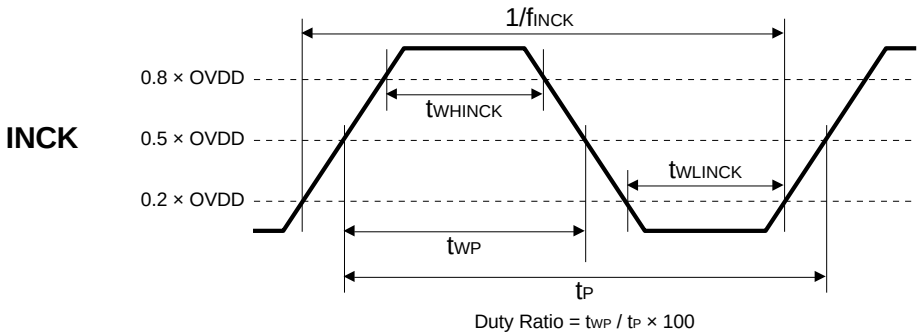
AC Characteristics

Master Clock Waveform Diagram



Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK Low level width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK High level width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

* The INCK fluctuation affects the frame rate.

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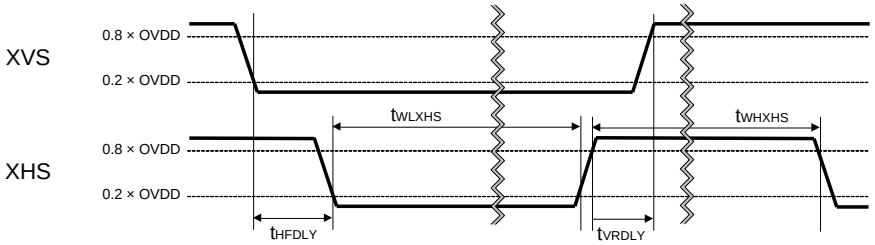
XVS / XHS Input Characteristics In Slave Mode (XMASTER pin = High)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS-XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	
XHS-XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	

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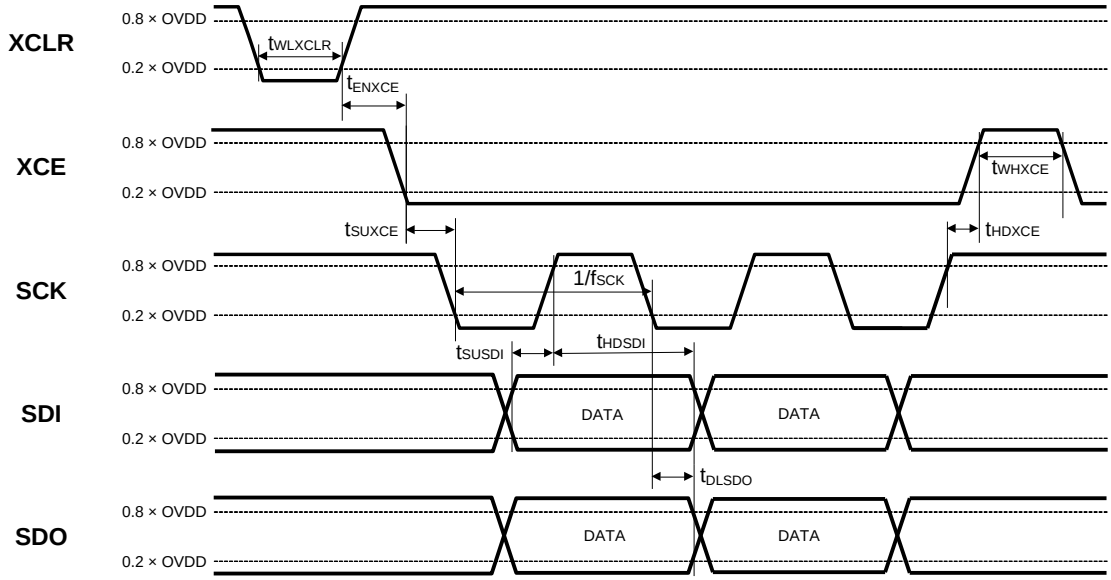
Serial Communication

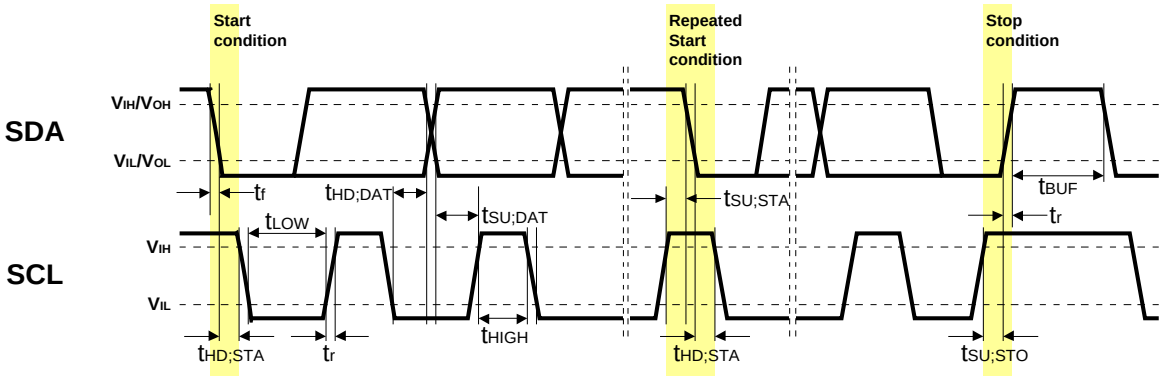
4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

TENTATIVE

I²C



I²C Specification

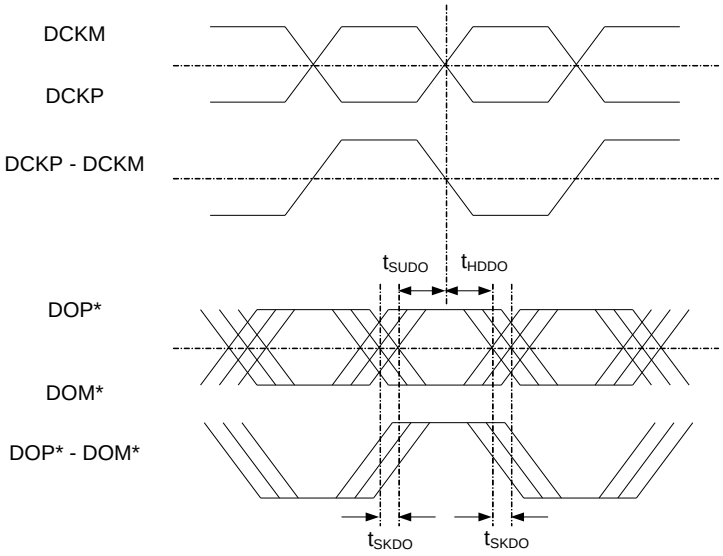
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

TENTATIVE

Low Voltage LVDS DDR Output



Parallel Output

(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCKP clock duty	—	45	50	55	%	DCK = 148.5 MHz (Max.)
DO skew time	t_{SKDO}	—	—	550	ps	Data Rate 148.5 MHz DDR
DO setup time	t_{SUDO}	800	—	—	ps	Data Rate 148.5 MHz DDR
DO hold time	t_{HDDO}	800	—	—	ps	Data Rate 148.5 MHz DDR

Serial Output

(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCKP clock duty	—	40	50	60	%	DCK = 297 MHz (Max.)
DO skew time	t_{SKDO}	—	—	400	ps	Data Rate 297 MHz DDR
DO setup time	t_{SUDO}	400	—	—	ps	Data Rate 297 MHz DDR
DO hold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK	TBD	XVS XHS	TBD
XCLR		SDO	
XMASTER XCE OMODE		SDI/SDA SCK/SCL	
VCP1 VCP2		VCAP1 VCAP7	
VRL1 VRL2		VCAP2	
DOPx DOMx DCKP DCKM		VCAP5 VCAP6	
DMOxP DMOxN DMCKP DMCKN		VCAP8 VCAP9	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

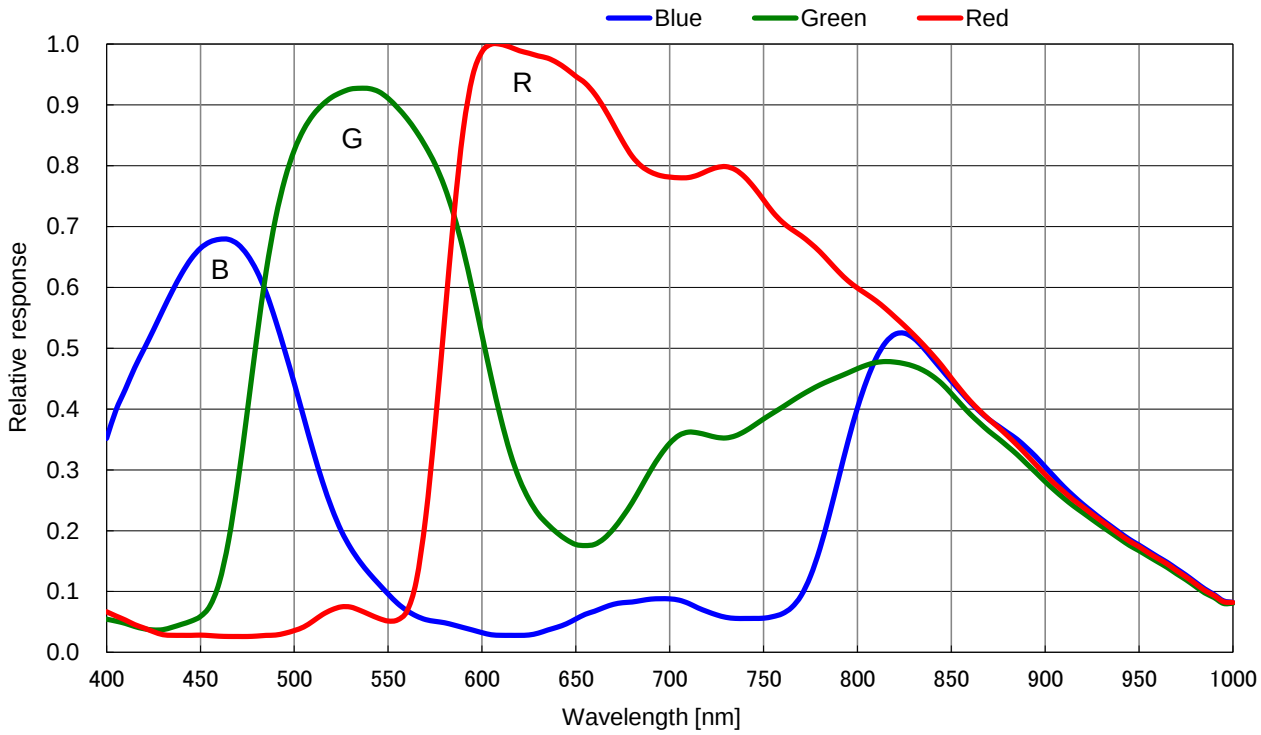


Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode 12 bit, 30 frame/s, Gain = 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	2679 (975)	3077 (1120)	—	Digit (mV)	1	1/30 s storage 12-bit output
Sensitivity ratio	R/G	RG	TBD	—	TBD	—	2	
	B/G	BG	TBD	—	TBD	—		
Saturation signal		Vsat01	3956 (1440)	—	—	Digit (mV)	3	Zone0, I 12-bit output
		Vsat2D	3956 (1440)	—	—	Digit (mV)		Zone0 to II' 12-bit output
Video signal shading		SH01	—	—	20	%	4	Zone0, I
		SH2D	—	—	25	%		Zone0 to II'
Dark signal		Vdt	—	—	0.41 (0.15)	Digit (mV)	5	1/30 s storage 12-bit output
Dark signal shading		ΔVdt	—	—	0.41 (0.15)	Digit (mV)	6	1/30 s storage 12-bit output
Line crawl R		Lcr	—	—	6	%	7	
Line crawl B		Lcb	—	—	6	%		
Lag		Lag	—	—	0.50	%	8	

Note) 1. Converted value into mV using 1Digit = 1.454 mV for 10 bit output and 1Digit = 0.364 mV for 12 bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the glass.

Video Shading Zone Definition

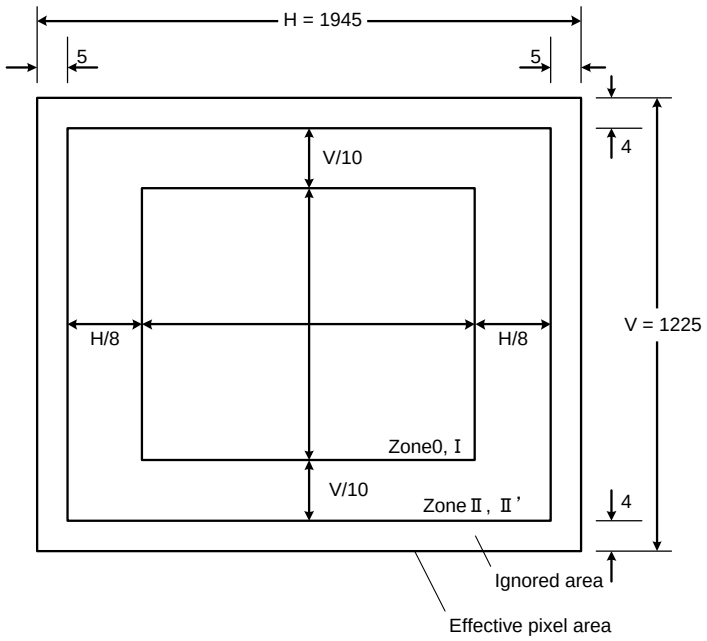


Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

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Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   $$Sg = (VGr + VGb) / 2 \times 100 / 30 \text{ [mV]}$$

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 1120 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   $$VG = (VGr + VGb) / 2$$
   $$RG = VR / VG$$
   $$BG = VB / VG$$

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 500 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 1120 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   $$SH = (Gmax - Gmin) / 1120 \times 100 \text{ [\%]}$$

5. Dark signal
   With the device junction temperature of 60 °C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Line crawl
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr signal output to 1120 mV, insert R and B filters and measure the difference between G signal lines (ΔGlr, ΔGlb [mV]) as well as the average values of the G signal outputs (Gar, Gab). Substitute the values into the following formula.

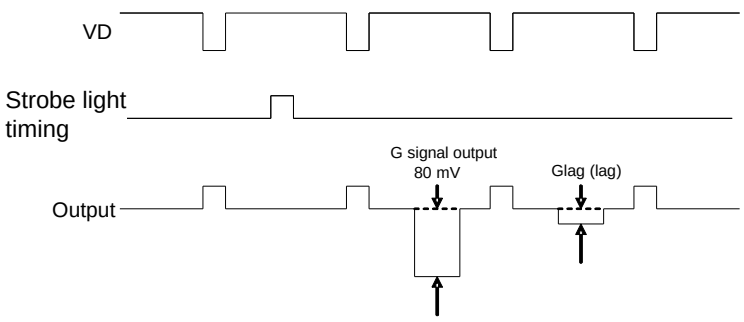
   $$Lci = (\Delta Gli / Gai) \times 100 \text{ [\%]} \quad (i = r, b)$$

TENTATIVE

8. Lag

Adjust the G signal output value generated by strobe light to 80 mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Glag), and substitute the value into the following formula.

Lag = (Glag / 80) × 100 [%]



Setting Registers with Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

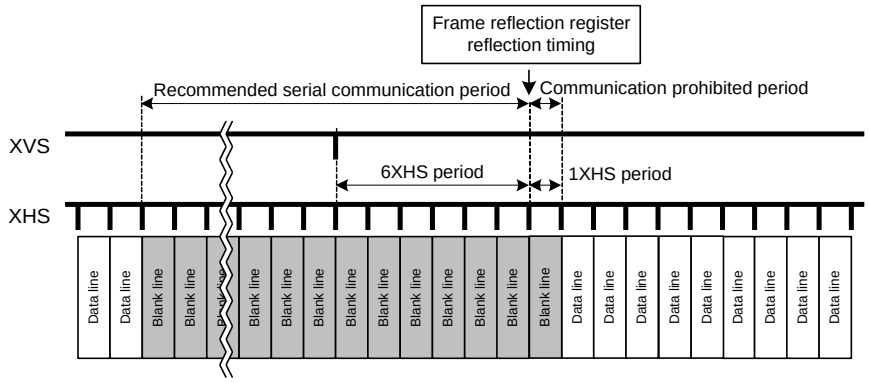
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	02h: Write to the CID = 02h register 03h: Write to the CID = 03h register 04h: Write to the CID = 04h register 05h: Write to the CID = 05h register 82h: Read from the CID = 02h register 83h: Read from the CID = 03h register 84h: Read from the CID = 04h register 85h: Read from the CID = 05h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within in the 6XHS period after the falling edge of XVS from the blanking line output start time after valid line of one frame is finished. (In CSI-2 output master mode, this period is from the blanking line after FE to before 2 H period from FS.) For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.)



Register Write and Read (4-wire)

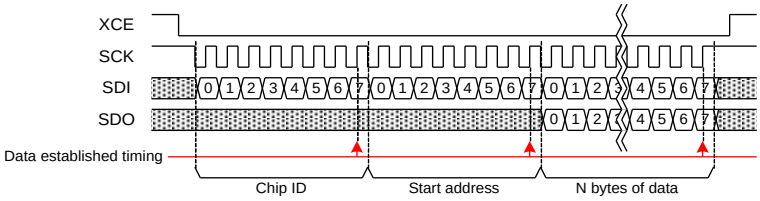
Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h or 03h or 04h or 05h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

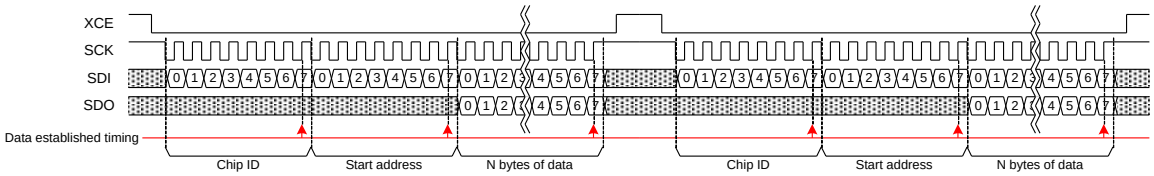
Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h or 83h or 84h or 85h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



Serial Communication (Continuous Addresses)

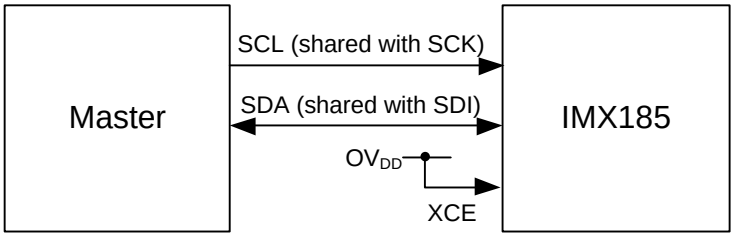


Serial Communication (Discontinuous Addresses)

TENTATIVE

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

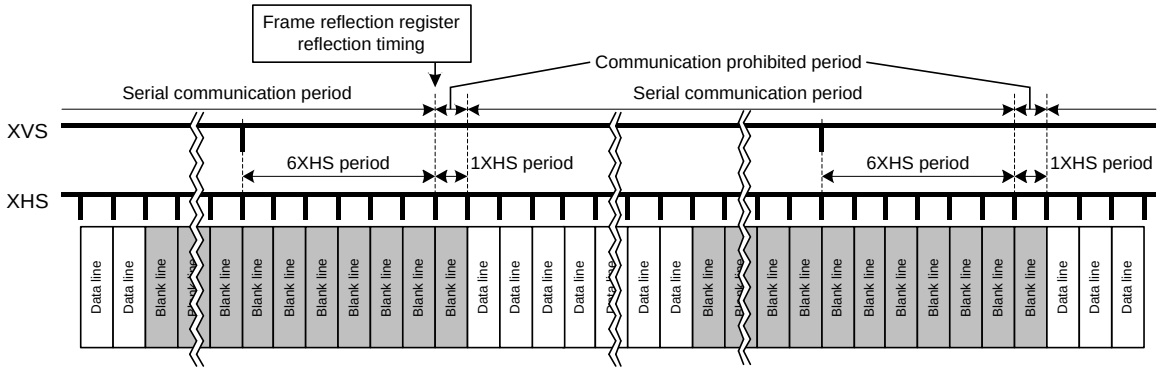
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	J2	Serial clock input
SDA (common to SDI)	F1	Serial data communication

Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 6H after (1 H period : In CSI-2 output master mode, before 1 H period from FS). For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REG_HOLD function is recommended for register setting using I^2C communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”.



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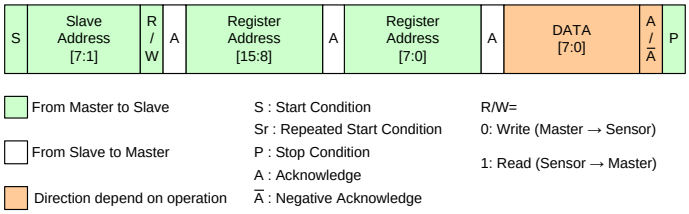
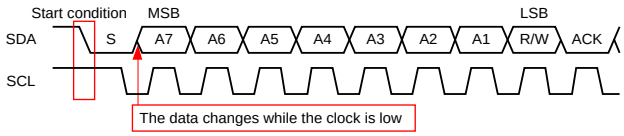
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

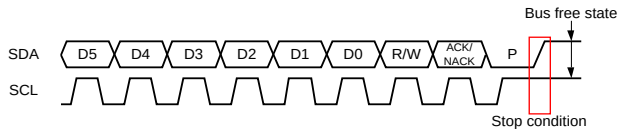


Communication protocol

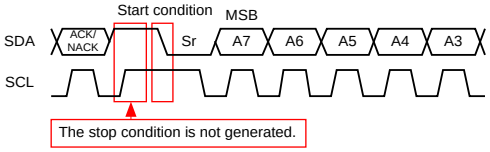
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

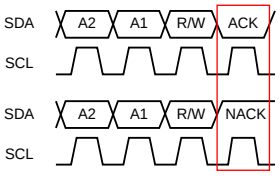


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



Acknowledge and Negative Acknowledge

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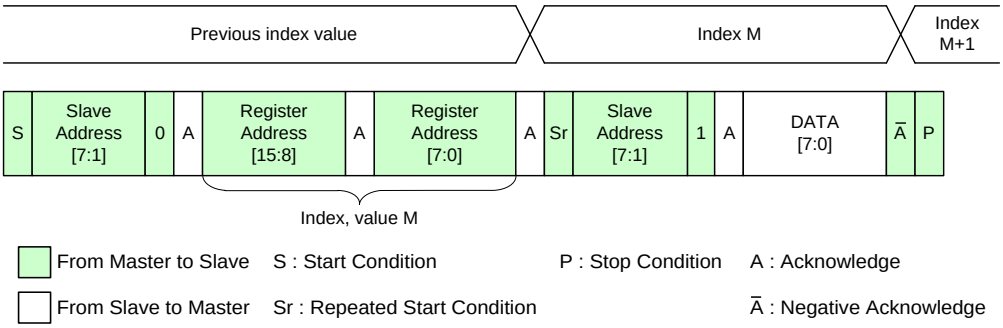
I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

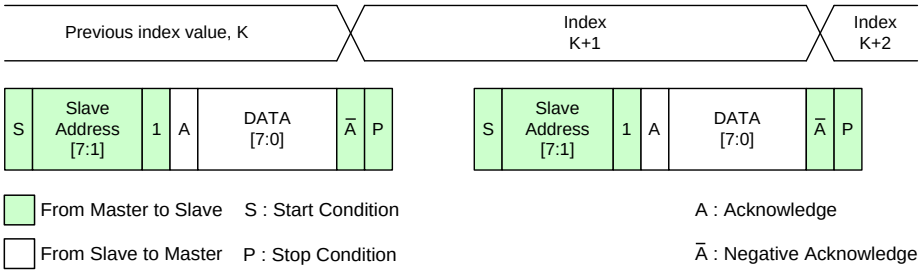
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.

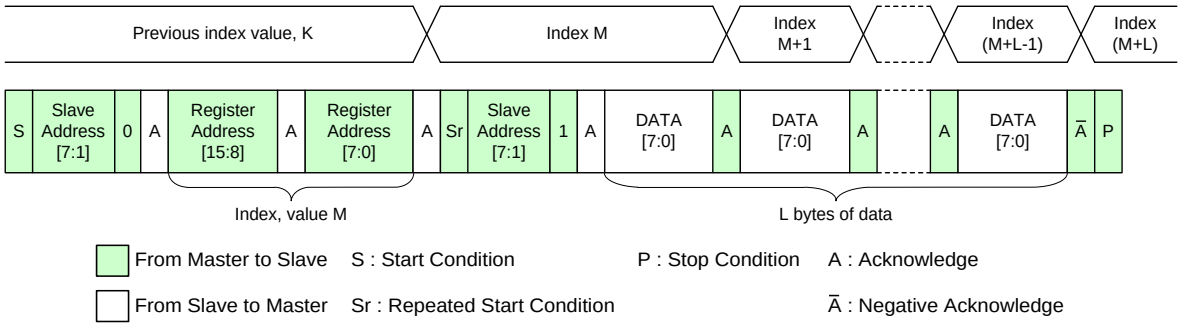


Single Read from Current Location

TENTATIVE

Sequential Read Starting from Random Location

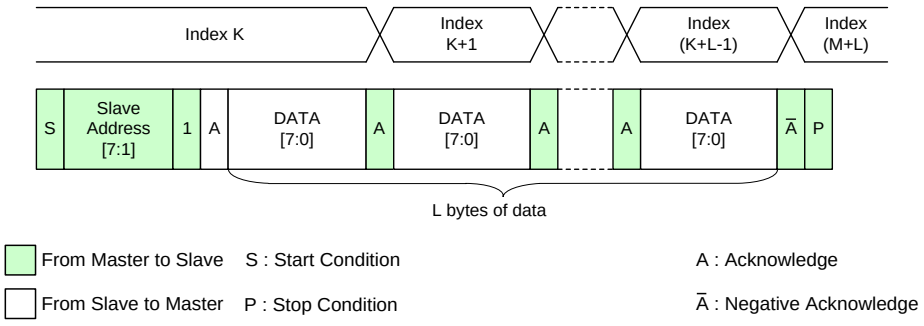
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.

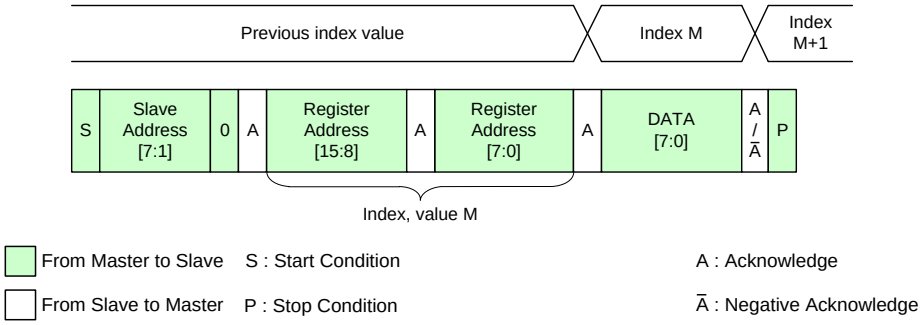


Sequential Read Starting from Current Location

TENTATIVE

Single Write to Random Location

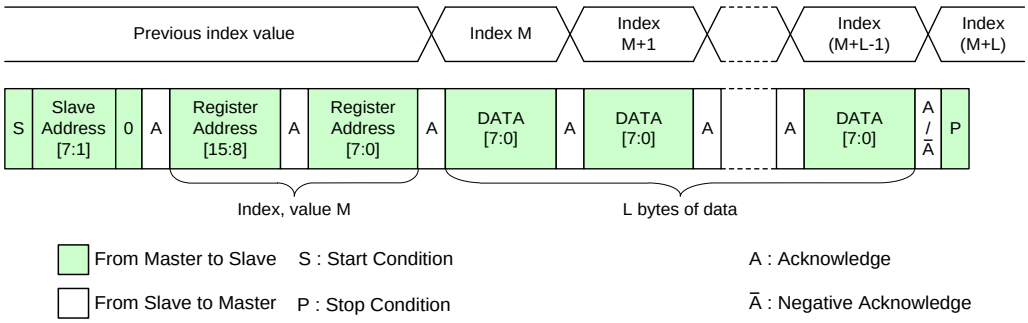
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

In 4-wire serial communication, this sensor has a total of 1020 bytes of registers, composed of registers with addresses 00h to FFh that correspond to Chip ID = 02h (write mode) / 82h (read mode), registers with addresses 00h to FFh that correspond to Chip ID = 03h (write mode) /83h (read mode), registers with addresses 00h to FFh that correspond to Chip ID = 04h (write mode) /84h (read mode).and registers with addresses 00h to FFh that correspond to Chip ID = 05h (write mode) /85h (read mode). Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 1020 bytes. I^2C communication has also the same number of registers, so perform the same way above. See the table below and on the following pages for 4-wire serial communication and I^2C communication address correspondence.

The register setting of Chip ID = 05h (write mode) /85h (read mode) is only for CSI-2 output mode. Therefore these registers need not be set in low-voltage LVDS output modes.

(1) 4-wire serial communication: Chip ID = 02h / I^2C communication: 30**h

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h	3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
01h	3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
02h	3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
03h	3003h	0	SW_RESET	Software reset 0: Operating 1: Reset	0h	00h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
04h	3004h	[7:0]		Fixed to "10h"	10h	10h	

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
05h	3005h	0	ADBIT	AD conversion bits setting 0: 10 bit, 1:12 bit	1h	01h	V
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	STD12EN	Data processing setting when 10-bit AD conversion *Valid only when ADBIT = 0 0: No bit shift 1: 2 bit shift leftward (AD 12 bit normalization)	0h		V
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
06h	3006h	0	MODE [5:0]	Drive mode setting 00h: All-pix scan mode 22h: Horizontal / vertical 2/2-line bining readout mode Others: Setting prohibited	00h	00h	V
		1					
		2					
		3					
		4					
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
07h	3007h	0	VREVERSE	Vertical (V) direction readout inversion control 0:Normal, 1:Inverted	0h	10h	V
		1	HREVERSE	Horizontal (H) direction readout inversion control 0:Normal, 1:Inverted	0h		V
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	WINMODE [3:0]	Window mode setting 0: WUXGA mode 1: 1080p mode 2: 720p mode 4: Window cropping mode (from WUXGA mode) 5: Window cropping mode (from 1080p mode) 6: Window cropping mode (from 720p mode)	1h		V
		5					
		6					
		7					

08h	3008h	[7:0]		Fixed to "10h"	10h	10h	

09h	3009h	0	FRSEL [1:0]	Frame rate grade setting 0: High speed mode, 1: Middle speed mode, 2: Low speed mode 3: Setting prohibited See the detailed description in register list for each mode	2h	02h	V
		1					
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
0Ah	300Ah	0	BLKLEVEL [8:0]	LSB	0F0h	F0h	V
		1					
		2					
		3					
		4		Black level offset value setting			
		5					
		6					
		7					
0Bh	300Bh	0		MSB		00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
0Ch	300Ch	[7:0]		Fixed to "00h"	00h	00h	
0Dh	300Dh	[7:0]		Fixed to "00h"	00h	00h	
0Eh	300Eh	[7:0]		Fixed to "01h"	01h	01h	
0Fh	300Fh	[7:0]		Fixed to "01h"	01h	01h	
10h	3010h	[7:0]		Fixed to "39h"	39h	39h	
11h	3011h	[7:0]		Fixed to "00h"	00h	00h	
12h	3012h	[7:0]		Fixed to "50h"	50h	50h	
13h	3013h	[7:0]		Fixed to "00h"	00h	00h	
14h	3014h	0	GAIN [7:0]	LSB	00h	00h	V
		1					
		2					
		3					
		4		Gain setting			
		5					
		6					
		7		MSB			
15h	3015h	[7:0]		Fixed to "00h"	00h	00h	
16h	3016h	[7:0]		Fixed to "08h"	08h	08h	
17h	3017h	[7:0]		Fixed to "00h"	00h	00h	

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
18h	3018h	0	VMAX [16:0]	LSB	00465h	65h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Vertical span setting (Effective in master mode. Invalid in slave mode) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions"			
19h	3019h	0				04h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Ah	301Ah	0		MSB		00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
1Bh	301Bh	0	HMAX [15:0]	LSB	0898h	98h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7		Horizontal span setting (Effective in master mode. Invalid in slave mode) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions".			
1Ch	301Ch	0				08h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

1Dh	301Dh	[7:0]		Set to "08h"	FFh	FFh	
1Eh	301Eh	[7:0]		Set to "02h"	01h	01h	
1Fh	301Fh	[7:0]		Fixed to "00h"	00h	00h	

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
20h	3020h	0	SHS1 [16:0]	LSB	00000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3021h	0		Storage time adjustment Designated in line units		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
22h	3022h	0		MSB		00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
23h to 35h	3023h to 3035h	[7:0] to [7:0]		Do not rewrite			

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
36h	3036h	0	WINWV_OB [4:0]	LSB In window cropping mode VOB size designation (Vertical direction) MSB	10h	10h	V
		1					
		2					
		3					
		4					
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
37h	3037h	[7:0]		Fixed to "00h"	00h	00h	
38h	3038h	0	WINPV [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
39h	3039h	0				00h	
		1					
		2		MSB			
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
3Ah	303Ah	0	WINWV [10:0]	LSB In window cropping mode Cropping size designation (Vertical direction)	4C9h	C9h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Bh	303Bh	0				04h	
		1					
		2		MSB			
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
3Ch	303Ch	0	WINPH [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (horizontal position) Set to become the multiple of four	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Dh	303Dh	0		MSB			
		1					
		2					
		3		Fixed to "0"	0h	00h	
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
3Eh	303Eh	0	WINWH [10:0]	LSB In window cropping mode Cropping size designation (horizontal direction) Set to become the multiple of eight and plus four	79Ch	9Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Fh	303Fh	0		MSB			
		1					
		2					
		3		Fixed to "0"	0h	07h	
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		

40h	3040h	[7:0]		Fixed to "01h"	01h	01h	
41h	3041h	[7:0]		Fixed to "00h"	00h	00h	
42h	3042h	[7:0]		Fixed to "01h"	01h	01h	
43h	3043h	[7:0]		Fixed to "00h"	00h	00h	
44h	3044h	0	ODBIT	Number of output bit setting 0:10 bit, 1:12 bit Set to"1" in CSI-2 output mode	1h	E1h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	OPORTSEL [3:0]	Output system selection 6h: Parallel low-voltage LVDS DDR output Dh: Serial low-voltage LVDS 2 ch DDR output Eh: Serial low-voltage LVDS 4 ch DDR output / CSI-2 output Others: Setting prohibited	Eh		Immediately
		5					
		6					
		7					

45h	3045h	[7:0]		Fixed to "01h"	01h	01h	

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
46h	3046h	0		Fixed to "0"	0h	00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	XVSLNG [1:0]	XVS pulse width setting in master mode (Invalid in slave mode) 0: 1H, 1: 2H, 2: 4H, 3: 8H	0h		Immediately
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
47h	3047h	0		Fixed to "0"	0h	08h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "1"	1h		
		4	XHSLNG [1:0]	XHS pulse width setting in master mode (Invalid in slave mode) 0: Min. to 3: Max.	0h		Immediately
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
48h	3048h	[7:0]		Set to "33h"	13h	13h	Immediately
49h	3049h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0:Output High setting 2:VSYNC output Others: Setting prohibited	0h	00h	Immediately
		1					
		2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0:Output High setting 2:HSYNC output Others: Setting prohibited	0h		Immediately
		3					
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
4Ah to 5Bh	304Ah to 305Bh	[7:0] [7:0]		Do not rewrite			

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
5Ch	305Ch	[7:0]	INCKSEL1 [7:0]	The value is set according to INCK Setting	20h	20h	Immediately
5Dh	305Dh	[7:0]	INCKSEL2 [7:0]	The value is set according to INCK Setting	00h	00h	Immediately
5Eh	305Eh	[7:0]	INCKSEL3 [7:0]	The value is set according to INCK Setting	18h	18h	Immediately
5Fh	305Fh	[7:0]	INCKSEL4 [7:0]	The value is set according to INCK Setting	00h	00h	Immediately

60h	3060h	[7:0]		Fixed to "00h"	00h	00h	
61h	3061h	[7:0]		Fixed to "01h"	01h	01h	
62h	3062h	[7:0]		Fixed to "08h"	08h	08h	
63h	3063h	[7:0]	INCKSEL5 [7:0]	The value is set according to INCK Setting	E8h	E8h	Immediately

TENTATIVE

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
64h to A0h	3064h to 30A0h	[7:0] [7:0]		Do not rewrite			
A1h	30A1h	[7:0]		Do not rewrite	44h	44h	
A2h to FFh	30A2h to 30FFh	[7:0] [7:0]		Do not rewrite			

*1 There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.

*2 Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h and 05h. (In I^2C communication, the address 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FFh and 3300h to 33FFh should be available.)

TENTATIVE

(2) 4-wire serial communication: Chip ID = 03h / I²C communication: 31**h

Address		Setting value	Default value after reset
4-wire	I²C		
1Dh	311Dh	0Ah	08h
23h	3123h	0Fh	07h
26h	3126h	Do not rewrite	DFh
47h	3147h	87h	B4h
E0h	31E0h	Do not rewrite	01h
E1h	31E1h	9Eh	00h
E2h	31E2h	01h	00h
E5h	31E5h	05h	00h
E6h	31E6h	05h	00h
E7h	31E7h	3Ah	3Dh
E8h	31E8h	3Ah	3Dh
C5h	31C5h	Communication prohibited*2	
to	to		
D4h	31D4h		

*1 Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h and 05h. (In I²C communication, the address 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FF and 3300h to 33FFh should be available.)

*2 These registers are communication prohibited. Do not write and read.

TENTATIVE

(3) 4-wire serial communication: Chip ID = 04h / I²C communication: 32**h

Address		Setting value	Default value after reset
4-wire	I²C		
03h	3203h	C8h	CDh
07h	3207h	54h	4Bh
13h	3213h	16h	1Bh
15h	3215h	F6h	EDh
1Ah	321Ah	14h	19h
1Bh	321Bh	51h	A1h
29h	3229h	E7h	ECh
2Ah	322Ah	F0h	40h
2Bh	322Bh	10h	11h
31h	3231h	E7h	ECh
32h	3232h	F0h	40h
33h	3233h	10h	11h
3Ch	323Ch	E8h	EDh
3Dh	323Dh	70h	C0h
43h	3243h	08h	0Dh
44h	3244h	E1h	31h
45h	3245h	10h	11h
47h	3247h	E7h	ECh
48h	3248h	60h	D0h
49h	3249h	1Eh	1Dh
4Bh	324Bh	00h	05h
4Ch	324Ch	41h	91h
50h	3250h	30h	A0h
51h	3251h	0Ah	08h
52h	3252h	FFh	D4h
53h	3253h	FFh	20h
54h	3254h	FFh	1Dh
55h	3254h	02h	03h
57h	3257h	F0h	60h
5Dh	325Dh	EEh	F3h
5Eh	325Eh	A0h	F0h
60h	3060h	03h	00h
61h	3261h	61h	5Eh
66h	3266h	30h	00h
67h	3267h	05h	05h
75h	3275h	E7h	ECh
81h	3281h	EAh	EFh
82h	3282h	70h	C0h
85h	3285h	FFh	F6h
8Ah	328Ah	F0h	60h
8Dh	328Dh	B6h	BBh
8Eh	328Eh	40h	90h

Address		Setting value	Default value after reset
4-wire	I²C		
90h	3290h	42h	39h
91h	3291h	51h	C1h
92h	3292h	1Eh	1Dh
94h	3294h	C4h	C9h
95h	3295h	20h	70h
97h	3297h	50h	47h
98h	3298h	31h	A1h
99h	3299h	1Fh	1Eh
9Bh	329Bh	C0h	C5h
9Ch	329Ch	60h	B0h
9Eh	329Eh	4Ch	43h
9Fh	329Fh	71h	E1h
A0h	32A0h	1Fh	1Eh
A2h	32A2h	B6h	BBh
A3h	32A3h	C0h	10h
A4h	32A4h	0Bh	0Ch
A9h	32A9h	24h	29h
AAh	32AAh	41h	91h
B0h	32B0h	25h	2Ah
B1h	32B1h	51h	A1h
B7h	32B7h	1Ch	21h
B8h	32B8h	C1h	11h
B9h	32B9h	12h	13h
BEh	32BEh	1Dh	22h
BFh	32BFh	D1h	21h
C0h	32C0h	12h	13h
C2h	32C2h	A8h	ADh
C3h	32C3h	C0h	10h
C4h	32C4h	0Ah	0Bh
C5h	32C5h	1Eh	23h
C6h	32C6h	21h	71h
C9h	32C9h	B0h	B5h
CAh	32CAh	40h	90h
CCh	32CCh	26h	2Bh
CDh	32CDh	A1h	F1h

Address		Setting value	Default value after reset
4-wire	I²C		
D0h	32D0h	B6h	BBh
D1h	32D1h	C0h	10h
D2h	32D2h	0Bh	0Ch
D4h	32D4h	E2h	E7h
D5h	32D5h	40h	90h
D8h	32D8h	4Eh	45h
D9h	32D9h	A1h	11h
ECh	32ECh	F0h	60h

* Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h and 05h. (In I²C communication, the address 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FFh and 3300h to 33FFh should be available.)

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(4) 4-wire serial communication: Chip ID = 05h / I^{2}C communication: 33**h

The register setting of Chip ID = 05h is only for CSI-2 output mode. Therefore these registers need not be set in low-voltage LVDS output modes.

Address		bit	Register Name	Description	Default value after reset	Reflection timing	RW
4-wire	I^{2}C						
00h	3300h	[7:0]		Fixed to “11h”	11h		RW
01h	3301h	[7:0]		Fixed to “11h”	11h		RW
02h	3302h	[7:0]		Fixed to “00h”	00h		RW
03h	3303h	[3:0]		Fixed to “0h”	00h		RW
		[5:4]	REPETITION [1:0]	*Refer to “Readout Drive Modes” section.		V	RW
		[7:6]		Fixed to “0h”			RW
04h	3304h	[7:0]		Fixed to “00h”	00h		RW
05h	3305h	[1:0]	PHYSICAL_Lane_NUM [1:0]	Physically connect the Lane number 1: 2Lane, 3: 4Lane Other: Setting prohibited	03h	Immediately	RW
		[7:2]		Fixed to “0h”			RW
06h	3306h	[7:0]		Fixed to “00h”	00h		RW
07h	3307h	[7:0]		Fixed to “00h”	00h		RW
08h	3308h	[7:0]		Fixed to “00h”	00h		RW
09h	3309h	[7:0]		Fixed to “00h”	00h		RW
0Ah	330Ah	[7:0]		Fixed to “00h”	00h		RW
0Bh	330Bh	[7:0]		Fixed to “00h”	00h		RW
0Ch	330Ch	[7:0]		Fixed to “00h”	00h		RW
0Dh	330Dh	[7:0]		Fixed to “00h”	00h		RW
0Eh	330Eh	[7:0]		Fixed to “00h”	00h		RW
0Fh	330Fh	[7:0]		Fixed to “0Fh”	0Fh		RW
10h	3310h	[7:0]		Fixed to “20h”	20h		RW
11h	3311h	[7:0]		Fixed to “00h”	00h		RW
12h	3312h	[7:0]		Fixed to “00h”	10h		RW
13h	3313h	[7:0]		Fixed to “01h”	01h		RW
14h	3314h	[5:0]	OB_SIZE_V [5:0]	Vertical (V) direction OB width setting. *Refer to each operating setting.	08h	V	RW
		[7:6]					
15h	3315h	[5:0]	NULL0_SIZE_V [5:0]	Vertical (V) direction NULL0 width setting. *Refer to each operating setting.	01h	V	RW
		[7:6]					
16h	3316h	[5:0]	NULL1_SIZE_V [5:0]	Vertical (V) direction NULL1 width setting. *Refer to each operating setting.	04h	V	RW
		[7:6]					
17h	3317h	[5:0]	NULL2_SIZE_V [5:0]	Vertical (V) direction NULL2 width setting. *Refer to each operating setting.	04h	V	RW
		[7:6]					
18h	3318h	[7:0]	PIC_SIZE_V [7:0]	Vertical (V) direction effective pixel width setting. *Refer to each operating setting.	49h	V	RW
19h	3319h	[3:0]	PIC_SIZE_V [11:8]		04h		
		[7:4]		Fixed to “0h”	0h		RW
1Ah	331Ah	[7:0]		Fixed to “01h”.	01h		RW
1Bh	331Bh	[7:0]		Fixed to “00h”.	00h		RW
1Ch	331Ch	[7:0]		Fixed to “40h”	40h		RW
1Dh to 2Bh	331Dh to 332Bh	[7:0] to [7:0]		Do not rewrite			
2Ch	332Ch	[7:0]	THSEXIT [7:0]	Global Timing Setting *Refer to each operating modes	3Fh	V	RW
2Dh	332Dh	[7:0]	TCLKPRE [7:0]	Global Timing Setting *Refer to each operating modes	1Fh	V	RW
2Eh	332Eh	[7:0]	TLPXESC [7:0]	Global Timing Setting *Refer to each operating modes	03h	Immediately	RW
2Fh to 3Dh	332Fh to 333Dh	[7:0] to [7:0]		Do not rewrite			
3Eh	333Eh	[7:0]	CSI_DT_FMT [7:0]	LSB RAW10 : 0A0Ah RAW12 : 0C0Ch MSB	0Ch	V	RW
3Fh	333Fh	[7:0]	CSI_DT_FMT [15:8]		0Ch		

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Address		bit	Register Name	Description	Default value after reset	Reflection timing	RW
4-wire	I²C						
40h	3340h	[1:0]	CSI_Lane_MODE [1:0]	Lane number setting. 1: 2Lane, 3: 4Lane	03h	Immediately	RW
		[7:2]		Fixed to “00h”.			RW
41h	3341h	[7:0]	INCK_FREQ [7:0]	LSB Master Clock Frequency 1B00h : INCK = 27 MHz 3600h : INCK = 54 MHz 2520h : INCK = 37.125 MHz 4A40h : INCK = 74.25 MHz MSB	20h	Immediately	RW
42h	3342h	[7:0]	INCK_FREQ [15:8]		25h		
43h	3343h	[7:0]	TCLK_POST [7:0]	Global Timing Setting *Refer to each operating modes	67h	V	RW
44h	3344h	[7:0]	THS_PREPARE [7:0]	Global Timing Setting *Refer to each operating modes	17h	V	RW
45h	3345h	[7:0]	THS_ZERO_MIN [7:0]	Global Timing Setting *Refer to each operating modes	47h	V	RW
46h	3346h	[7:0]	THS_TRAIL [7:0]	Global Timing Setting *Refer to each operating modes	27h	V	RW
47h	3347h	[7:0]	TCLK_TRAIL_MIN [7:0]	Global Timing Setting *Refer to each operating modes	1Fh	V	RW
48h	3348h	[7:0]	TCLK_PREPARE [7:0]	Global Timing Setting *Refer to each operating modes	17h	V	RW
49h	3349h	[7:0]	TCLK_ZERO [7:0]	Global Timing Setting *Refer to each operating modes	77h	V	RW
4Ah	334Ah	[7:0]	TLPX [7:0]	Global Timing Setting *Refer to each operating modes	27h	V	RW
4Bh to 4Dh	334Bh to 334Dh			Do not rewrite			
4Eh	334Eh	[7:0]	INCK_FREQ2 [7:0]	LSB 13Dh : INCK = 27 MHz 1B4h : INCK = 37.125 MHz 279h : INCK = 54 MHz 367h : INCK = 74.25 MHz MSB	67h	Immediately	RW
4Fh	334Fh	[2:0]	INCK_FREQ2 [10:8]		03h		
		[7:3]		Fixed to “00h”			RW
50h to 80h	3350h to 3380h			Do not rewrite			
81h	3381h	[0]	REG_HOLD_OUTPUT	Readout Register Hold enable Register: REGHOLD Address[*4]: 3001h	00h	—	RODynamic
		[7:1]		Fixed to “0h”			ROstatic
82h	3382h	[7:0]		Fixed to “00h”	00h		ROstatic
83h	3383h	[7:0]		Fixed to “00h”	00h		ROstatic
84h	3384h	[7:0]	MODEL_ID [7:0]	Sensor type name 0185h = IMX185	85h	—	ROstatic
85h	3385h	[7:0]	MODEL_ID [15:8]		01h		
86h	3386h	[7:0]		Fixed to “01h”	01h		ROstatic
87h	3387h	[7:0]		Fixed to “01h”	01h	—	ROstatic
88h	3388h	[7:0]	FRM_CNT [7:0]	Readout counted frame number. Count range: 1 to 254d In standby: 0d	00h	—	RODynamic
89h	3389h	[7:0]					
8Ah	338Ah	[7:0]	DT_PEDESTAL [7:0]	Readout Black level setting. Register: BLKLEVEL Address[*4]: 0x300A-300B	F0h	—	RODynamic
8Bh	338Bh	[7:0]	DT_PEDESTAL [15:8]		00h		

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Address		bit	Register Name	Description	Default value after reset	Reflection timing	RW
4-wire	I²C						
8Ch	338Ch	[7:0]	CCP_DT_FMT [7:0]	Readout CSI-2 Output data format Register: CSI_DT_FMT Address*4: 0x333E-333F	0Ch	—	RODynamic
8Dh	338Dh	[7:0]	CCP_DT_FMT [15:8]		0Ch		
8Eh	338Eh	[7:0]		Fixed to “00h”	00h		ROStatic
8Fh	338Fh	[7:0]		Fixed to “00h”	00h		ROStatic
90h	3390h	[7:0]		Fixed to “00h”	00h		ROStatic
91h	3391h	[7:0]		Fixed to “F0h”	F0h		ROStatic
92h	3392h	[7:0]		Fixed to “00h”	00h		ROStatic
93h	3393h	[7:0]		Fixed to “01h”	01h		ROStatic
94h	3394h	[7:0]		Fixed to “00h”	00h		ROStatic
95h	3395h	[7:0]		Fixed to “00h”	00h		ROStatic
96h	3396h	[7:0]		Fixed to “00h”	00h		ROStatic
97h	3397h	[7:0]		Fixed to “00h”	00h		ROStatic
98h	3398h	[7:0]		Fixed to “F0h”	F0h		ROStatic
99h	3399h	[7:0]		Fixed to “00h”	00h		ROStatic
9Ah	339Ah	[7:0]		Fixed to “01h”	01h		ROStatic
9Bh	339Bh	[7:0]		Fixed to “00h”	00h		ROStatic
9Ch	339Ch	[7:0]		Fixed to “F0h”	F0h		ROStatic
9Dh	339Dh	[7:0]		Fixed to “00h”	00h		ROStatic
9Eh	339Eh	[7:0]	GAIN_GLOBAL [7:0]	Readout gain setting value. Register: GAIN Address*4: 0x3014	00h	—	RODynamic
9Fh	339Fh	[7:0]	GAIN_GLOBAL [15:8]		00h		
A0h	33A0h	[7:0]	SHUTTER_TIME1 [7:0]	Readout SHS1 Setting value Register: SHS1 Address*4: 0x3020-3022	00h	—	RODynamic
A1h	33A1h	[7:0]	SHUTTER_TIME1 [15:8]		00h		
A2h	33A2h	[7:0]	SHUTTER_TIME1 [23:16]		00h		
A3h	33A3h	[7:0]		Fixed to “00h”.	00h		ROStatic
A4h	33A4h	[7:0]		Fixed to “00h”.	00h		ROStatic
A5h	33A5h	[7:0]		Fixed to “00h”.	00h		ROStatic
A6h	33A6h	[7:0]		Fixed to “00h”.	00h		ROStatic
A7h	33A7h	[7:0]		Fixed to “00h”.	00h		ROStatic
A8h	33A8h	[7:0]		Fixed to “00h”.	00h		ROStatic
A9h	33A9h	[7:0]		Fixed to “00h”.	00h		ROStatic
AAh	33AAh	[7:0]		Fixed to “00h”.	00h		ROStatic
ABh	33ABh	[7:0]		Fixed to “00h”.	00h		ROStatic
ACh	33ACh	[7:0]		Fixed to “00h”.	00h		ROStatic
ADh	33ADh	[7:0]		Fixed to “00h”.	00h		ROStatic
AEh	33AEh	[7:0]		Fixed to “00h”.	00h		ROStatic
AFh	33AFh	[7:0]		Fixed to “00h”.	00h		ROStatic
B0h	33B0h	[7:0]		Fixed to “00h”.	00h		ROStatic
B1h	33B1h	[7:0]		Fixed to “00h”.	00h		ROStatic
B2h	33B2h	[7:0]		Fixed to “00h”.	00h		ROStatic
B3h	33B3h	[7:0]		Fixed to “00h”.	00h		ROStatic
B4h	33B4h	[7:0]	FRM_LENGTH [7:0]	In master mode Readout XHS numbers of 1 frame period. Register: VMAX Address*4:0x3018-301A	65h	—	RODynamic
B5h	33B5h	[7:0]	FRM_LENGTH [15:8]		04h		
B6h	33B6h	[7:0]	FRM_LENGTH [23:16]		00h		
B7h	33B7h	[7:0]	LINE_LENGTH [7:0]	In master mode Readout clock number of 1 H period. Register: HMAX Address*4:0x301B-301C	98h	—	RODynamic
B8h	33B8h	[7:0]	LINE_LENGTH [15:8]		08h		
B9h	33B9h	[7:0]	X_ADD_STA [7:0]	In Window cropping mode Readout X-direction starting address coodinates Register: WINPH Address*4:0x303C-303D	00h	—	RODynamic
BAh	33BAh	[7:0]	X_ADD_STA [15:8]		00h		
BBh	33BBh	[7:0]	Y_ADD_STA [7:0]	In Window cropping mode Readout Y-direction starting address coodinates Register: WINPV Address*4:0x3038-3039	00h	—	RODynamic
BCh	33BCh	[7:0]	Y_ADD_STA [15:8]		00h		
BDh	33BDh	[7:0]	X_ADD_END [7:0]	In Window cropping mode Readout X-direction end address coordinates	9Bh	—	RODynamic
BEh	33BEh	[7:0]	X_ADD_END [15:8]		07h		

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Address		bit	Register Name	Description	Default value after reset	Reflection timing	RW
4-wire	I²C						
BFh	33BFh	[7:0]	Y_ADD_END [7:0]	In Window cropping mode Readout Y-direction end address coordinates.	C8h	—	RODynamic
C0h	33C0h	[7:0]	Y_ADD_END [15:8]		04h		
C1h	33C1h	[7:0]	X_OUT_SIZE [7:0]	In Window cropping mode Readout X-direction extraction width. Register: WINWH Address*4:0x303E-303F	9Ch	—	RODynamic
C2h	33C2h	[7:0]	X_OUT_SIZE [15:8]		07h		
C3h	33C3h	[7:0]	Y_OUT_SIZE [7:0]	In Window cropping mode Readout Y-direction extraction width. Register: WINWV Address*4:0x303A-303B	C9h	—	RODynamic
C4h	33C4h	[7:0]	Y_OUT_SIZE [15:8]		04h		
C5h	33C5h	[1:0]	SCALE_MODE [1:0]	Readout Scaling mode 00h: Normal, 01h:V Inverted 10h: H Inverted, 11h: V&H Inverted	00h	—	RODynamic
		[7:2]		Fixed to “00h”			ROstatic
C6h	33C6h	[7:0]		Fixed to “00h”	00h		ROstatic
C7h	33C7h	[7:0]		Fixed to “00h”	00h		ROstatic
C8h	33C8h	[7:0]		Fixed to “00h”	00h		ROstatic
C9h	33C9h	[7:0]		Fixed to “00h”	00h		ROstatic
CAh	33CAh	[7:0]		Fixed to “00h”	00h		ROstatic
CBh	33CBh	[7:0]		Fixed to “9Bh”	9Bh		ROstatic
CCh	33CCh	[7:0]		Fixed to “07h”	07h		ROstatic
CDh	33CDh	[7:0]		Fixed to “F0h”	F0h		ROstatic
CEh	33CEh	[7:0]		Fixed to “04h”	04h		ROstatic
CFh	33CFh	[7:0]		Fixed to “7Ch”	7Ch		ROstatic
D0h	33D0h	[7:0]		Fixed to “01h”	01h		ROstatic
D1h	33D1h	[7:0]		Fixed to “38h”	38h		ROstatic
D2h	33D2h	[7:0]		Fixed to “01h”	01h		ROstatic
D3h	33D3h	[7:0]		Fixed to “9Ch”	9Ch		ROstatic
D4h	33D4h	[7:0]		Fixed to “07h”	07h		ROstatic
D5h	33D5h	[7:0]		Fixed to “C9h”	C9h		ROstatic
D6h	33D6h	[7:0]		Fixed to “04h”	04h		ROstatic
D7h	33D7h	[7:0]		Fixed to “01h”	01h		ROstatic
D8h	33D8h	[1:0]	Lane_MODE [1:0]	Readout Lane setting value Register: CSI_Lane_MODE Address*4: 0x3340h	03h	—	RODynamic
		[7:2]		Fixed to “00h”			ROstatic
D9h	33D9h	[7:0]		Fixed to “00h”	00h	—	ROstatic
DAh	33DAh	[7:0]		Fixed to “00h”	00h	—	ROstatic
DBh	33DBh	[7:0]	Y_OB_ADD_END [7:0]	In Window cropping mode Readout Y-direction end address coordinates of OB.	0Bh	—	RODynamic
DCh	33DCh	[7:0]	Y_OB_ADD_END [15:8]		00h		
DDh	33DDh	[7:0]	Y_OB_OUT_SIZE [7:0]	In Window cropping mode Readout Y-direction extraction width of OB.	0Ch	—	RODynamic
DEh	33DEh	[7:0]	Y_OB_OUT_SIZE [15:8]		00h		
DFh to FFh	33DFh to 33FFh			Do not rewrite			

*1 There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, set them in sensor standby state.

*2 Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h and 05h. (In I²C communication, the address 3000h to 30FFh, 3100h to 31FFh, 3200h to 32FFh, and 3300h to 33FFh should be available.)

*3 The register written as “RW” is a read and a write register. The register written as “ROstatic” is a read only register that the fixed value is output and also output to an embedded data line. The register written as “RODynamic” is a read only register that the sensor setting value is output and also output to an embedded data line.

*4 This is an address for I²C communication. In 4-wire serial communication, each address corresponds to the register when Chip ID = 02h.

Readout Drive Modes

The table below lists the operating modes available with this sensor.

List of Operation Modes and Output Rates for Low-voltage LVDS Parallel Output

Operating mode	INCK [MHz]	Frame rate [fps]	Data rate [Mpix/s]	Low -voltage LVDS Parallel	ADC (bit)	Bit width (bit)	Number of recording pixels		Total number of pixels		Number of output vertical lines and horizontal pixels		Number of INCK in 1H			
							H	V	H	V	H	V	37.125 MHz	27 MHz	74.25 MHz	54 MHz
All-pixel scan mode	37.125 /27 /74.25 /54	25.00	74.25	○	10/12	10/12	1920	1200	1952	1241	2250	1320	1125	818.18	2250	1636.4
		30.00	148.5	○	10/12	10/12					3750		937.5	681.82	1875	1363.6
		50.00	148.5	○	10/12	10/12					2250		562.5	409.09	1125	818.18
		60.00	297.0	○	10	10					3750		468.75	340.91	937.5	681.82
		100.00	297.0	○	10	10					2250		281.25	204.55	562.5	409.1
Horizontal / vertical 2/2-line bining readout mode	37.125 /27 /74.25 /54	25.00	18.563	○	10	12	960	600	976	621	1125	660	2250	1636.4	4500	3272.7
		30.00	37.125	○	10	12					1875		1875	1363.6	3750	2727.3
		50.00	37.125	○	10	12					1125		1125	818.18	2250	1636.4
		60.00	74.25	○	10	12					1875		937.5	681.82	1875	1636.3
		100.00	74.25	○	10	12					1125		562.5	409.09	1125	818.18
1080p-HD mode	37.125 /27 /74.25 /54	30.00	74.25	○	10/12	10/12	1920	1080	1952	1115	2200	1125	1100	800	2200	1600
		60.00	148.5	○	10/12	10/12							550	400	1100	800
		120.00	297	○	10	10							275	200	550	400
720p-HD mode	37.125 /27 /74.25 /54	30.00	37.125	○	10/12	10/12	1280	720	1312	739	1650	750	1650	1200	3300	2400
		60.00	74.25	○	10/12	10/12							825	600	1650	1200
		120.00	148.5	○	10	10							412.5	300	825	600

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List of Operation Modes and Output Rates for Low-voltage LVDS Serial Output

Operating mode	INCK [MHz]	Frame rate [fps]	Data rate [Mpix/s]	Low-voltage LVDS Serial 2 ch	Low-voltage LVDS Serial 4 ch	ADC (bit)	Bit width (bit)	Number of recording pixels H	Number of recording pixels V	Total number of pixels H	Total number of pixels V	Number of output vertical lines and horizontal pixels H	Number of output vertical lines and horizontal pixels V	Number of INCK in 1H 37.125 MHz	Number of INCK in 1H 27 MHz	Number of INCK in 1H 74.25 MHz	Number of INCK in 1H 54 MHz
All-pixel scan mode	37.125 /27 /74.25 /54	25.00	445.5	○	N/A	10	10	1920	1200	1952	1241	2700	1320	1125	818.18	2250	1636.4
			222.75	N/A	○	10	10					2700		1125	818.18	2250	1636.4
			445.5	○	N/A	12	12					2250		1125	818.18	2250	1636.4
			222.75	N/A	○	12	12					2250		1125	818.18	2250	1636.4
		30.00	445.5	N/A	○	10	10					4500		937.5	681.82	1875	1363.6
			445.5	N/A	○	12	12					3750		937.5	681.82	1875	1363.6
		50.00	445.5	N/A	○	10	10					2700		562.5	409.09	1125	818.18
			445.5	N/A	○	12	12					2250		562.5	409.09	1125	818.18
Horizontal / vertical 2/2-line bining readout mode	37.125 /27 /74.25 /54	25.00	111.375	○	N/A	10	12	960	600	976	621	1125	660	2250	1636.4	4500	3272.7
			55.688	N/A	○	10	12					1125		2250	1636.4	4500	3272.7
		30.00	111.375	N/A	○	10	12					1875		1875	1363.6	3750	2727.3
		50.00	111.375	N/A	○	10	12					1125		1125	818.18	2250	1636.4
1080p-HD mode	37.125 /27 /74.25 /54	30.00	445.5	○	N/A	10	10	1920	1080	1952	1115	2640	1125	1100	800	2200	1600
			222.75	N/A	○	10	10							1100	800	2200	1600
		30.00	445.5	○	N/A	12	12							1100	800	2200	1600
			222.75	N/A	○	12	12							1100	800	2200	1600
		60.00	445.5	N/A	○	10	10							550	400	1100	800
			445.5	N/A	○	12	12							550	400	1100	800
720p-HD mode	37.125 /27 /74.25 /54	30.00	222.75	○	N/A	10	10	1280	720	1312	739	1980	750	1650	1200	3300	2400
			111.375	N/A	○	10	10					1980		1650	1200	3300	2400
			222.75	○	N/A	12	12					1650		1650	1200	3300	2400
			111.375	N/A	○	12	12					1650		1650	1200	3300	2400
		60.00	445.5	○	N/A	10	10					1980		825	600	1650	1200
			222.75	N/A	○	10	10					1980		825	600	1650	1200
			445.5	○	N/A	12	12					1650		825	600	1650	1200
			222.75	N/A	○	12	12					1650		825	600	1650	1200
		120.00	445.5	N/A	○	10	10					1980		412.5	300	825	600

* N/A: Mode not supported

TENTATIVE

List of Operation Modes and Output Rates for CSI-2 Serial Output

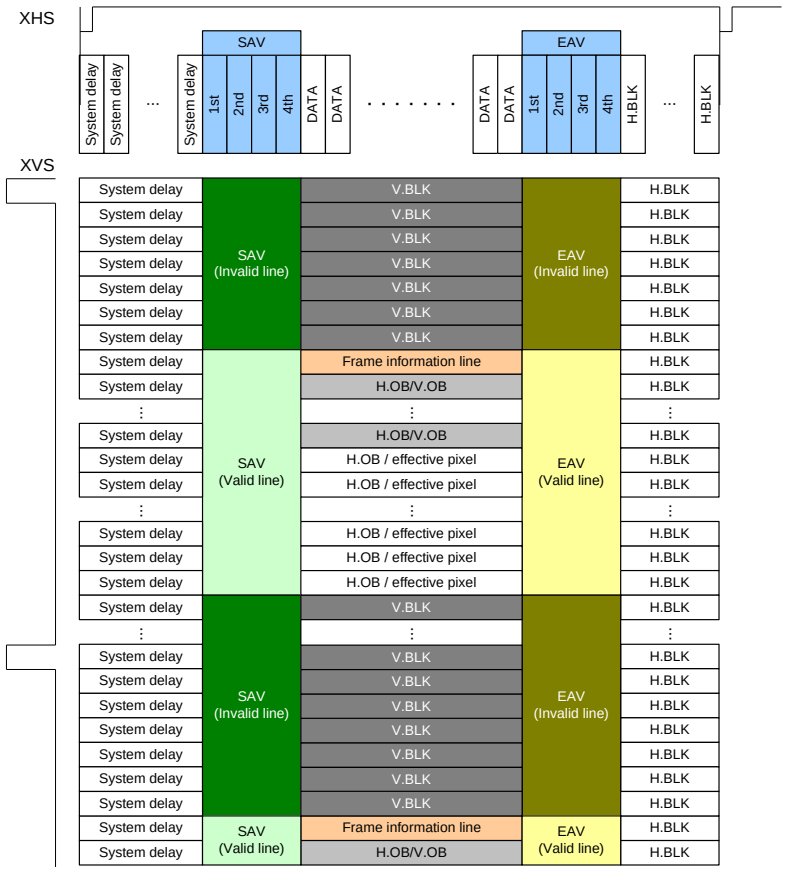
Operating mode	INCK [MHz]	Frame rate [fps]	Data rate [Mpix/s]	CSI-2 Serial Output		ADC (bit)	Output Format	Number of recording pixels		Total number of pixels		Number of output vertical lines and horizontal pixels		Number of INCK in 1H			
				2 Lane	4 Lane			H	V	H	V	H	V	37.125 MHz	27 MHz	74.25 MHz	54 MHz
All-pixel scan mode	37.125 /27 /74.25 /54	25.00	445.5	○	N/A	10	RAW 10	1920	1200	1952	1241	2700	1320	1125	818.18	2250	1636.4
			222.75	N/A	○	10	RAW 10					2700		1125	818.18	2250	1636.4
			445.5	○	N/A	12	RAW 12					2250		1125	818.18	2250	1636.4
			222.75	N/A	○	12	RAW 12					2250		1125	818.18	2250	1636.4
		30.00	445.5	N/A	○	10	RAW 10					4500		937.5	681.82	1875	1363.6
			445.5	N/A	○	12	RAW 12					3750		937.5	681.82	1875	1363.6
		50.00	445.5	N/A	○	10	RAW 10					2700		562.5	409.09	1125	818.18
			445.5	N/A	○	12	RAW 12					2250		562.5	409.09	1125	818.18
Horizontal / vertical 2/2-line bining readout mode	37.125 /27 /74.25 /54	22.00	111.375	○	N/A	10	RAW 12	960	600	976	621	1250	675	2500	1818.2	5000	3636.4
			111.375	N/A	○	10	RAW 12					1250		2500	1818.2	5000	3636.4
		30.00	111.375	N/A	○	10	RAW 12					1875	660	1875	1363.6	3750	2727.3
		44.00	111.375	N/A	○	10	RAW 12					1250	675	1250	909.09	2500	18182
1080p-HD mode	37.125 /27 /74.25 /54	30.00	445.5	○	N/A	10	RAW 10	1920	1080	1952	1115	2640	1125	1100	800	2200	1600
			222.75	N/A	○	10	RAW 10					2640		1100	800	2200	1600
			445.5	○	N/A	12	RAW 12					2200		1100	800	2200	1600
			222.75	N/A	○	12	RAW 12					2200		1100	800	2200	1600
		60.00	445.5	N/A	○	10	RAW 10					2640		550	400	1100	800
			445.5	N/A	○	12	RAW 12					2200		550	400	1100	800
720p-HD mode	37.125 /27 /74.25 /54	30.00	222.75	○	N/A	10	RAW 10	1280	720	1312	739	1980	750	1650	1200	3300	2400
			111.375	N/A	○	10	RAW 10					1980		1650	1200	3300	2400
			222.75	○	N/A	12	RAW 12					1650		1650	1200	3300	2400
			111.375	N/A	○	12	RAW 12					1650		1650	1200	3300	2400
		60.00	445.5	○	N/A	10	RAW 10					1980		825	600	1650	1200
			222.75	N/A	○	10	RAW 10					1980		825	600	1650	1200
			445.5	○	N/A	12	RAW 12					1650		825	600	1650	1200
			222.75	N/A	○	12	RAW 12					1650		825	600	1650	1200
		120.00	222.75	N/A	○	10	RAW 10					1980		412.5	300	825	600

* N/A: Mode not supported

TENTATIVE

Sync Code

The sync code is added just before and after “dummy signal + OB signal + effective pixel data”. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd.
(BLK: Blanking period)



Sync Code Output Timing

List of Sync Code

Sync code	1st code		2nd code		3rd code		4th code	
	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit
SAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

(Note 1) 10 bit is the value output to the DOP/M [11:2] when the register ODBIT = 0 in parallel output.

(Note 2) 12 bit is the value output to the DOA/B [11:0] when the register ODBIT = 1 in parallel output.

(Note 3) They are output to each channel seriously in MSB first when low-voltage LVDS serial.
For details, see the item of "Signal output" and "Output pin setting".

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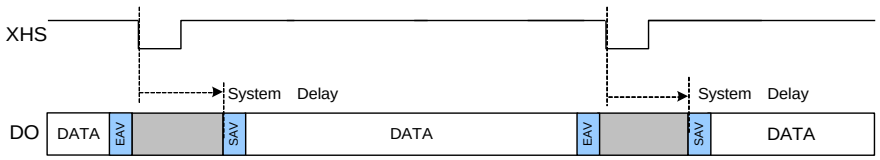
Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



TENTATIVE

Image Data Output Format

Frame Format

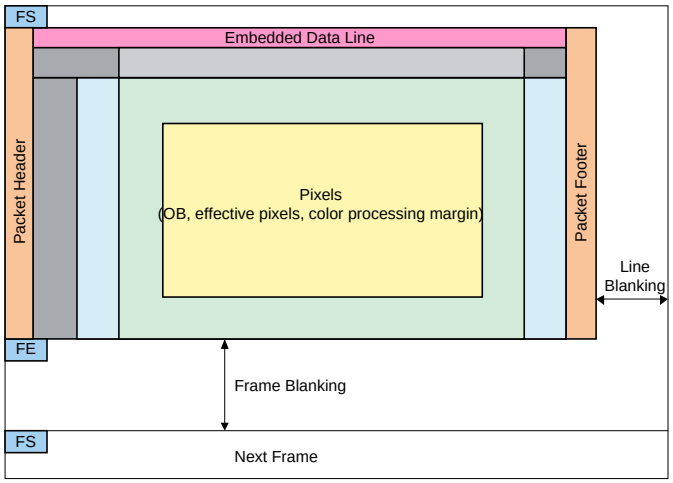
Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

Data Type

Header[5:0]	Name	Register setting (I^2C)	Description
6'h00	Frame Start Code	N.A	FS
6'h01	Frame End Code	N.A	FE
6'h10	Null	N.A	Invalid data
6'h12	Embedded Data	N.A	Embedded data
6'h2B	RAW10	Address : 0x333E,0x333F CCP_DT_FMT[15:0]	0A0Ah
6'h2C	RAW12		0C0Ch
6'h37	OB Data	N.A	Vertical OB line data

Frame Structure

The figure below shows the image frame structure.



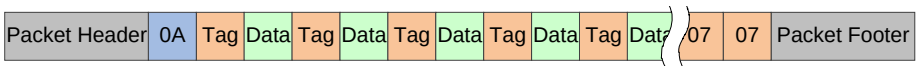
Frame Structure of 4 Lane / 2 Lane

TENTATIVE

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

Embedded Data Format



RAW10 Output

RAW12 Output

The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
aah	CCI Register Index MSB[15:8]
a5h	CCI Register Index LSB[7:0]
5ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
ffh	Illegal Tag. If found treat as end of Data.

TENTATIVE

Specific output examples are shown below. (4-wire: Chip ID = 05h)

pixel	Address [HEX] 4-wire	Address [HEX] I²C	Data Byte Description	Value
1	—	—	Data format	0x0A
2			CCI Register Index MSB [15:8]	0xAA
3				0x33
4			CCI Register Index LSB [7:0]	0xA5
5				0x80
6			Fixed to 0x00	0x5A
7	80	3380		0x00
8			REG_HOLD Hold V-reflection timing registerenable	0x5A
9	81	3381		0x00
10			Fixed to 0x00	0x5A
11	82	3382		0x00
12			Fixed to 0x00	0x5A
13	83	3383		0x00
14			MODEL_ID 0x0185 = IMX185	0x5A
15	84	3384		0x85
16				0x5A
17	85	3385		0x01
18			Fixed to 0x01	0x5A
19	86	3386		0x01
20			Fixed to 0x01	0x5A
21	87	3387		0x01
22			FRM_CNT Frame count (1 to 254d)	0x5A
23	88	3388		[7:0]
24				
25	89	3389		
26			DT_PEDESTAL Black level value ADC = 10 bit : 0x3C ADC = 12 bit : 0xF0	0x5A
27	8A	338A		[7:0]
28				0x5A
29	8B	338B		[15:8]
30			CCP_DT_FMT RAW10 : 0x0A0A RAW12 : 0x0C0C	0x5A
31	8C	338C		[7:0]
32				0x5A
33	8D	338D		[15:8]
34			Fixed to 0x00	0x5A
35	8E	338E		0x00
36			Fixed to 0x00	0x5A
37	8F	338F		0x00
38			Fixed to 0x00	0x5A
39	90	3390		0x00
40			Fixed to 0xF0	0x5A
41	91	3391		0xF0
42			Fixed to 0x00	0x5A
43	92	3392		0x00

pixel	Address [HEX] 4-wire	Address [HEX] I²C	Data Byte Description	Value
44			Fixed to 0x01	0x5A
45	93	3393		0x01
46			Fixed to 0x00	0x5A
47	94	3394		0x00
48			Fixed to 0x00	0x5A
49	95	3395		0x00
50			Fixed to 0x00	0x5A
51	96	3396		0x00
52			Fixed to 0x00	0x5A
53	97	3397		0x00
54			Fixed to 0xF0	0x5A
55	98	3398		0xF0
56			Fixed to 0x00	0x5A
57	99	3399		0x00
58			Fixed to 0x01	0x5A
59	9A	339A		0x01
60			Fixed to 0x00	0x5A
61	9B	339B		0x00
62			Fixed to 0xF0	0x5A
63	9C	339C		0xF0
64			Fixed to 0x00	0x5A
65	9D	339D		0x00
66			GAIN_GLOBAL Gain setting value.	0x5A
67	9E	339E		[7:0]
68				0x5A
69	9F	339F		[15:8]
70			SHUTTER_TIME1 SHS1 setting value.	0x5A
71	A0	33A0		[7:0]
72				0x5A
73	A1	33A1		[15:8]
74				0x5A
75	A2	33A2		[23:16]
76			Fixed to 0x00	0x5A
77	A3	33A3		0x00
78			Fixed to 0x00	0x5A
79	A4	33A4		0x00
80			Fixed to 0x00	0x5A
81	A5	33A5		0x00
82			Fixed to 0x00	0x5A
83	A6	33A6		0x00
84			Fixed to 0x00	0x5A
85	A7	33A7		0x00
86			Fixed to 0x00	0x5A
87	A8	33A8		0x00

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pixel	Address [HEX] 4-wire	Address [HEX] I²C	Data Byte Description	Value
88			Fixed to 0x00	0x5A
89	A9	33A9		0x00
90			Fixed to 0x00	0x5A
91	AA	33AA		0x00
92			Fixed to 0x00	0x5A
93	AB	33AB		0x00
94			Fixed to 0x00	0x5A
95	AC	33AC		0x00
96			Fixed to 0x00	0x5A
97	AD	33AD		0x00
98			Fixed to 0x00	0x5A
99	AE	33AE		0x00
100			Fixed to 0x00	0x5A
101	AF	33AF		0x00
102			Fixed to 0x00	0x5A
103	B0	33B0		0x00
104			Fixed to 0x00	0x5A
105	B1	33B1		0x00
106			Fixed to 0x00	0x5A
107	B2	33B2		0x00
108			Fixed to 0x00	0x5A
109	B3	33B3		0x00
110			FRM_LENGTH VMAX setting value.	0x5A
111	B4	33B4		[7:0]
112				0x5A
113	B5	33B5		[15:8]
114				0x5A
115	B6	33B6		[23:16]
116			LINE_LENGTH HMAX setting value.	0x5A
117	B7	33B7		[7:0]
118				0x5A
119	B8	33B8		[15:8]
120			X_ADD_STA WINPH setting value.	0x5A
121	B9	33B9		[7:0]
122				0x5A
123	BA	33BA		[15:8]
124			Y_ADD_STA WINPV setting value.	0x5A
125	BB	33BB		[7:0]
126				0x5A
127	BC	33BC		[15:8]
128			X_ADD_END In window cropping, X-direction end coodinates.	0x5A
129	BD	33BD		[7:0]
130				0x5A
131	BE	33BE		[15:8]
132			Y_ADD_END In window cropping, Y-direction end coodinates.	0x5A
133	BF	33BF		[7:0]
134				0x5A
135	C0	33C0		[15:8]

pixel	Address [HEX] 4-wire	Address [HEX] I²C	Data Byte Description	Value
136			X_OUT_SIZE WINWH setting value.	0x5A
137	C1	33C1		[7:0]
138				0x5A
139	C2	33C2		[15:8]
140			Y_OUT_SIZE WINWV setting value.	0x5A
141	C3	33C3		[7:0]
142				0x5A
143	C4	33C4		[15:8]
144			SCALE_MODE 00h: Normal, 01h: Inverted	0x5A
145	C5	33C5		[7:0]
146			Fixed to 0x00	0x5A
147	C6	33C6		0x00
148			Fixed to 0x00	0x5A
149	C7	33C7		0x00
150			Fixed to 0x00	0x5A
151	C8	33C8		0x00
152			Fixed to 0x00	0x5A
153	C9	33C9		0x00
154			Fixed to 0x00	0x5A
155	CA	33CA		0x00
156			Fixed to 0x9B	0x5A
157	CB	33CB		0x9B
158			Fixed to 0x07	0x5A
159	CC	33CC		0x07
160			Fixed to 0xF0	0x5A
161	CD	33CD		0xF0
162			Fixed to 0x04	0x5A
163	CE	33CE		0x04
164			Fixed to 0x7C	0x5A
165	CF	33CF		0x7C
166			Fixed to 0x01	0x5A
167	D0	33D0		0x01
168			Fixed to 0x38	0x5A
169	D1	33D1		0x38
170			Fixed to 0x01	0x5A
171	D2	33D2		0x01
172			Fixed to 0x9C	0x5A
173	D3	33D3		0x9C
174			Fixed to 0x07	0x5A
175	D4	33D4		0x07
176			Fixed to 0xC9	0x5A
177	D5	33D5		0xC9
178			Fixed to 0x04	0x5A
179	D6	33D6		0x04
180			Fixed to 0x01	0x5A
181	D7	33D7		0x01
182			Lane_MODE 1:2 Lane 3:4 Lane	0x5A
183	D8	33D8		[7:0]

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pixel	Address [HEX]		Data Byte Description	Value
	4-wire	I^2C		
184			Fixed to 0x00	0x5A
185	D9	33D9		0x00
186			Fixed to 0x00	0x5A
187	DA	33DA		0x00
188			Y_OB_ADD_END In window cropping, Y-direction end coodinates of OB.	0x5A
189	DB	33DB		[7:0]
190				0x5A
191	DC	33DC		[15:8]
192			Y_OB_OUT_SIZE In window cropping, Y-direction extraction width of OB.	0x5A
193	DD	33DD		[7:0]
194				0x5A
195	DE	33DE		[15:8]
196			Fixed to 0x00	0x5A
197	DF	33DF		0x00
198			Fixed to 0x00	0x5A
199	E0	33E0		0x00
200			Fixed to 0x0B	0x5A
201	E1	33E1		0x0B
202			Fixed to 0x00	0x5A
203	E2	33E2		0x00
204			Fixed to 0x06	0x5A
205	E3	33E3		0x06
206			Fixed to 0x00	0x5A
207	E4	33E4		0x00
208			Fixed to 0x10	0x5A
209	E5	33E5		0x10
210			Fixed to 0x00	0x5A
211	E6	33E6		0x00
212			End of data	0x07
213				0x07
214				0x07

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Image Data Output Format

All-pixel Scan Mode

All the pixel signals of sensor are read.

Register List of All-pixel Mode Setting (Low-voltage LVDS Parallel / Serial output)

Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
		ChipID ; 02h				
ADBIT	—	05h	[0]	1h	See below and the next section	10 bit or 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	All-pixel scan mode
WINMODE [3:0]	—	07h	[5:4]	1h	0h	WUXGA mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below and the next section	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	See below and the next section	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h	[7:0]			
	VMAX [16]	1Ah	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	See below and the next section	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch	[7:0]			
ODBIT	—	44h	[0]	1h	See below and the next section	10 bit or 12 bit
OPORTSEL [3:0]	—	44h	[7:4]	Eh	See below and the next section	Low-voltage LVDS Parallel / Low-voltage LVDS Serial /CSI-2 Serial output selection
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting	
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h		
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h		
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h		
INCKSEL5 [7:0]	—	63h	[7:0]	E8h		

Detailed Register List of All-pixel Mode Setting (Low-voltage Parallel Output)

NCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage Parallel Output	25.00	10 bit	2h	0528h	1320d	1194h	4500d	0h	0h	6h
			12 bit	2h					1h	1h	
		30.00	10 bit	1h			0EA6h	3750d	0h	0h	
			12 bit	1h					1h	1h	
		50.00	10 bit	1h			08CAh	2250d	0h	0h	
			12 bit	1h					1h	1h	
		60.00	10 bit	0h			0753h	1875d	0h	0h	
		100.00	10 bit	0h			0465h	1125d	0h	0h	

TENTATIVE

Detailed Register List of All-pixel Mode Setting (Low-voltage Serial Output)

INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage serial 2 ch	25.00	10 bit	2h	0528h	1320d	08CAh	2250d	0h	0h	Dh
			12 bit	2h					1h	1h	
	Low -voltage serial 4 ch	25.00	10 bit	2h					0h	0h	Eh
			12 bit	2h					1h	1h	
		30.00	10 bit	1h			0753h	1875d	0h	0h	
			12 bit	1h					1h	1h	
		50.00	10 bit	1h			0465h	1125d	0h	0h	
			12 bit	1h					1h	1h	

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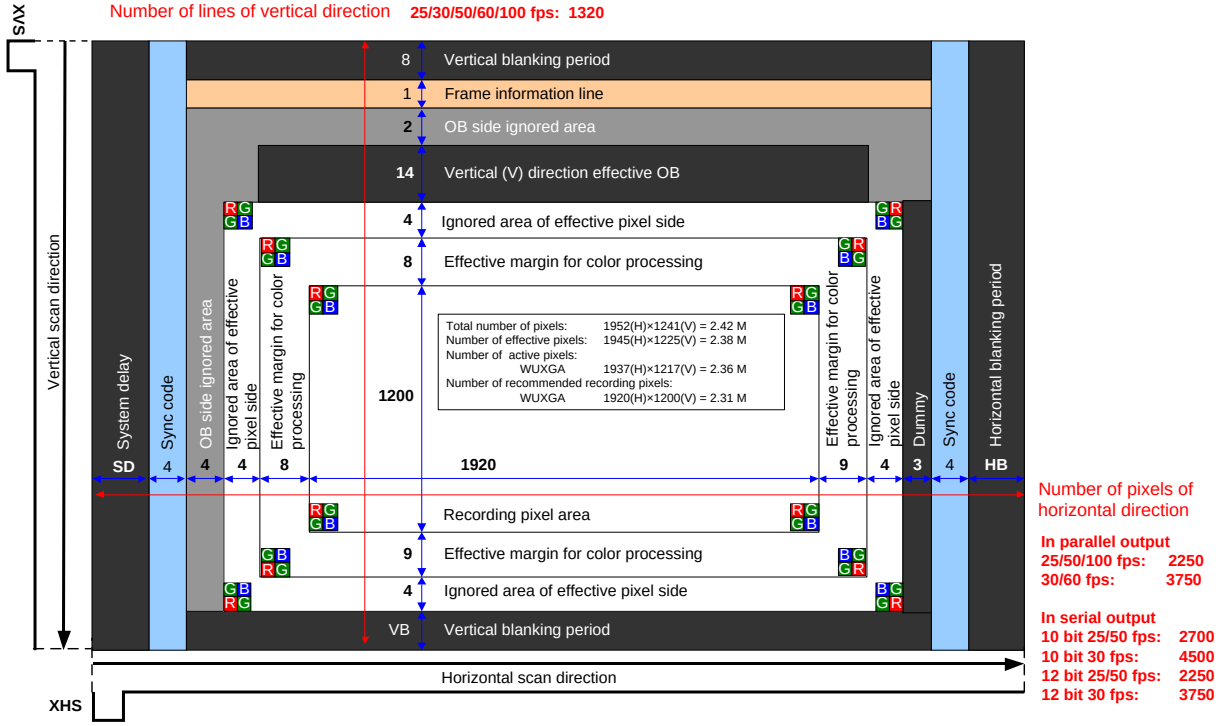
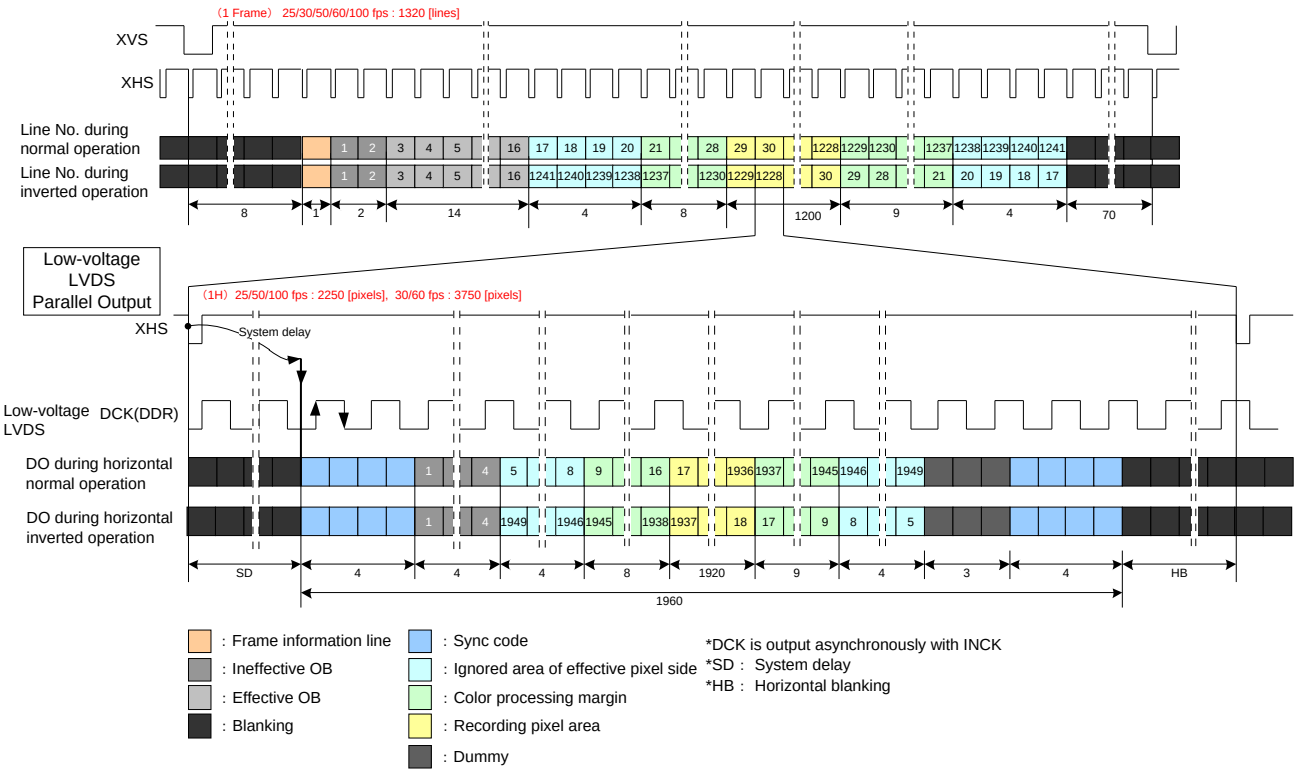
Detailed Register List of All-pixel Mode Setting for CSI-2 Serial Output

Setting item	Register details			Initial value	Setting value				Function
					50 fps	30 fps	25 fps		
					4 Lane	4 Lane	4 Lane	2 Lane	
	Register	Address	bit		RAW10/ RAW12	RAW10/ RAW12	RAW10/ RAW12	RAW10/ RAW12	
		ChipID ; 02h							
ADBIT	—	05h	[0]	1h	0h / 1h	←	←	←	0h ; 10 bit, 1h ; 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	←	←	←	All-pixel scan mode
WINMODE [3:0]	—	07h	[5:4]	1h	0h	←	←	←	WUXGA mode
FRSEL [1:0]	—	09h	[1:0]	2h	1h	1h	2h	2h	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	00528h (1320d)	00528h (1320d)	00528h (1320d)	00528h (1320d)	Vertical (V) direction line number designation (Effective in master mode.)
	VMAX [15:8]	19h	[7:0]						
	VMAX [16]	1Ah	[0]						
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	0465h (1125d)	0753h (1875d)	08CAh (2250d)	08CAh (2250d)	Horizontal (H) direction pixel number designation (Effective in master mode.)
	HMAX [15:8]	1Ch	[7:0]						
ODBIT	—	44h	[0]	1h	1h	←	←	←	Fixed 1h in CSI-2 Output
OPORTSEL [3:0]	—	44h	[7:4]	Eh	Eh	←	←	←	CSI-2 selected
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting				
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h					
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h					
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h					
INCKSEL5 [7:0]	—	63h	[7:0]	E8h					
		ChipID ; 05h							
INCK_FREQ [15:0]	INCK_FREQ [7:0]	41h	[7:0]	2520h	The value is set according to INCK Setting				
	INCK_FREQ [15:8]	42h	[7:0]						
INCK_FREQ2 [10:0]	INCK_FREQ2 [7:0]	4Eh	[7:0]	367h	The value is set according to INCK Setting				
	INCK_FREQ2 [10:8]	4Fh	[2:0]						
REPETITION [1:0]		03h	[1:0]	0h	0h	0h	1h	0h	
PHYSICAL_ Lane_NUM [1:0]		05h	[1:0]	3h	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
OB_SIZE_V [5:0]		14h	[5:0]	08h	0Eh	←	←	←	
NULL0_SIZE_V [5:0]		15h	[5:0]	01h	01h	←	←	←	
NULL1_SIZE_V [5:0]		16h	[5:0]	04h	04h	←	←	←	
NULL2_SIZE_V [5:0]		17h	[5:0]	04h	04h	←	←	←	
PIC_SIZE_V[11:0]	PIC_SIZE_V [7:0]	18h	[7:0]	0449h (1097d)	4C1h (1217d)	←	←	←	
	PIC_SIZE_V [11:8]	19h	[3:0]						
THSEXIT		2Ch	[7:0]	3Fh	40h	40h	30h	40h	Global Timing Setting
TCLKPRE		2Dh	[7:0]	1Fh	20h	20h	20h	20h	
TLPXESC		2Eh	[7:0]	03h	03h	←	←	←	
CSI_DT_FMT [15:0]	CSI_DT_FMT [7:0]	3Eh	[7:0]	0C0Ch	0A0Ah/ 0C0Ch	←	←	←	0A0Ah ; RAW10 0C0Ch ; RAW12
	CSI_DT_FMT [15:8]	3Fh	[7:0]						
CSI_Lane_MODE [1:0]		40h	[1:0]	3h	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
TCLK_POST		43h	[7:0]	67h	68h	68h	58h	68h	Global Timing Setting
THS_PREPARE		44h	[7:0]	17h	20h	20h	20h	20h	
THS_ZERO_MIN		45h	[7:0]	47h	40h	40h	40h	40h	
THS_TRAIL		46h	[7:0]	27h	28h	28h	18h	28h	
TCLK_TRAIL_MIN		47h	[7:0]	1Fh	20h	20h	10h	20h	
TCLK_PREPARE		48h	[7:0]	17h	18h	18h	10h	18h	
TCLK_ZERO		49h	[7:0]	77h	78h	78h	48h	78h	
TLPX		4Ah	[7:0]	27h	28h	28h	28h	28h	

TENTATIVE

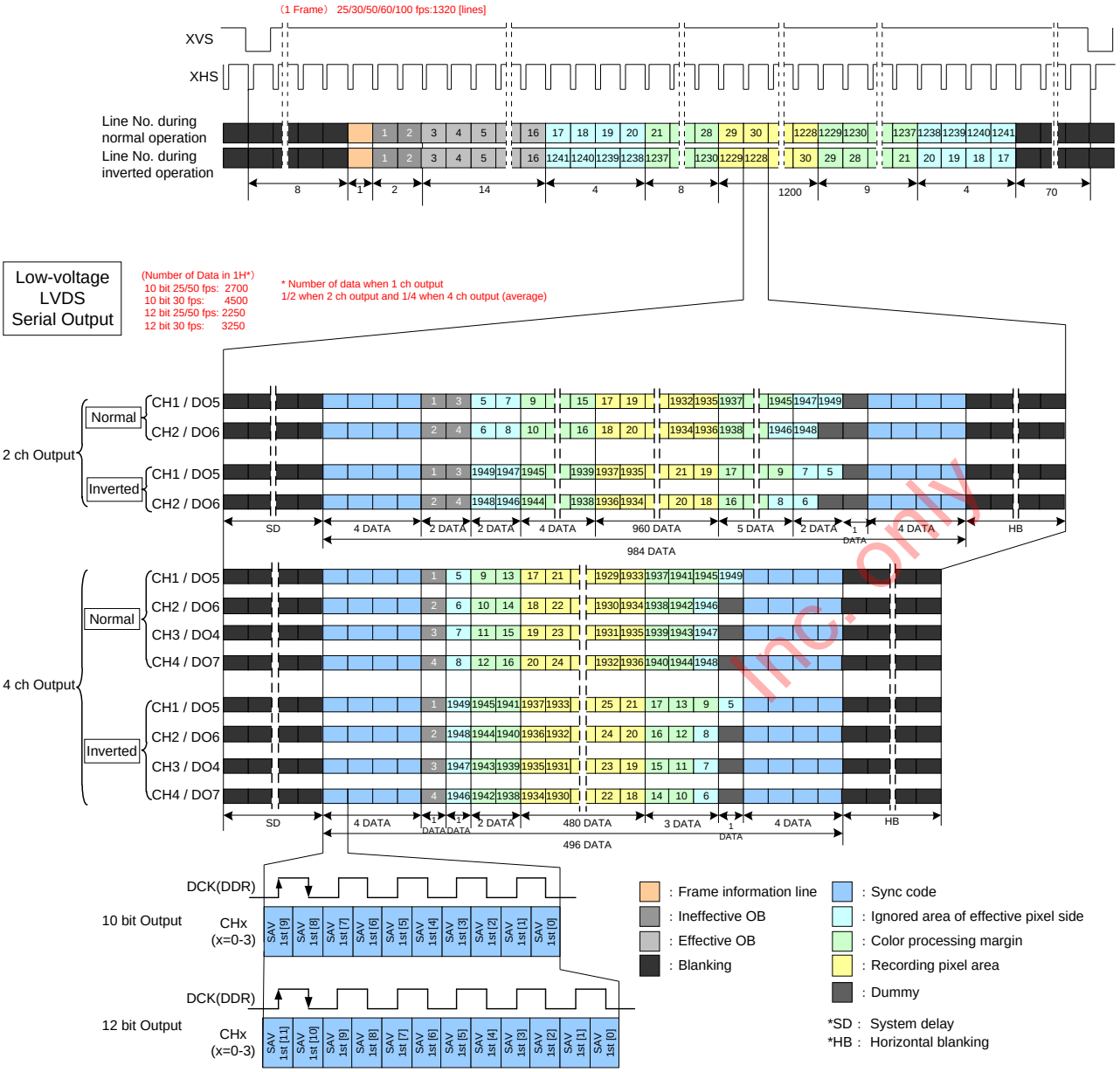


Pixel Array Image Drawing in All-pixel Scan Mode



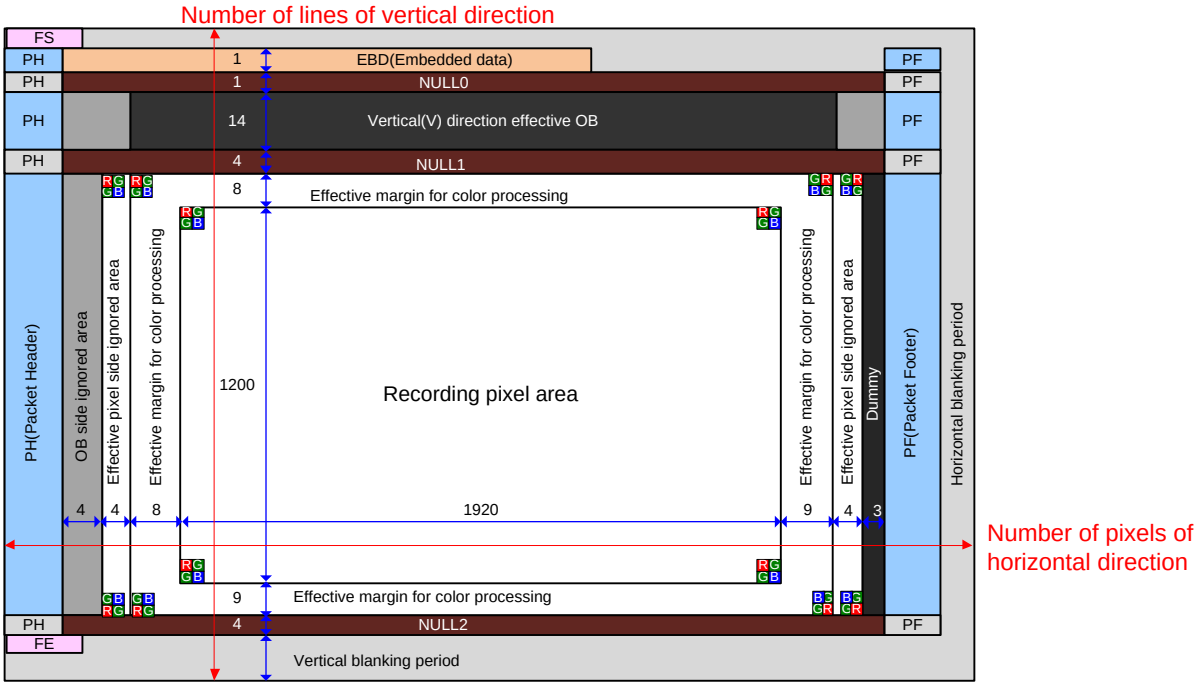
Drive Timing Chart for LVDS Parallel Output in All-pixel Scan Mode

TENTATIVE

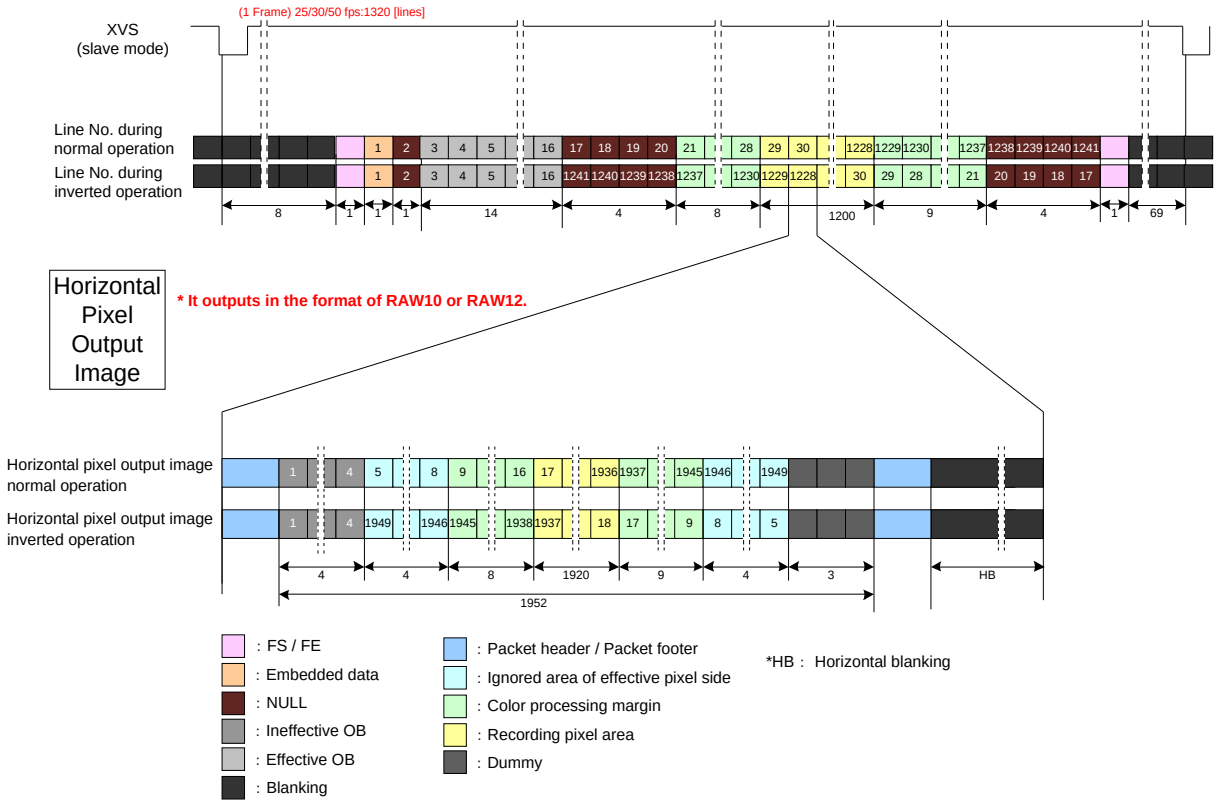


Drive Timing Chart for LVDS Serial Output in All-pixel Scan Mode

TENTATIVE



Pixel Array Image Drawing in All-pixel Scan Mode (CSI-2 Serial Output)



Drive Timing Chart for CSI-2 Serial Output in All-pixel Scan Mode

TENTATIVE

Horizontal / vertical 2/2-line bining readout mode

Sensor signals are read out by bining in vertical direction and horizontal direction.

Register List of Horizontal / Vertical 2/2-line Bining Readout Mode Setting

Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
		ChipID ; 02h				
ADBIT	—	05h	[0]	1h	0h ; See below and the next section	0h ; 10 bit
MODE [5:0]	—	06h	[5:0]	00h	22h	Horizontal / Vertical 2/2-line Bining
WINMODE [3:0]	—	07h	[5:4]	1h	0h	WUXGA mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below and the next section	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	See below and the next section	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h	[7:0]			
	VMAX [16]	1Ah	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	See below and the next section	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch	[7:0]			
ODBIT	—	44h	[0]	1h	1h ; See below and the next section	1h ; 12 bit
OPORTSEL [3:0]	—	44h	[7:4]	Eh	See below and the next section	Low-voltage LVDS Parallel / Low-voltage LVDS Serial /CSI-2 Serial output selection
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting	
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h		
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h		
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h		
INCKSEL5 [7:0]	—	63h	[7:0]	E8h		

Detailed Register List of Horizontal / Vertical 2/2-line Bining Readout Mode Setting for LVDS Parallel Output

INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage Parallel Output	25.00	12 bit	2h	0294h	660d	2328h	9000d	0h	1h	6h
		30.00	12 bit	1h			1D4Ch	7500d			
		50.00	12 bit	1h			1194h	4500d			
		60.00	12 bit	0h			0EA6h	3750d			
		100.00	12 bit	0h			08CAh	2250d			

Detailed Register List of Horizontal / Vertical 2/2-line Bining Readout Mode Setting for LVDS Serial Output

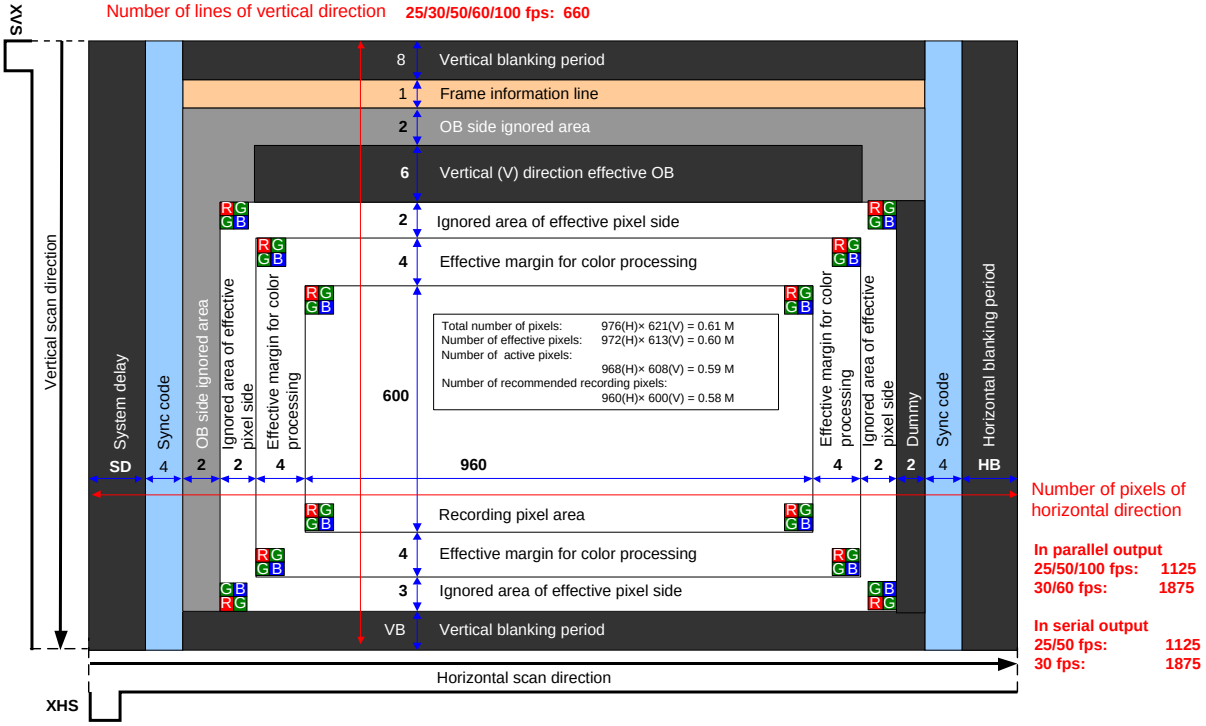
INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage serial 2 ch	25.00	12 bit	2h	0294h	660d	1194h	4500d	0h	1h	Dh
	Low -voltage serial 4 ch	25.00	12 bit	2h							Eh
		30.00	12 bit	1h			0EA6h	3750d			
		50.00	12 bit	1h			08CAh	2250d			

TENTATIVE

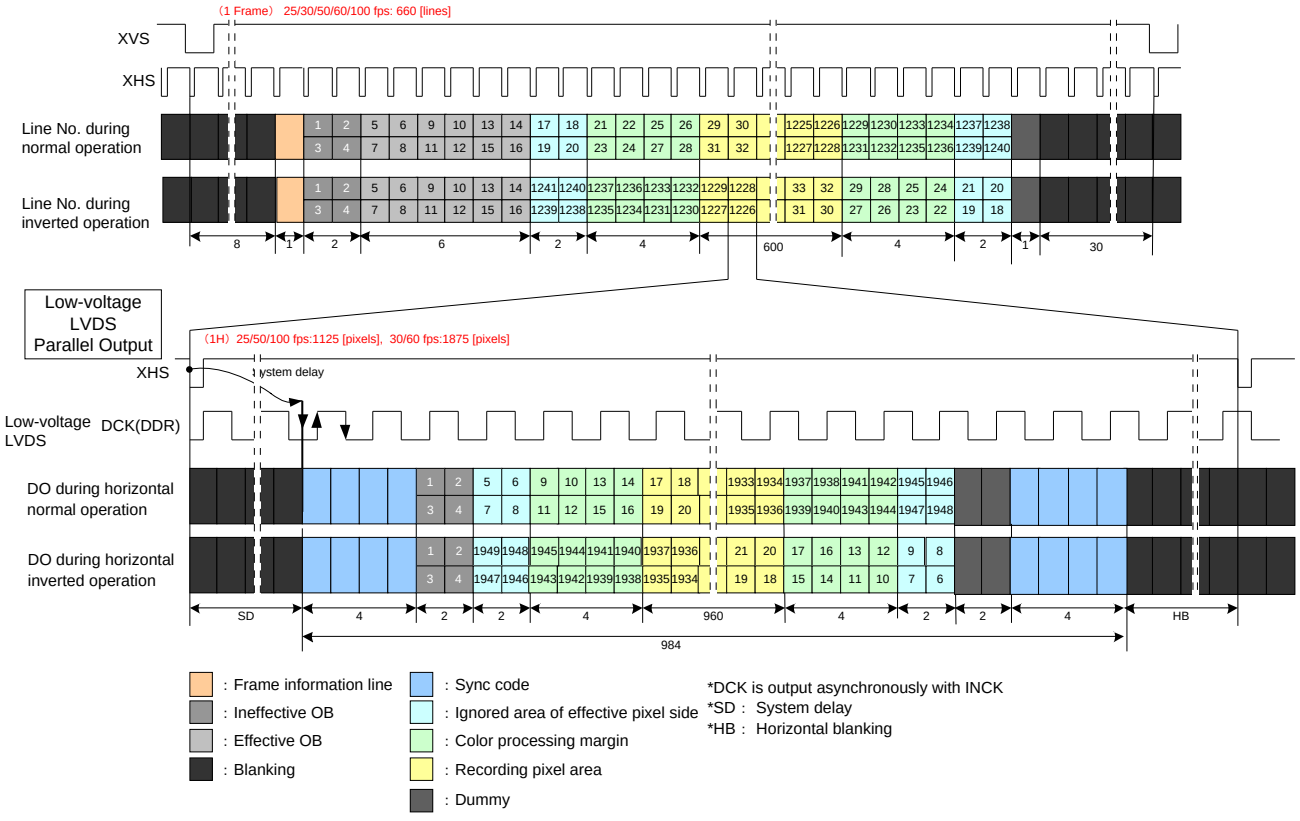
Detailed Register List of Horizontal / Vertical 2/2-line Bining Readout Mode Setting for CSI-2 Serial Output

Setting item	Register details			Initial value	Setting value				Function
	Register	Address	bit		44 fps	30 fps	22 fps		
					4 Lane	4 Lane	4 Lane	2 Lane	
					RAW12	RAW12	RAW12	RAW12	
		ChipID ; 02h							
ADBIT	—	05h	[0]	1h	0h	←	←	←	0h ; 10 bit
MODE [5:0]	—	06h	[5:0]	00h	22h	←	←	←	H/V 2/2-line Bining
WINMODE [3:0]	—	07h	[5:4]	1h	0h	←	←	←	WUXGA mode
FRSEL [1:0]	—	09h	[1:0]	2h	1h	1h	1h	2h	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	02A3h (675d)	0294h (660d)	02A3h (675d)	02A3h (675d)	Vertical (V) direction line number designation (Effective in master mode.)
	VMAX [15:8]	19h	[7:0]						
	VMAX [16]	1Ah	[0]						
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	09C4h (2500d)	0EA6h (3750d)	1388h (5000d)	1388h (5000d)	Horizontal (H) direction pixel number designation (Effective in master mode.)
	HMAX [15:8]	1Ch	[7:0]						
ODBIT	—	44h	[0]	1h	1h	←	←	←	Fixed 1h in CSI-2 Output
OPORTSEL [3:0]	—	44h	[7:4]	Eh	Eh	←	←	←	CSI-2 selected
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting				
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h					
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h					
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h					
INCKSEL5 [7:0]	—	63h	[7:0]	E8h					
		ChipID ; 05h							
INCK_FREQ [15:0]	INCK_FREQ [7:0]	41h	[7:0]	2520h	The value is set according to INCK Setting				
	INCK_FREQ [15:8]	42h	[7:0]						
INCK_FREQ2 [10:0]	INCK_FREQ2 [7:0]	4Eh	[7:0]	367h	The value is set according to INCK Setting				
	INCK_FREQ2 [10:8]	4Fh	[2:0]						
REPETITION [1:0]		03h	[1:0]	0h	2h	2h	2h	2h	
PHYSICAL_ Lane_NUM [1:0]		05h	[1:0]	3h	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
OB_SIZE_V [5:0]		14h	[5:0]	08h	06h	←	←	←	
NULL0_SIZE_V [5:0]		15h	[5:0]	01h	01h	←	←	←	
NULL1_SIZE_V [5:0]		16h	[5:0]	04h	02h	←	←	←	
NULL2_SIZE_V [5:0]		17h	[5:0]	04h	02h	←	←	←	
PIC_SIZE_V [11:0]	PIC_SIZE_V [7:0]	18h	[7:0]	0449h (1097d)	0260h (0608d)	0260h (0608d)	0260h (0608d)	0260h (0608d)	
	PIC_SIZE_V [11:8]	19h	[3:0]						
THSEXIT		2Ch	[7:0]	3Fh	28h	←	←	←	Global Timing Setting
TCLKPRE		2Dh	[7:0]	1Fh	20h	←	←	←	
TLPXESC		2Eh	[7:0]	03h	03h	←	←	←	
CSI_DT_FMT [15:0]	CSI_DT_FMT [7:0]	3Eh	[7:0]	0C0Ch	0C0Ch	←	←	←	0C0Ch ; RAW12
	CSI_DT_FMT [15:8]	3Fh	[7:0]						
CSI_Lane_MODE [1:0]		40h	[1:0]	3h	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
TCLK_POST		43h	[7:0]	67h	58h	←	←	←	Global Timing Setting
THS_PREPARE		44h	[7:0]	17h	10h	←	←	←	
THS_ZERO_MIN		45h	[7:0]	47h	30h	←	←	←	
THS_TRAIL		46h	[7:0]	27h	10h	←	←	←	
TCLK_TRAIL_MIN		47h	[7:0]	1Fh	0Bh	←	←	←	
TCLK_PREPARE		48h	[7:0]	17h	08h	←	←	←	
TCLK_ZERO		49h	[7:0]	77h	30h	←	←	←	
TLPX		4Ah	[7:0]	27h	20h	←	←	←	

TENTATIVE

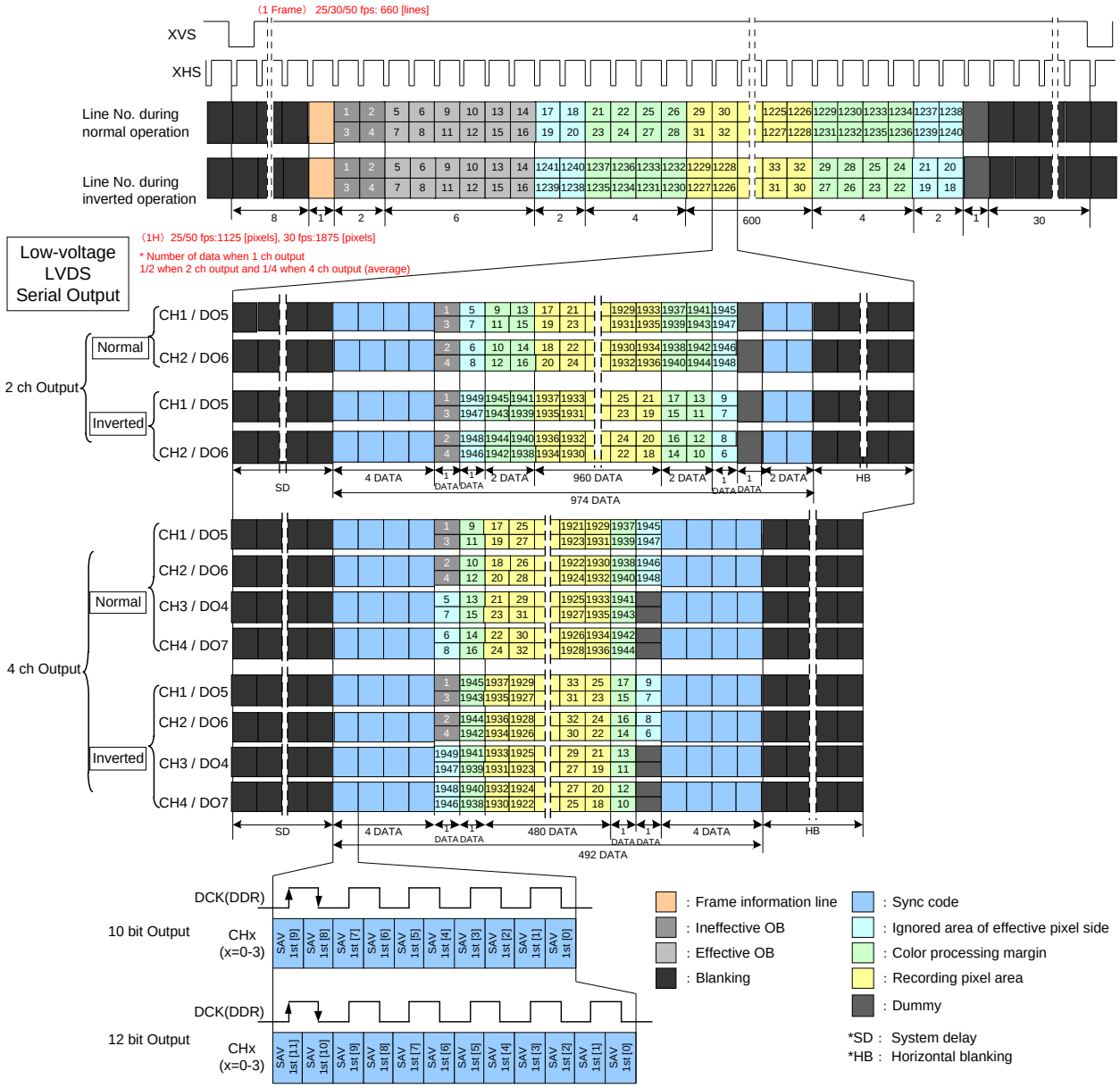


Pixel Array Image Drawing in Horizontal / Vertical 2/2-line Bining Readout Mode



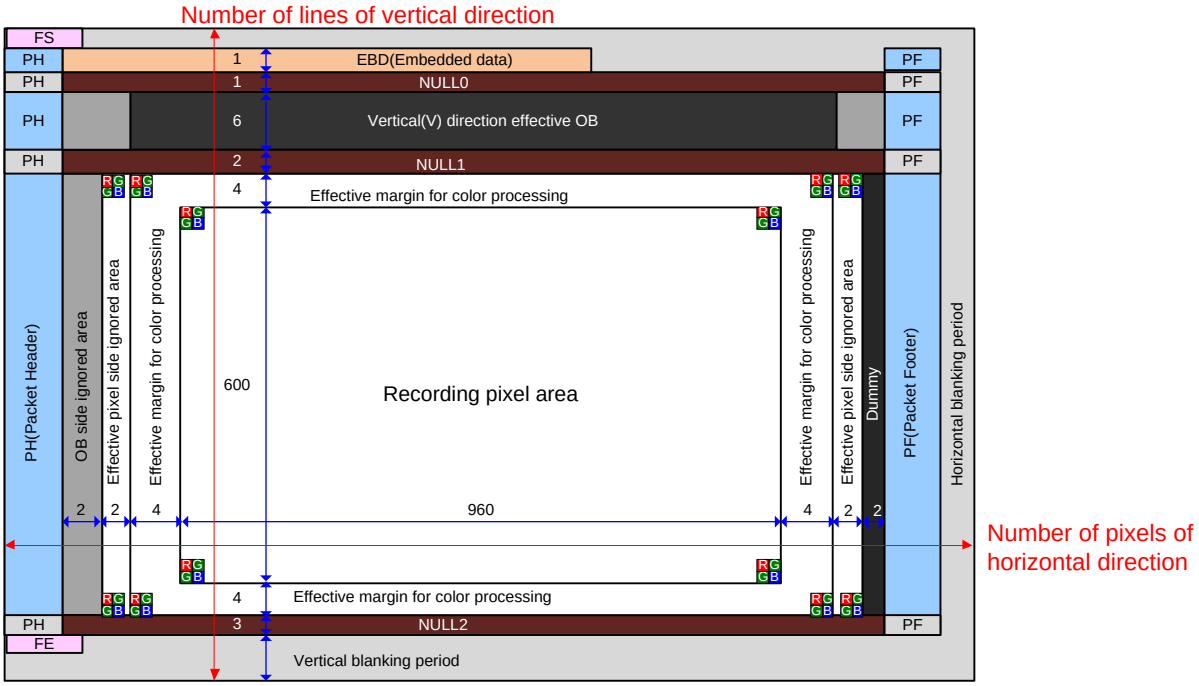
Drive Timing Chart for LVDS Parallel Output in Horizontal / Vertical 2/2-line Bining Readout Mode

TENTATIVE

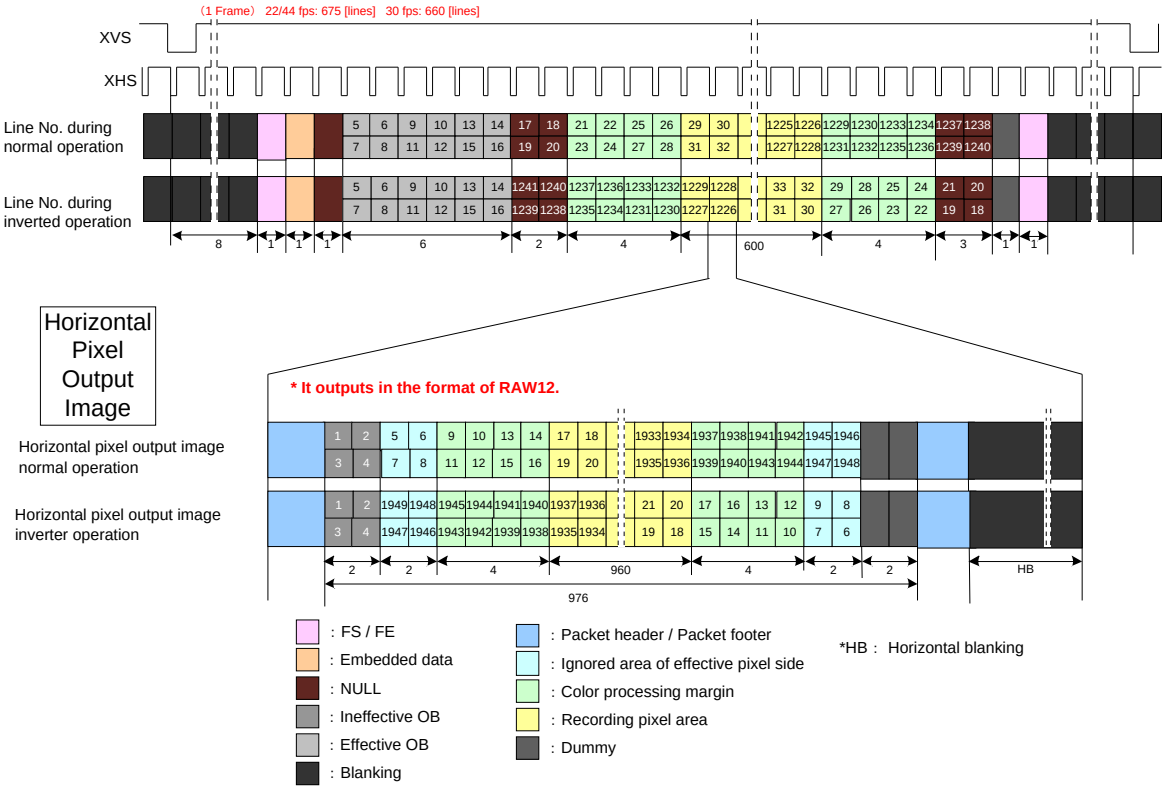


Drive Timing Chart for LVDS Serial Output Horizontal / Vertical 2/2-line Bining Readout Mode

TENTATIVE



Pixel Array Image Drawing in Horizontal / Vertical 2/2-line Bining Readout Mode
(CSI-2 Serial Output)



Drive Timing Chart for CSI-2 Serial Output Horizontal / Vertical 2/2-line Bining Readout Mode

TENTATIVE

1080p-HD Mode

The sensor signal is cut out with the angle of view for 1080p-HD (1920 × 1080) and read

Register List of 1080p-HD Mode (LVDS Parallel/Serial)

Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
		ChipID ; 02h				
ADBIT	—	05h	[0]	1h	See below and the next section	10 bit or 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	All-pixel scan mode
WINMODE [3:0]	—	07h	[5:4]	1h	1h	1080p mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below and the next section	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	See below and the next section	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h	[7:0]			
	VMAX [16]	1Ah	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	See below and the next section	1 Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch	[7:0]			
ODBIT	—	44h	[0]	1h	See below and the next section	10 bit or 12 bit
OPORTSEL [3:0]	—	44h	[7:4]	Eh	See below and the next section	Low-voltage LVDS Parallel / Low-voltage LVDS Serial /CSI-2 Serial output selection
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	I The value is set according to INCK Setting	
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h		
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h		
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h		
INCKSEL5 [7:0]	—	63h	[7:0]	E8h		

Detailed Register List of 1080p-HD Mode Setting for LVDS Parallel Output

INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage Parallel Output	30.00	10 bit	2h	0465h	1125d	1130h	4400d	0h	0h	6h
			12 bit	2h					1h	1h	
		60.00	10 bit	1h			0898h	2200d	0h	0h	
			12 bit	1h					1h	1h	
		120.00	10 bit	0h			044Ch	1100d	0h	0h	

TENTATIVE

Detailed Register List of 1080p-HD Mode Setting for LVDS Serial Output

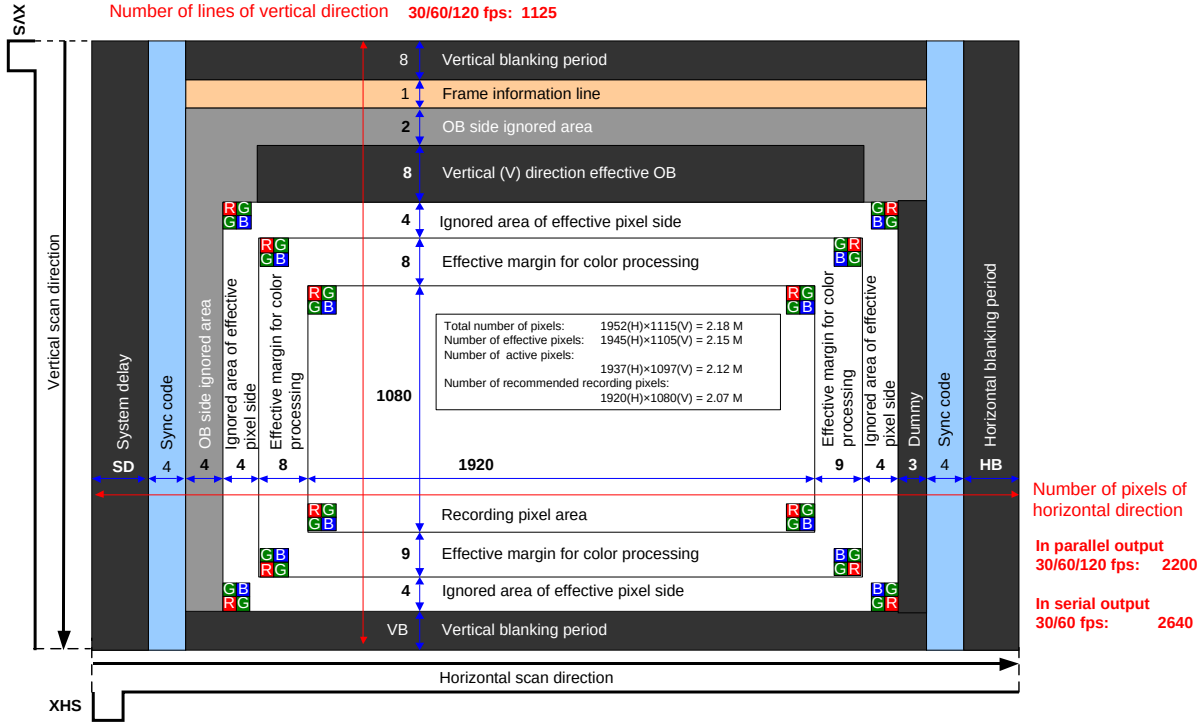
INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage serial 2 ch	30.00	10 bit	2h	0465h	1125d	0898h	2200d	0h	0h	Dh
			12 bit	2h					1h	1h	
	Low -voltage serial 4 ch	30.00	10 bit	2h					0h	0h	Eh
			12 bit	2h					1h	1h	
		60.00	10 bit	1h			044Ch	1100d	0h	0h	
			12 bit	1h					1h	1h	

TENTATIVE

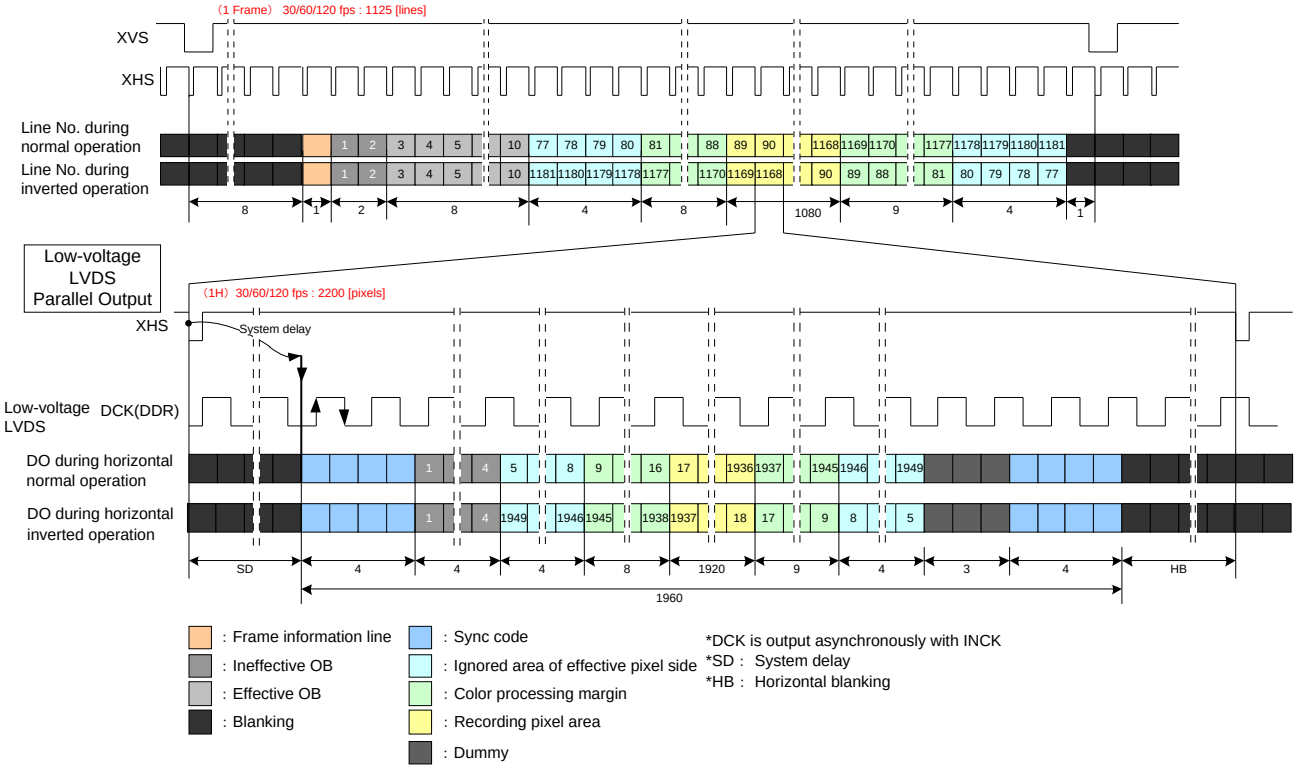
Detailed Register List of 1080p-HD Mode Setting for CSI-2 Serial Output

Setting item	Register details			Initial value	Setting value			Function
					60 fps	30 fps		
					4 Lane	4 Lane	2 Lane	
	Register	Address	bit		RAW10/ RAW12	RAW10/ RAW12	RAW10/ RAW12	
		ChipID ; 02h						
ADBIT	—	05h	[0]	1h	0h / 1h	0h / 1h	←	0h ; 10 bit, 1h ; 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	00h	←	All-pixel scan mode
WINMODE [3:0]	—	07h	[5:4]	1h	1h	1h	←	1080p mode
FRSEL [1:0]	—	09h	[1:0]	2h	1h	2h	2h	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	0465h (1125d)	0465h (1125d)	0465h (1125d)	Vertical (V) direction line number designation (Effective in master mode.)
	VMAX [15:8]	19h	[7:0]					
	VMAX [16]	1Ah	[0]					
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	044Ch (1100d)	0898h (2200d)	0898h (2200d)	Horizontal (H) direction pixel number designation (Effective in master mode.)
	HMAX [15:8]	1Ch	[7:0]					
ODBIT	—	44h	[0]	1h	1h	1h	←	Fixed 1h in CSI-2 Output
OPORTSEL [3:0]	—	44h	[7:4]	Eh	Eh	Eh	←	CSI-2 selected
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting			
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h				
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h				
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h				
INCKSEL5 [7:0]	—	63h	[7:0]	E8h				
		ChipID ; 05h						
INCK_FREQ [15:0]	INCK_FREQ [7:0]	41h	[7:0]	2520h	The value is set according to INCK Setting			
	INCK_FREQ [15:8]	42h	[7:0]					
INCK_FREQ2 [10:0]	INCK_FREQ2 [7:0]	4Eh	[7:0]	367h	The value is set according to INCK Setting			
	INCK_FREQ2 [10:8]	4Fh	[2:0]					
REPETITION [1:0]		03h	[1:0]	0h	0h	1h	0h	
PHYSICAL_ Lane_NUM [1:0]		05h	[1:0]	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
OB_SIZE_V [5:0]		14h	[5:0]	08h	08h	08h	←	
NULL0_SIZE_V [5:0]		15h	[5:0]	01h	01h	01h	←	
NULL1_SIZE_V [5:0]		16h	[5:0]	04h	04h	04h	←	
NULL2_SIZE_V [5:0]		17h	[5:0]	04h	04h	04h	←	
PIC_SIZE_V [11:0]	PIC_SIZE_V [7:0]	18h	[7:0]	0449h (1097d)	0449h (1097d)	0449h (1097d)	←	
	PIC_SIZE_V [11:8]	19h	[3:0]					
THSEXIT		2Ch	[7:0]	3Fh	40h	30h	40h	Global Timing Setting
TCLKPRE		2Dh	[7:0]	1Fh	20h	20h	20h	
TLPXESC		2Eh	[7:0]	03h	03h	03h	←	
CSI_DT_FMT [15:0]	CSI_DT_FMT [7:0]	3Eh	[7:0]	0C0Ch	0A0Ah/ 0C0Ch	0A0Ah/ 0C0Ch	←	0A0Ah ; RAW10 0C0Ch ; RAW12
	CSI_DT_FMT [15:8]	3Fh	[7:0]					
CSI_Lane_MODE [1:0]		40h	[1:0]	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
TCLK_POST		43h	[7:0]	67h	68h	58h	68h	Global Timing Setting
THS_PREPARE		44h	[7:0]	17h	20h	20h	20h	
THS_ZERO_MIN		45h	[7:0]	47h	40h	40h	40h	
THS_TRAIL		46h	[7:0]	27h	28h	18h	28h	
TCLK_TRAIL_MIN		47h	[7:0]	1Fh	20h	10h	20h	
TCLK_PREPARE		48h	[7:0]	17h	18h	10h	18h	
TCLK_ZERO		49h	[7:0]	77h	78h	48h	78h	
TLPX		4Ah	[7:0]	27h	28h	28h	28h	

TENTATIVE

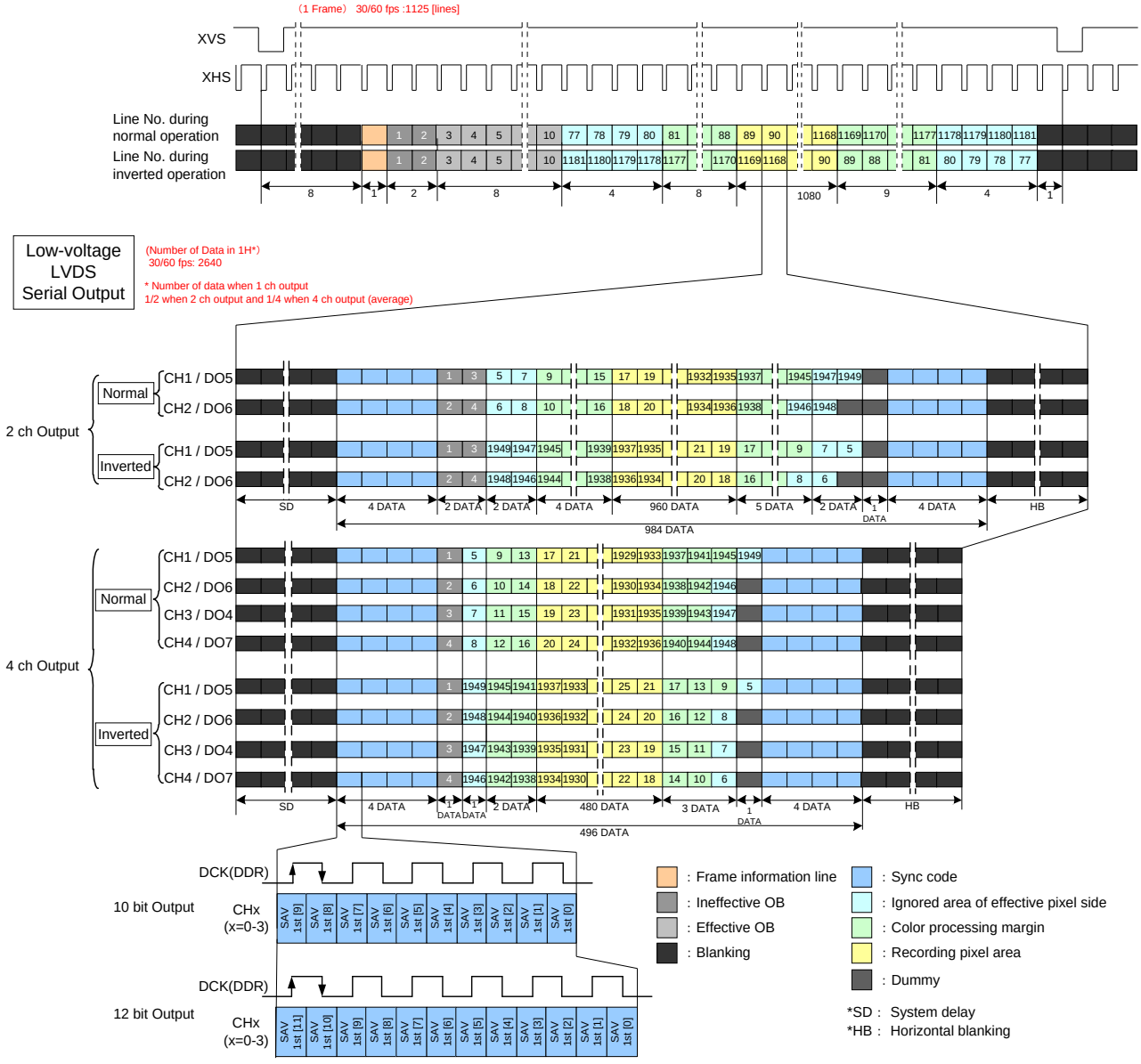


Pixel Array Image Drawing in 1080p-HD Mode



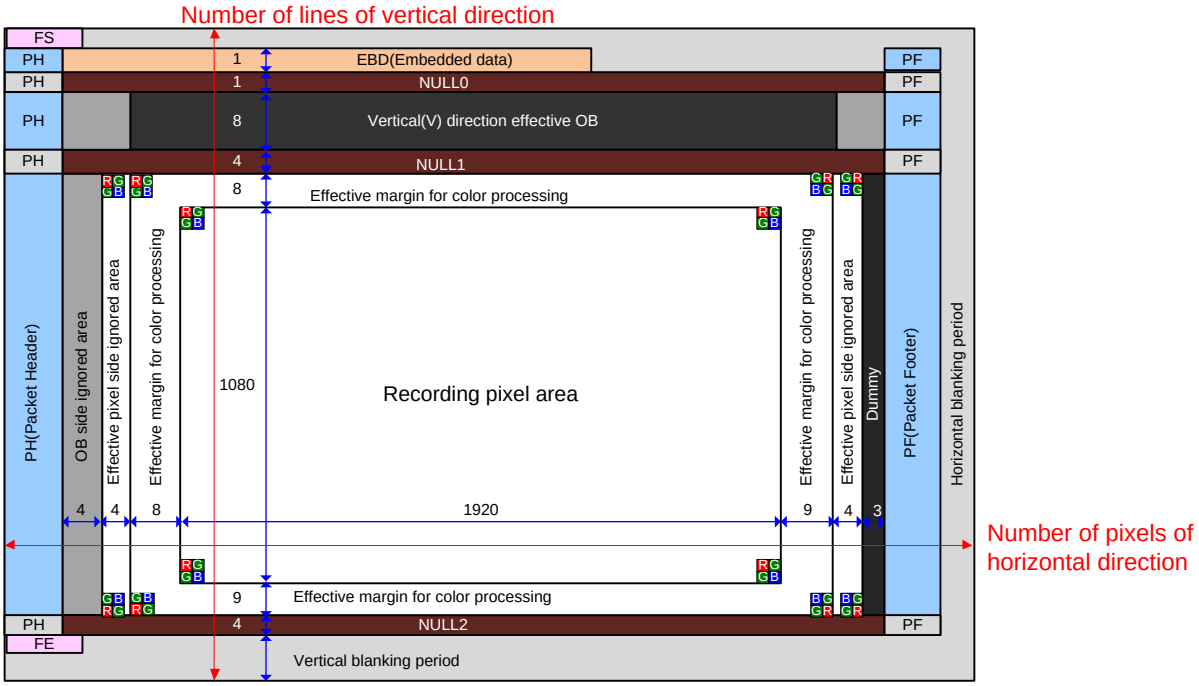
Drive Timing Chart for LVDS Parallel Output in 1080p-HD Mode

TENTATIVE

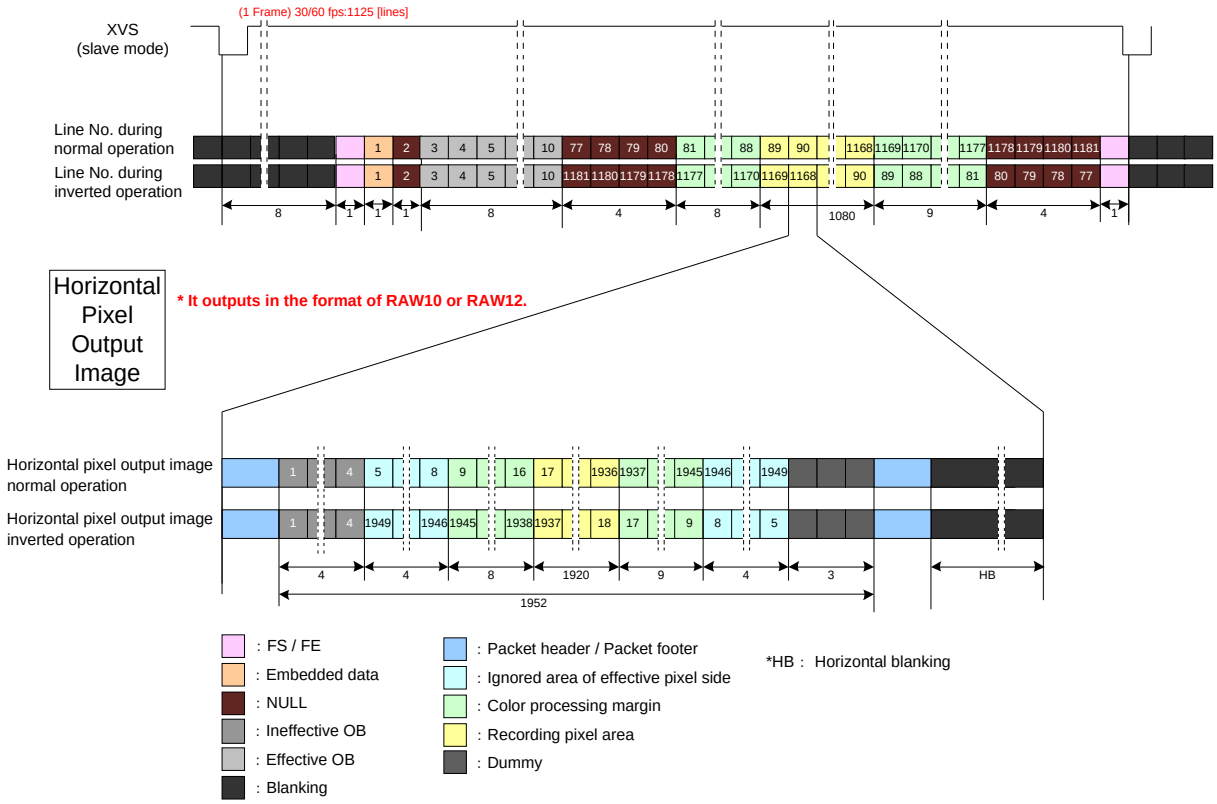


Drive Timing Chart for LVDS Serial Output in 1080p-HD Mode

TENTATIVE



Pixel Array Image Drawing in 1080p-HD Mode (CSI-2 Serial Output)



Drive Timing Chart for CSI-2 Serial Output in 1080p-HD Mode

TENTATIVE

720p-HD Mode

The sensor signal is cut out with the angle of view for 720p-HD (1280 × 720) and read

Register List of 720p-HD Mode (Low-voltage LVDS Parallel / Serial output)

Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
		ChipID ; 02h				
ADBIT	—	05h	[0]	1h	See below and the next section	10 bit or 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	All-pixel scan mode
WINMODE [3:0]	—	07h	[5:4]	1h	2h	720p mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below and the next section	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	See below and the next section	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h	[7:0]			
	VMAX [16]	1Ah	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	See below and the next section	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch	[7:0]			
ODBIT	—	44h	[0]	1h	See below and the next section	10 bit or 12 bit
OPORTSEL [3:0]	—	44h	[7:4]	Eh	See below and the next section	Low-voltage LVDS Parallel / Low-voltage LVDS Serial /CSI-2 Serial output selection
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting	
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h		
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h		
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h		
INCKSEL5 [7:0]	—	63h	[7:0]	E8h		

Detailed Register List of 720p-HD Mode Setting (LVDS Parallel Output)

INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage Parallel Output	30.00	10 bit	2h	02EEh	750d	19C8h	6600d	0h	0h	6h
			12 bit	2h					1h	1h	
		60.00	10 bit	1h			0CE4h	3300d	0h	0h	
			12 bit	1h					1h	1h	
		120.00	10 bit	0h			0672h	1650d	0h	0h	

TENTATIVE

Detailed Register List of 720p-HD Mode Setting (LVDS Serial Output)

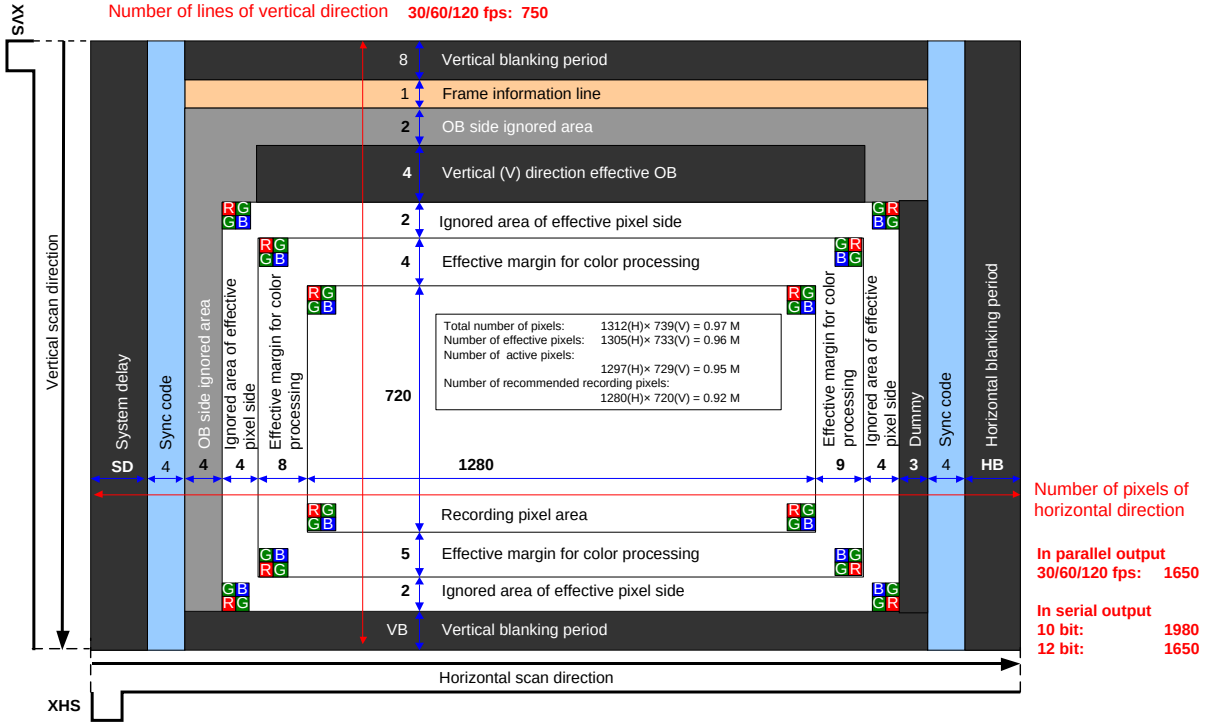
INCK [MHz]	Output format	Output frame rate (fps)	Bit Width	FRSEL [1:0]	VMAX [16:0]		HMAX [15:0]		ADBIT	ODBIT	OPORTSEL [3:0]
					HEX	DEC	HEX	DEC			
37.125 / 27 / 74.25 / 54	Low -voltage serial 2 ch	30.00	10 bit	2h	02EEh	0750d	0CE4h	3300d	0h	0h	Dh
			12 bit	2h					1h	1h	
		60.00	10 bit	1h			0672h	1650d	0h	0h	
			12 bit	1h					1h	1h	
	Low -voltage serial 4 ch	30.00	10 bit	2h			0CE4h	3300d	0h	0h	Eh
			12 bit	2h					1h	1h	
		60.00	10 bit	1h			0672h	1650d	0h	0h	
			12 bit	1h					1h	1h	
		120.00	10 bit	0h			0339h	825d	0h	0h	

TENTATIVE

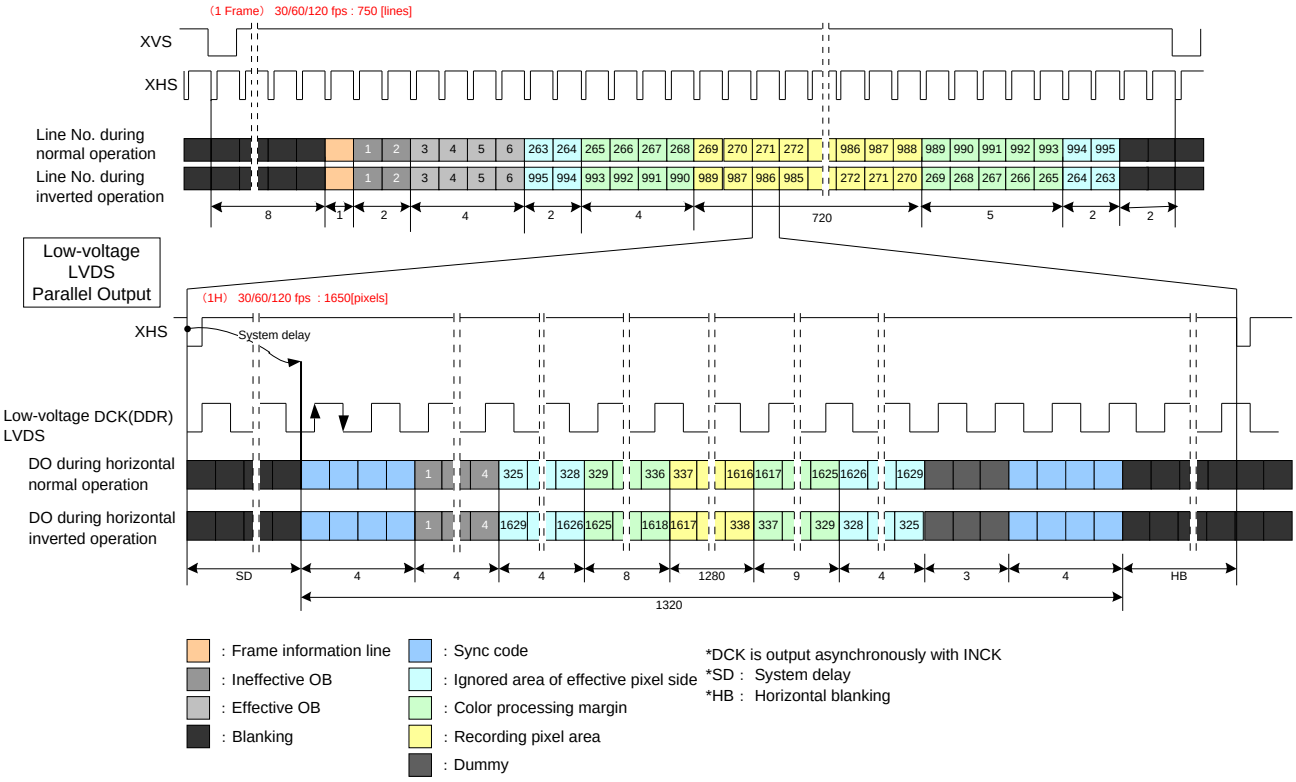
Detailed Register List of 720p-HD Mode Setting for CSI-2 Serial Output

Setting item	Register details			Initial value	Setting value					Function
					120 fps	60 fps		30 fps		
	Register	Address	bit		4 Lane	4 Lane	2 Lane	4 Lane	2 Lane	
					RAW10	RAW10/ RAW12	RAW10/ RAW12	RAW10/ RAW12	RAW10/ RAW12	
		ChipID ; 02h								
ADBIT	—	05h	[0]	1h	0h	0h / 1h	←	←	←	10 bit, 12 bit
MODE [5:0]	—	06h	[5:0]	00h	00h	←	←	←	←	All-pixel mode
WINMODE [3:0]	—	07h	[5:4]	1h	2h	←	←	←	←	720p mode
FRSEL [1:0]	—	09h	[1:0]	2h	0h	1h	1h	2h	2h	Frame rate grade setting
VMAX [16:0]	VMAX [7:0]	18h	[7:0]	00465h (1125d)	02EEh (750d)	02EEh (750d)	02EEh (750d)	02EEh (750d)	02EEh (750d)	Vertical (V) direction line number designation
	VMAX [15:8]	19h	[7:0]							
	VMAX [16]	1Ah	[0]							
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0898h (2200d)	0339h (825d)	0672h (1650d)	0672h (1650d)	0CE4h (3300d)	0CE4h (3300d)	Horizontal (H) direction pixel number designation
	HMAX [15:8]	1Ch	[7:0]							
ODBIT	—	44h	[0]	1h	1h	←	←	←	←	Fixed 1h
OPORTSEL [3:0]	—	44h	[7:4]	Eh	Eh	←	←	←	←	CSI-2 selected
INCKSEL1 [7:0]	—	5Ch	[7:0]	20h	The value is set according to INCK Setting					
INCKSEL2 [7:0]	—	5Dh	[7:0]	00h						
INCKSEL3 [7:0]	—	5Eh	[7:0]	18h						
INCKSEL4 [7:0]	—	5Fh	[7:0]	00h						
INCKSEL5 [7:0]	—	63h	[7:0]	E8h						
		ChipID ; 05h								
INCK_FREQ [15:0]	INCK_FREQ [7:0]	41h	[7:0]	2520h	The value is set according to INCK Setting					
	INCK_FREQ [15:8]	42h	[7:0]							
INCK_FREQ2 [10:0]	INCK_FREQ2 [7:0]	4Eh	[7:0]	367h	The value is set according to INCK Setting					
	INCK_FREQ2 [10:8]	4Fh	[2:0]							
REPETITION [1:0]		03h	[1:0]	0h	0h	1h	0h	2h	1h	
PHYSICAL_ Lane_NUM [1:0]		05h	[1:0]	3h	3h	3h	1h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
OB_SIZE_V [5:0]		14h	[5:0]	08h	08h	←	←	←	←	
NULL0_SIZE_V [5:0]		15h	[5:0]	01h	01h	←	←	←	←	
NULL1_SIZE_V [5:0]		16h	[5:0]	04h	02h	←	←	←	←	
NULL2_SIZE_V [5:0]		17h	[5:0]	04h	02h	←	←	←	←	
PIC_SIZE_V[11:0]	PIC_SIZE_V [7:0]	18h	[7:0]	0449h (1097d)	02D9h (0729d)	←	←	←	←	
	PIC_SIZE_V [11:8]	19h	[3:0]							
THSEXIT		2Ch	[7:0]	3Fh	40h	30h	40h	28h	30h	Global Timing Setting
TCLKPRE		2Dh	[7:0]	1Fh	20h	20h	20h	20h	20h	
TLPXESC		2Eh	[7:0]	03h	03h	←	←	←	←	
CSI_DT_FMT[15:0]	CSI_DT_ FMT[7:0]	3Eh	[7:0]	0C0Ch	0A0Ah	0A0Ah/ 0C0Ch	←	←	←	0A0Ah ; RAW10 0C0Ch ; RAW12
	CSI_DT_ FMT[15:8]	3Fh	[7:0]							
CSI_Lane_MODE [1:0]		40h	[1:0]	3h	3h	3h	3h	3h	1h	1h; 2 Lane, 3h ; 4 Lane
TCLK_POST		43h	[7:0]	67h	68h	58h	68h	58h	58h	Global Timing Setting
THS_PREPARE		44h	[7:0]	17h	20h	20h	20h	10h	20h	
THS_ZERO_MIN		45h	[7:0]	47h	40h	40h	40h	30h	40h	
THS_TRAIL		46h	[7:0]	27h	28h	18h	28h	10h	18h	
TCLK_TRAIL_MIN		47h	[7:0]	1Fh	20h	10h	20h	0Bh	10h	
TCLK_PREPARE		48h	[7:0]	17h	18h	10h	18h	08h	10h	
TCLK_ZERO		49h	[7:0]	77h	78h	48h	78h	30h	48h	
TLPX		4Ah	[7:0]	27h	28h	28h	28h	20h	28h	

TENTATIVE

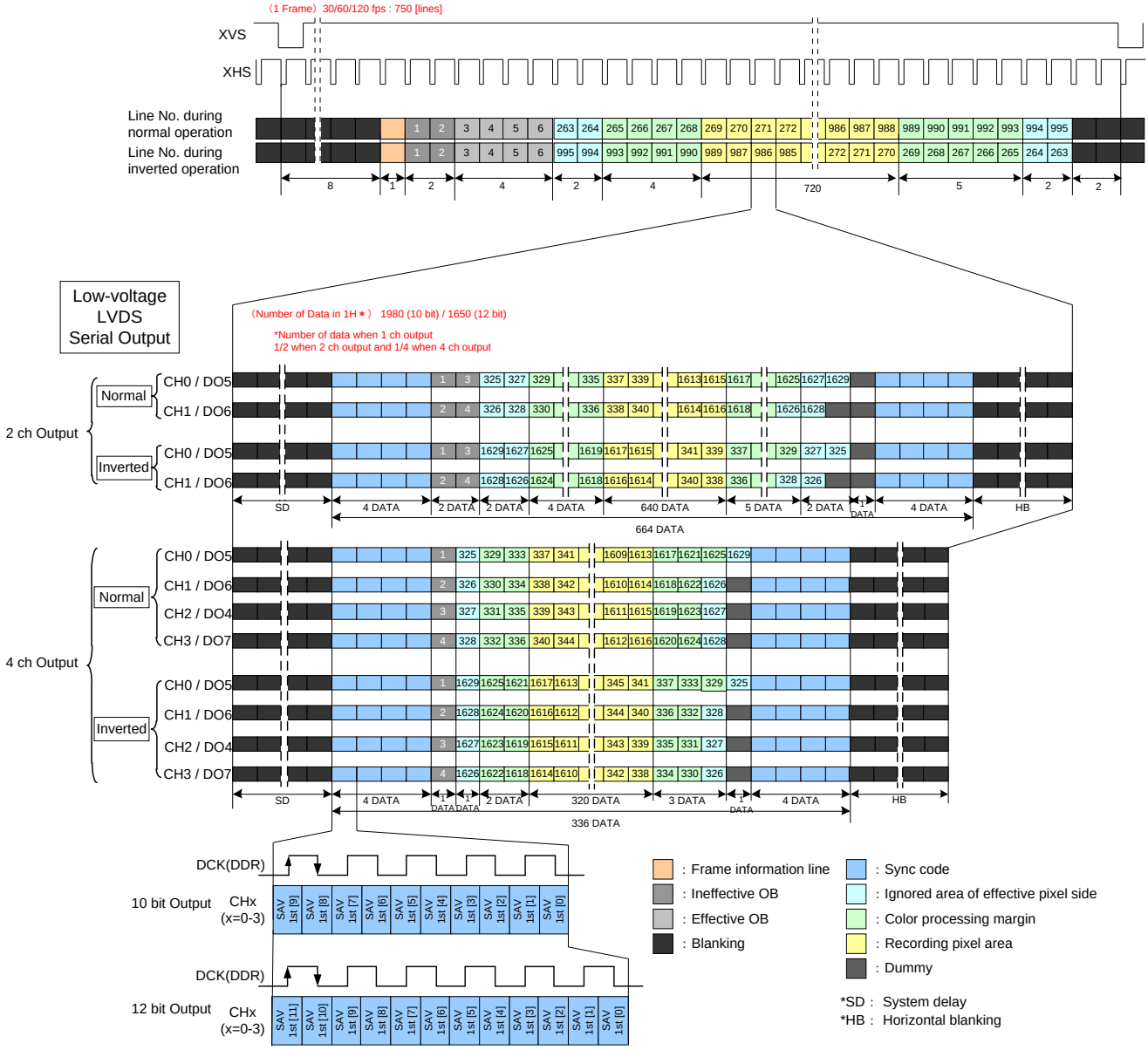


Pixel Array Image Drawing in 720p-HD Mode



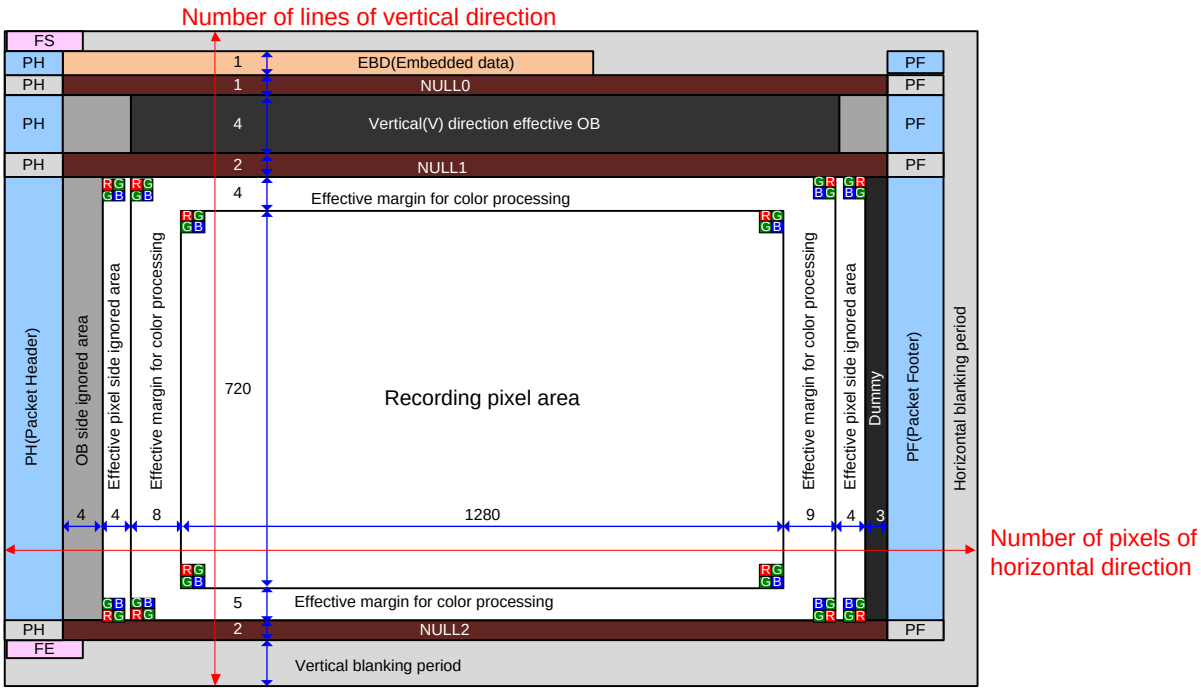
Drive Timing Chart for LVDS Parallel Output in 720p-HD Mode

TENTATIVE

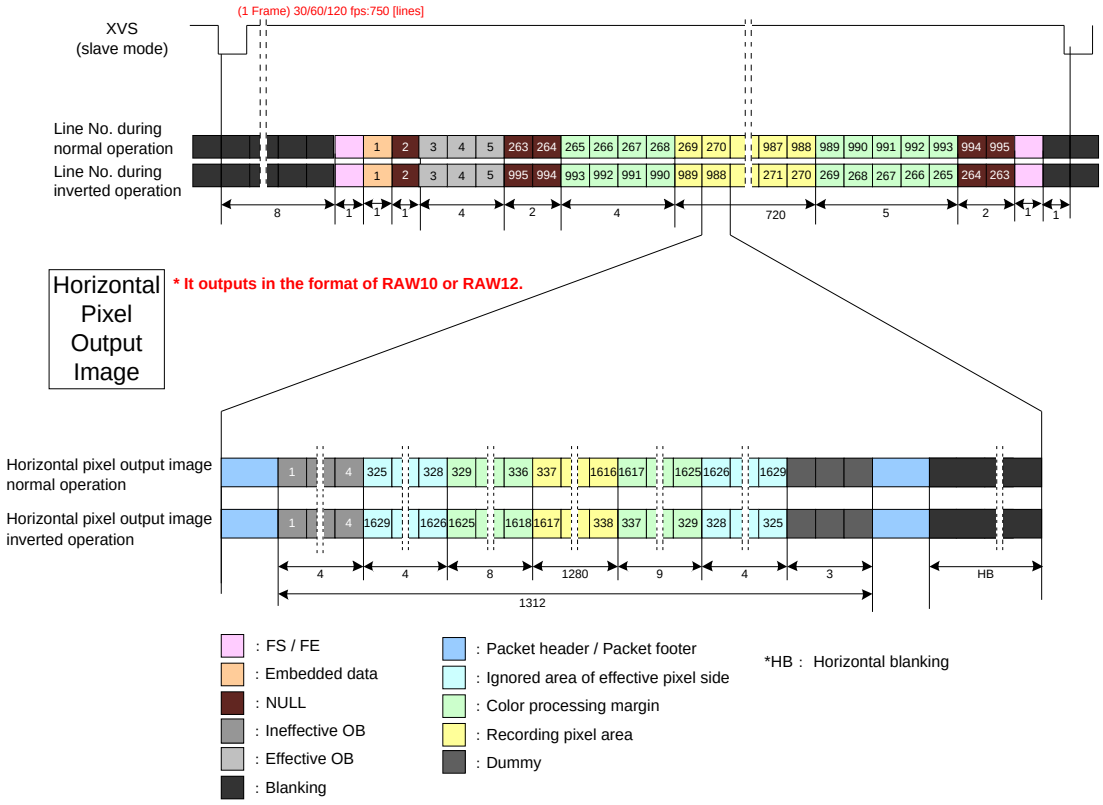


Drive Timing Chart for LVDS Serial Output in 720p-HD Mode

TENTATIVE



Pixel Array Image Drawing in 720p-HD Mode (CSI-2 Serial Output)



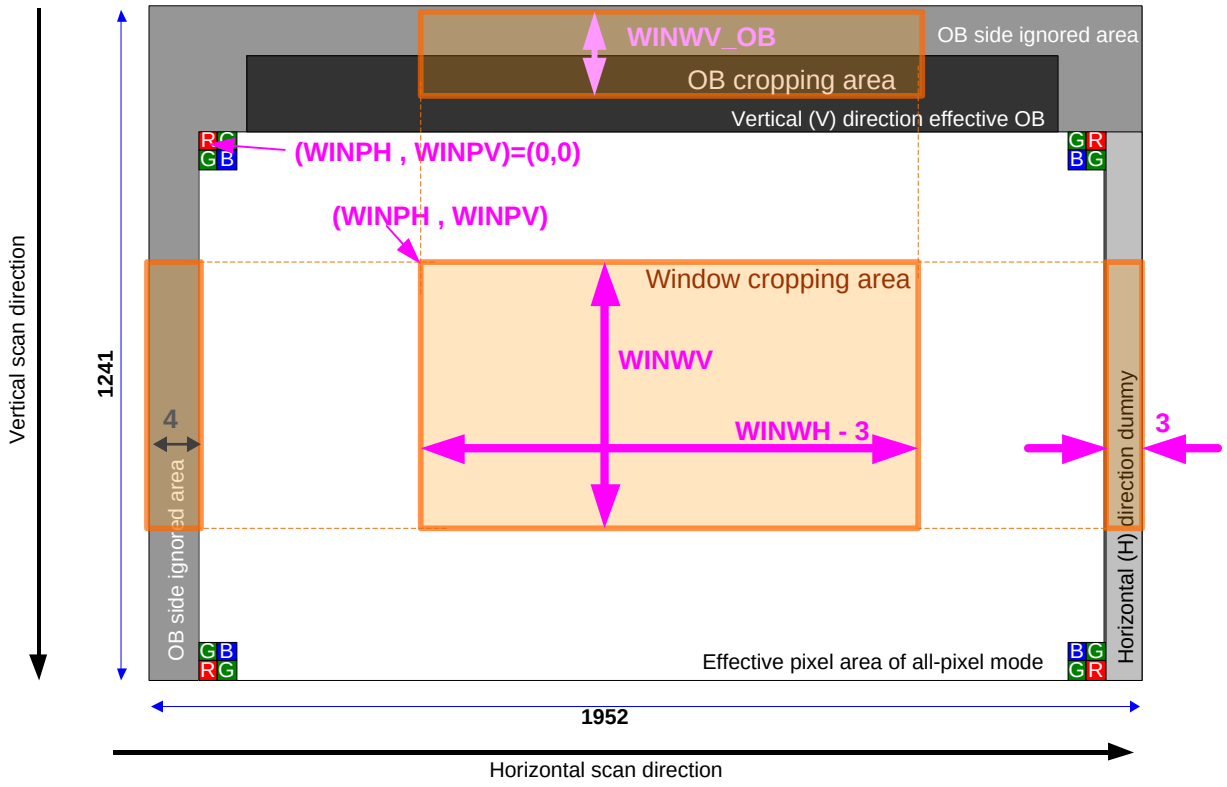
Drive Timing Chart for CSI-2 Serial Output in 720p-HD Mode

TENTATIVE

Window Cropping Mode

A sensor signals are cropped and read out at arbitrary positions.
Cropping is available at all-pixel scan mode, 1080p-HD mode and 720p-HD mode. Horizontal period is fixed to the value for each mode. Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period. In vertical cropping, the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.

Window cropping image is shown in the figure below.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.
Only vertical width can be set for OB (horizontal width is the same as the Window cropping width).



Window cropping image from all pixel (WUXGA) scan mode

TENTATIVE

Register List of Window cropping Mode Setting (Low-voltage LVDS Parallel / Serial output)

Setting item	Register details			Initial value	Setting value	Function
	Register	Address ( ) : I^2C	Bit			
		ChipID ; 02h				
MODE [5:0]	—	06h (3006h)	[5:0]	00h	00h	All-pixel scan mode
WINMODE [3:0]	—	07h (3007h)	[7:4]	1h	4h	Window cropping mode (WUXGA mode)
					5h	Window cropping mode (1080p mode)
					6h	Window cropping mode (720p mode)
VMAX [16:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h (1125d)	See below	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h (3019h)	[7:0]			
	VMAX [16]	1Ah (301Ah)	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	0898h (2200d)	See each mode setting	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch (301Ch)	[7:0]			
WINWV_OB [4:0]	WINWV_OB [4:0]	36h (3036h)	[4:0]	10h (16d)	See below	VOB Window size designation
WINPV [10:0]	WINPV [7:0]	38h (3038h)	[7:0]	000h	See below	Designation of upper left coordinate for cropping position (Vertical)
	WINPV [10:8]	39h (3039h)	[2:0]			
WINWV [10:0]	WINWV [7:0]	3Ah (303Ah)	[7:0]	4C9h (1225d)	See below	Cropping size designation (Vertical)
	WINWV [10:8]	3Bh (303Bh)	[2:0]			
WINPH [10:0]	WINPH [7:0]	3Ch (303Ch)	[7:0]	000h	See below	Designation of upper left coordinate for cropping position (Horizontal) (Set to become a multiple of 4)
	WINPH [10:8]	3Dh (303Dh)	[2:0]			
WINWH [10:0]	WINWH [7:0]	3Eh (303Eh)	[7:0]	51Ch (1308d)	See below	Cropping size designation (Horizontal) (Set to become a multiple of 8 and plus 4)
	WINWH [10:8]	3Fh (303Fh)	[2:0]			

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

WINPH + WINWH ≤ 1948
380 ≤ WINWH
Set WINPH to a multiple of 4, and set WINWH to a multiple of 8 and plus 4.

(Number of lines per frame) or VMAX ≥ WINWV_OB + WINPV + WINWV + 8

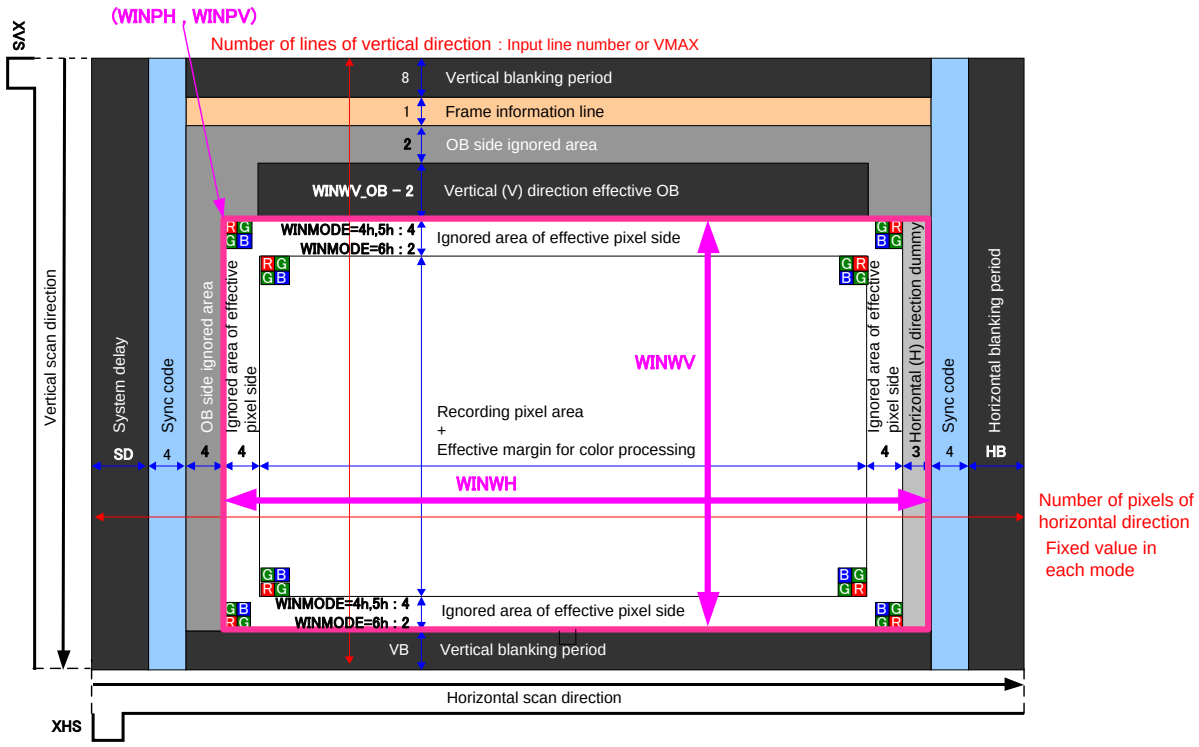
However,
6 ≤ WINWV_OB ≤ 16
WINPV + WINWV ≤ 1225
313 ≤ WINWV

Frame rate on Window cropping mode

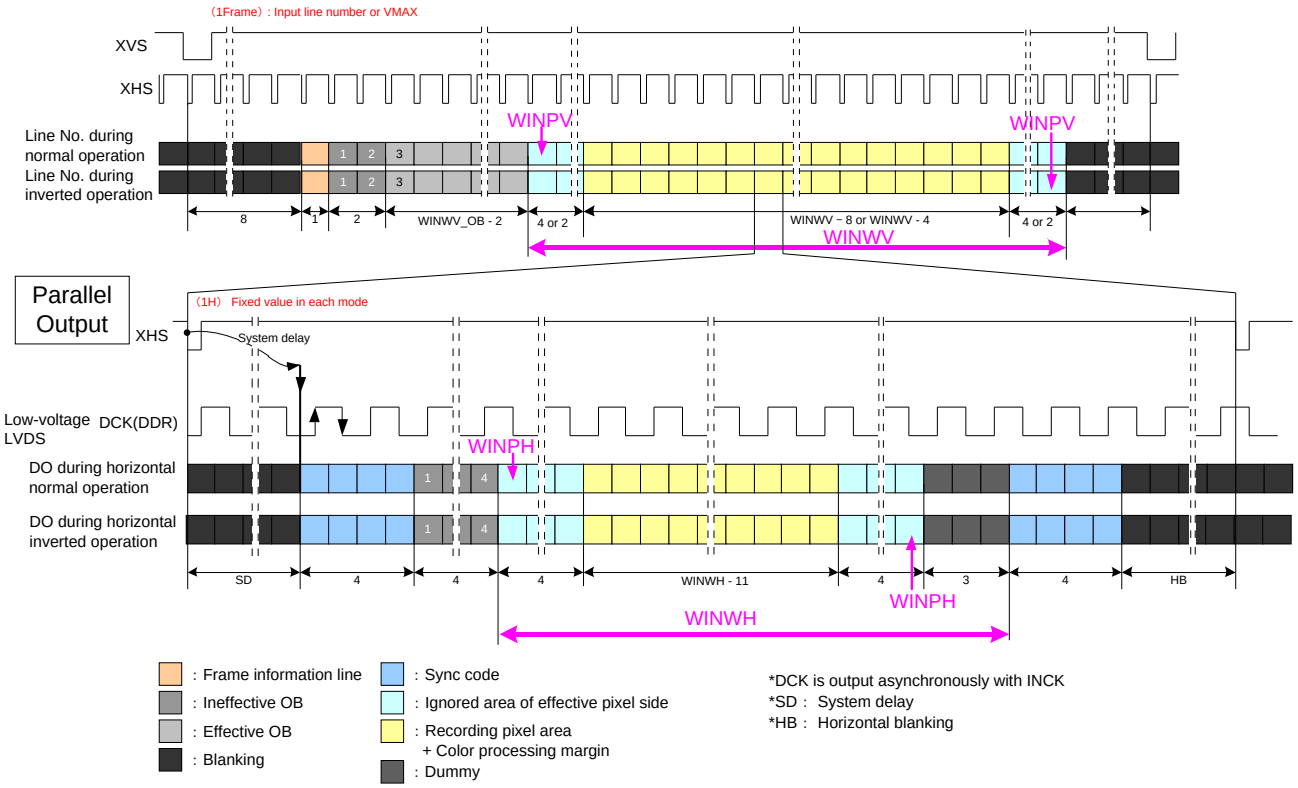
Frame rate [frame/s] = 1 / (("Number of lines per frame" or VMAX) × (1H period))

1H period (unit: [µs]) : Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

TENTATIVE

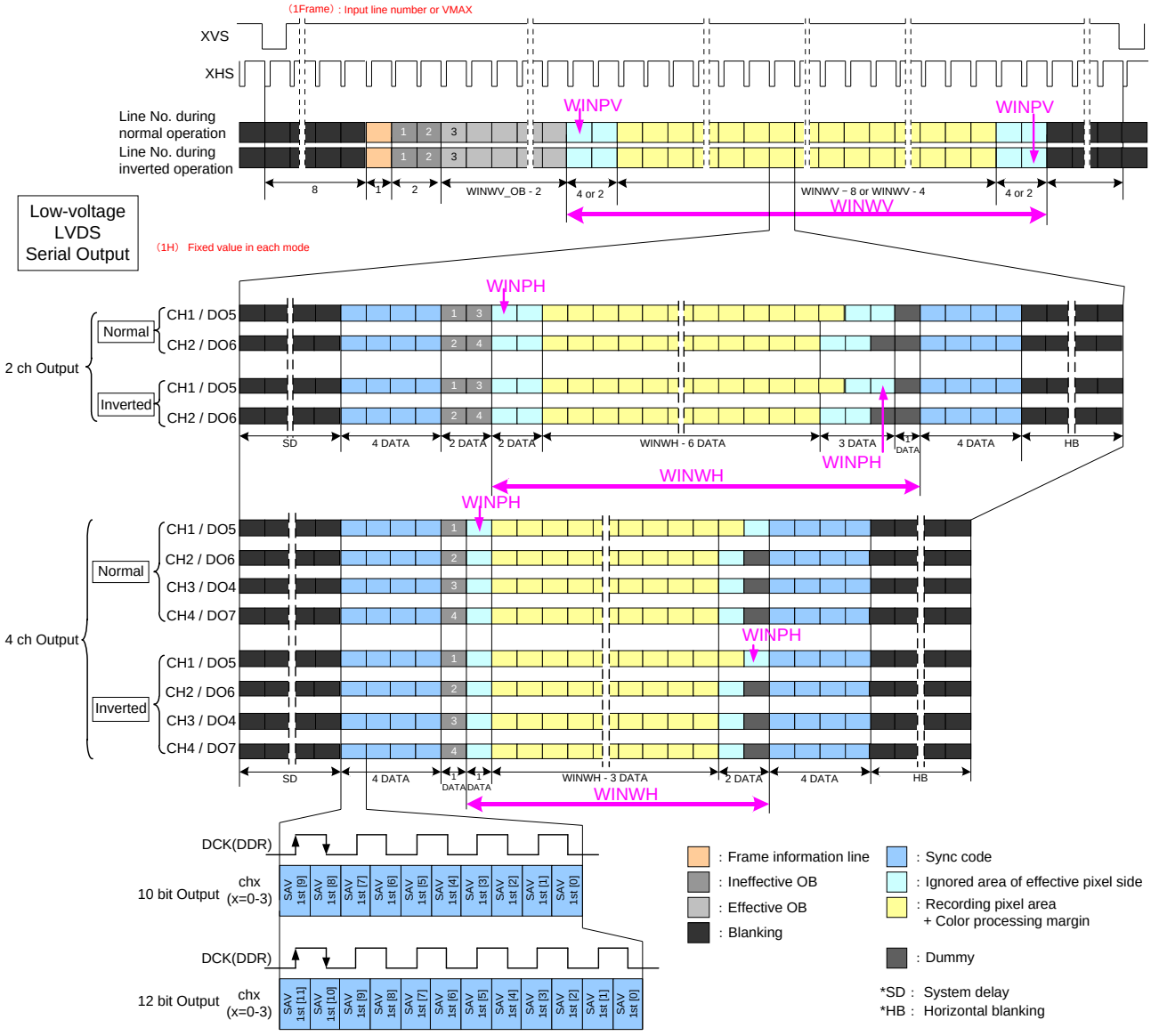


Pixel Array Image Drawing in Window cropping Mode



Drive Timing Chart for LVDS Parallel Output in Window cropping Mode

TENTATIVE



Drive Timing Chart for LVDS Serial Output in Window cropping Mode

TENTATIVE

Register List of Window cropping Mode Setting (CSI-2 output)

Setting item	Register details			Initial value	Setting value	Function
	Register	Address ( ) 内: I²C	Bit			
		ChipID ; 02h				
MODE [5:0]	—	06h (3006h)	[5:0]	00h	00h	All-pixel scan mode
WINMODE [3:0]	—	07h (3007h)	[7:4]	1h	4h	Window cropping mode (WUXGA mode)
					5h	Window cropping mode (1080p mode)
					6h	Window cropping mode (720p mode)
VMAX [16:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h (1125d)	See below	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h (3019h)	[7:0]			
	VMAX [16]	1Ah (301Ah)	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	0898h (2200d)	See each mode setting	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch (301Ch)	[7:0]			
WINWV_OB [4:0]	WINWV_OB [4:0]	36h (3036h)	[4:0]	10h (16d)	See below	VOB Window size designation
WINPV [10:0]	WINPV [7:0]	38h (3038h)	[7:0]	000h	See below	Designation of upper left coordinate for cropping position (Vertical)
	WINPV [10:8]	39h (3039h)	[2:0]			
WINWV [10:0]	WINWV [7:0]	3Ah (303Ah)	[7:0]	4C9h (1225d)	See below	Cropping size designation (Vertical)
	WINWV [10:8]	3Bh (303Bh)	[2:0]			
WINPH [10:0]	WINPH [7:0]	3Ch (303Ch)	[7:0]	000h	See below	Designation of upper left coordinate for cropping position (Horizontal) (Set to become a multiple of 4)
	WINPH [10:8]	3Dh (303Dh)	[2:0]			
WINWH [10:0]	WINWH [7:0]	3Eh (303Eh)	[7:0]	51Ch (1308d)	See below	Cropping size designation (Horizontal) (Set to become a multiple of 8 and plus 4)
	WINWH [10:8]	3Fh (303Fh)	[2:0]			
		ChipID ; 05h				
OB_SIZE_V[5:0]	—	14h (3314h)	[5:0]	0Eh (14d)	0Eh	VOB Window size designation
NULL0_SIZE_V[5:0]	—	15h (3315h)	[5:0]	01h	01h	Vertical (V) direction NULL0 number designation
NULL1_SIZE_V[5:0]	—	16h (3316h)	[5:0]	04h	04h	V NULL1 number WUXGA mode
					04h	V NULL1 number 1080p mode
					02h	V NULL1 number 720p mode
NULL2_SIZE_V[5:0]	—	17h (3317h)	[5:0]	04h	04h	V NULL1 number WUXGA mode
					04h	V NULL1 number 1080p mode
					02h	V NULL1 number 720p mod
PIC_SIZE_V[11:0]	PIC_SIZE_V[7:0]	18h (3318h)	[7:0]	0449h (1097d)	See below	
	PIC_SIZE_V[11:8]	19h (3319h)	[3:0]			

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

WINPH + WINWH ≤ 1948
380 ≤ WINWH
Set WINPH to a multiple of 4, and set WINWH to a multiple of 8 and plus 4.

(Number of lines per frame) or VMAX ≥ WINWV_OB + WINPV + WINWV + 8

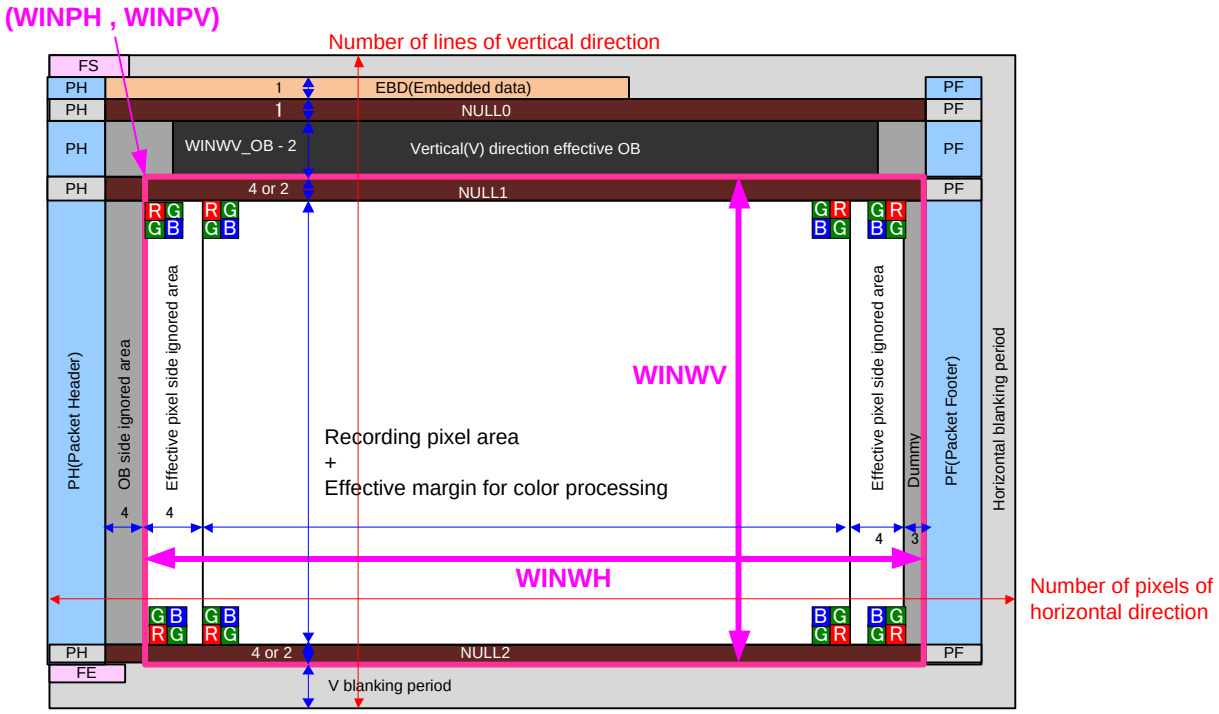
However,
6 ≤ WINWV_OB = OB_SIZE_V + 2 ≤ 16
WINPV + WINWV ≤ 1225
313 ≤ WINWV
WINPV = PIC_SIZE_V + NULL1_SIZE_V + NULL2_SIZE_V

Frame rate on Window cropping mode

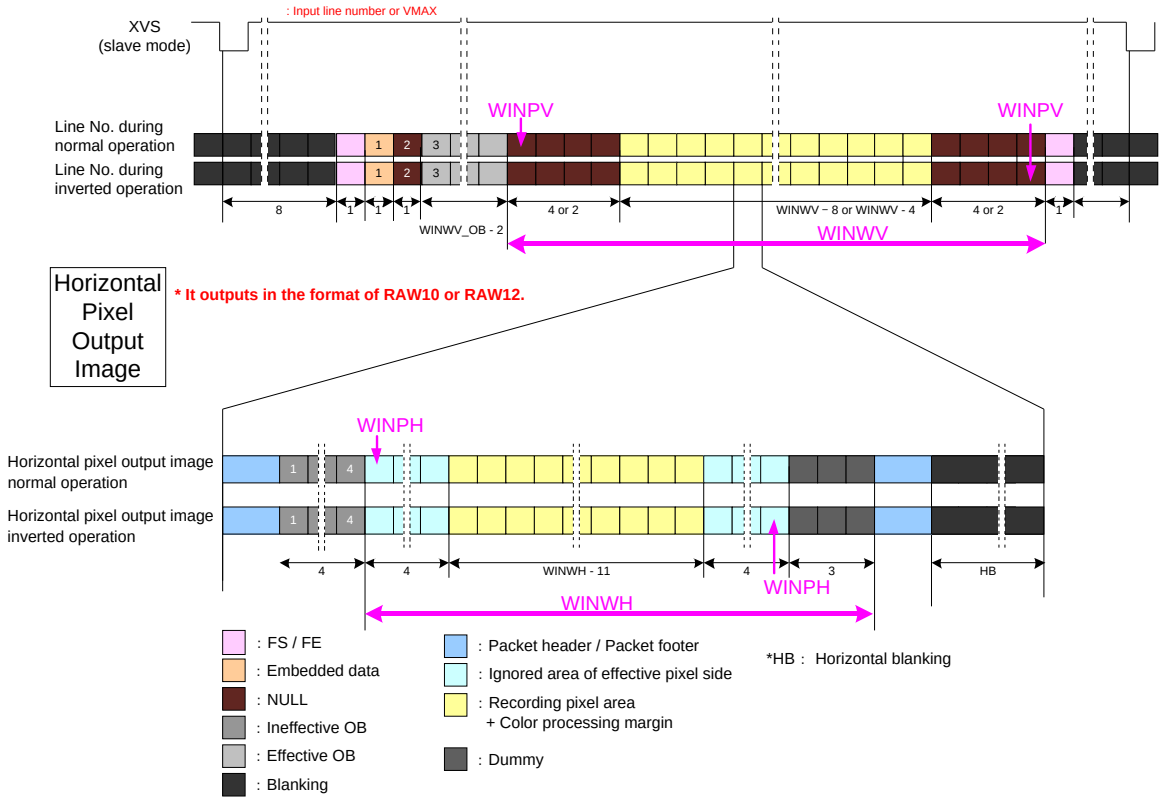
Frame rate [frame/s] = 1 / (("Number of lines per frame" or VMAX) × (1 H period))

1 H period (unit: [µs]) : Fix 1 H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

TENTATIVE



Pixel Array Image Drawing in Window cropping Mode (CSI-2 Output)



Drive Timing Chart for CSI-2 Serial Output in Window cropping Mode

Description of Various Function

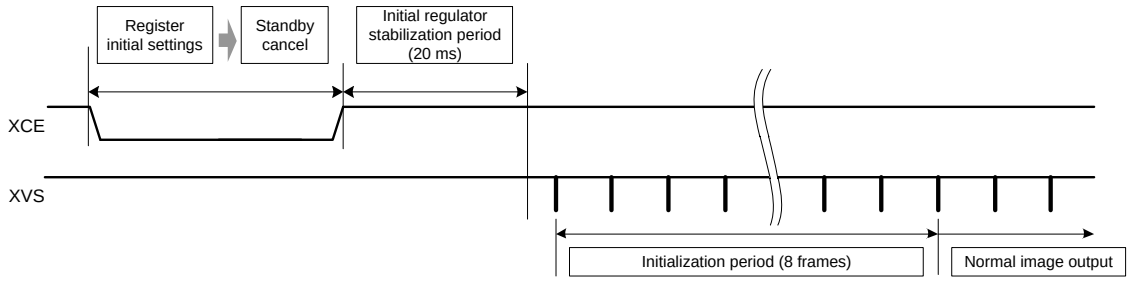
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing "1" to the standby control register STANDBY (address 00h (I^2C: 3000h), Bit [0]).
Standby mode is also established after Power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details (Chip ID = 02h)				Initial value	Setting value	Status	Remarks
	Register	Chip ID	Address ( ) : I^2C	bit				
STANDBY	—	02h	00h (3000h)	[0]	1	1	Standby	Register communication is executed even in standby mode
						0	Operating	

The serial communication registers hold the previous values.
However, the address registers transmitted in standby mode are overwritten.
The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to "0".
Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (20 ms or more).



Sequence from Standby Cancel to Stable Image Output

TENTATIVE

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal.
See the section of "Operating mode" for the number of output data line and 1H period.

Set the XMSTA register (address 02h (I^2C: 3002h) [0]) to “0” in order to start the operation after setting to master mode.
In addition, set the count number of sync signal in vertical direction by the VMAX [16:0] register (address 18h (I^2C:3018h) [7:0], 19h (I^2C: 3019h) [7:0], 1Ah (I^2C: 301Ah) [0]) and the clock number in horizontal direction by the HMAX [15:0] register (address 1Bh (I^2C: 301Bh) [7:0], 1Ch (I^2C: 301Ch) [7:0]). See the description of Operation Mode for details of the section of “Operating Modes”.

Slave and Master Mode Setting

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master Mode	High: OV_{DD} Low: GND
	High fixed	Slave Mode	

Registers that Requires Setting in Master Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I^2C	bit			
XMSTA	—	02h (3002h)	[0]	1	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [16:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h (1125d)	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	19h (3019h)	[7:0]			
	VMAX [16]	1Ah (301Ah)	[0]			
HMAX [15:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	0898h (2200d)	See the item of each drive mode.	Clock number per line designated
	HMAX [15:8]	1Ch (301Ch)	[7:0]			
XVSLNG [1:0]	XVSLNG [1:0]	46h (3046h)	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS width designated
XHSLNG [1:0]	XHSLNG [1:0]	47h (3047h)	[5:4]	0h	0: Min. to 3: Max. See the next page.	XHS width designated
XVSOUTSEL [1:0]	—	49h (3049h)	[1:0]	0h	0: High level output 2: VSYNC output Others: Setting prohibited	
XHSOUTSEL [1:0]	—		[3:2]	0h	0: High level output 2: HSYNC output Others: Setting prohibited	

TENTATIVE

Detailed Register Setting of XHSLNG

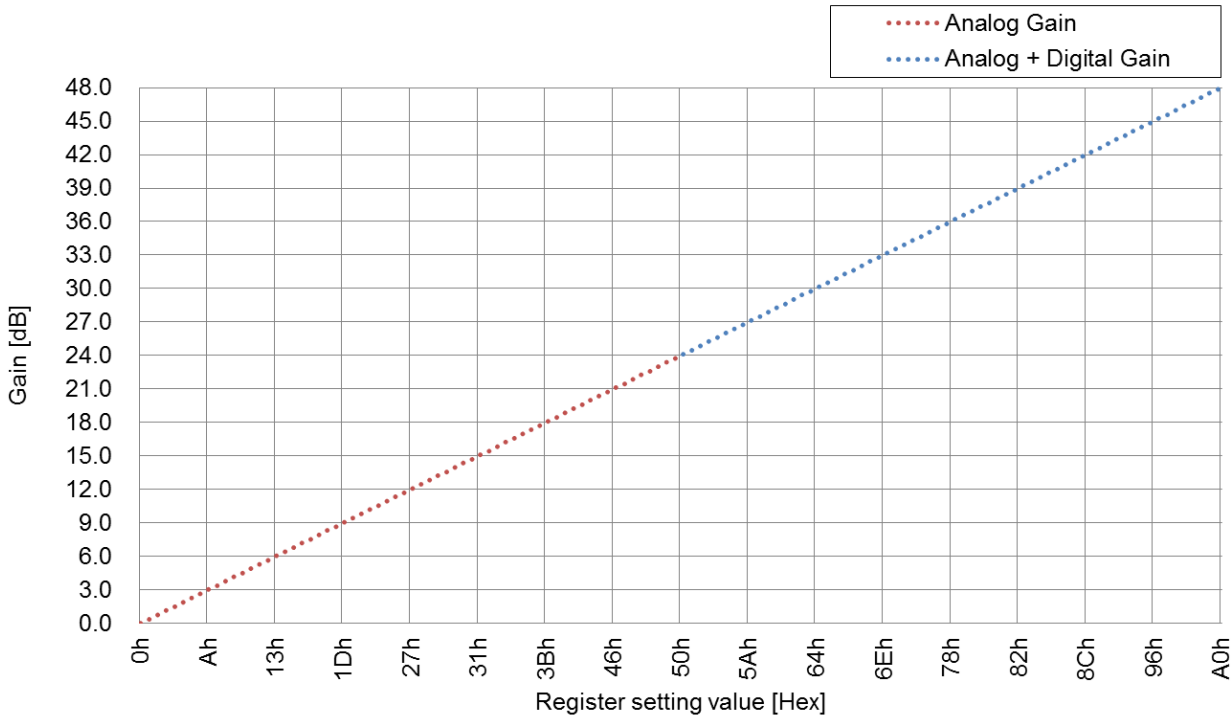
Register name ChipID = 02h	Setting value	Output Low Level Width	Reference Clock	
			Low-voltage LVDS Parallel	Low-voltage LVDS Serial / CSI-2 Serial Output
XHSLNG [1:0]	0	16 × (1 / Clock)	148.5 MHz	74.25 MHz
	1	32 × (1 / Clock)		
	2	64 × (1 / Clock)		
	3	128 × (1 / Clock)		

TENTATIVE

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [7:0] register (address 14h (I^2C: 3014h) [7:0]) setting. The same setting is applied in all colors.

See the List of Gain Setting Register Value for Each Register.



List of PGC Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I^2C	bit		Setting range	
GAIN [7:0]	—	14h (3014h)	[7:0]	00h	00h-A0h (0d-160d)	See next page.

TENTATIVE

List of Gain Setting Register Value

Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]
0.0	0h	16.2	36h	32.4	6Ch
0.3	1h	16.5	37h	32.7	6Dh
0.6	2h	16.8	38h	33.0	6Eh
0.9	3h	17.1	39h	33.3	6Fh
1.2	4h	17.4	3Ah	33.6	70h
1.5	5h	17.7	3Bh	33.9	71h
1.8	6h	18.0	3Ch	34.2	72h
2.1	7h	18.3	3Dh	34.5	73h
2.4	8h	18.6	3Eh	34.8	74h
2.7	9h	18.9	3Fh	35.1	75h
3.0	Ah	19.2	40h	35.4	76h
3.3	Bh	19.5	41h	35.7	77h
3.6	Ch	19.8	42h	36.0	78h
3.9	Dh	20.1	43h	36.3	79h
4.2	Eh	20.4	44h	36.6	7Ah
4.5	Fh	20.7	45h	36.9	7Bh
4.8	10h	21.0	46h	37.2	7Ch
5.1	11h	21.3	47h	37.5	7Dh
5.4	12h	21.6	48h	37.8	7Eh
5.7	13h	21.9	49h	38.1	7Fh
6.0	14h	22.2	4Ah	38.4	80h
6.3	15h	22.5	4Bh	38.7	81h
6.6	16h	22.8	4Ch	39.0	82h
6.9	17h	23.1	4Dh	39.3	83h
7.2	18h	23.4	4Eh	39.6	84h
7.5	19h	23.7	4Fh	39.9	85h
7.8	1Ah	24.0	50h	40.2	86h
8.1	1Bh	24.3	51h	40.5	87h
8.4	1Ch	24.6	52h	40.8	88h
8.7	1Dh	24.9	53h	41.1	89h
9.0	1Eh	25.2	54h	41.4	8Ah
9.3	1Fh	25.5	55h	41.7	8Bh
9.6	20h	25.8	56h	42.0	8Ch
9.9	21h	26.1	57h	42.3	8Dh
10.2	22h	26.4	58h	42.6	8Eh
10.5	23h	26.7	59h	42.9	8Fh
10.8	24h	27.0	5Ah	43.2	90h
11.1	25h	27.3	5Bh	43.5	91h
11.4	26h	27.6	5Ch	43.8	92h
11.7	27h	27.9	5Dh	44.1	93h
12.0	28h	28.2	5Eh	44.4	94h
12.3	29h	28.5	5Fh	44.7	95h
12.6	2Ah	28.8	60h	45.0	96h
12.9	2Bh	29.1	61h	45.3	97h
13.2	2Ch	29.4	62h	45.6	98h
13.5	2Dh	29.7	63h	45.9	99h
13.8	2Eh	30.0	64h	46.2	9Ah
14.1	2Fh	30.3	65h	46.5	9Bh
14.4	30h	30.6	66h	46.8	9Ch
14.7	31h	30.9	67h	47.1	9Dh
15.0	32h	31.2	68h	47.4	9Eh
15.3	33h	31.5	69h	47.7	9Fh
15.6	34h	31.8	6Ah	48.0	A0h
15.9	35h	32.1	6Bh	—	—

TENTATIVE

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [8:0] register (address: 0Ah (I^2C: 300Ah) [7:0], 0Bh (I^2C: 300Bh) [0]). When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

Use with values shown below is recommended.
10-bit output: 03Ch (60d)
12-bit output: 0F0h (240d)

List of Black Level Adjustment Register

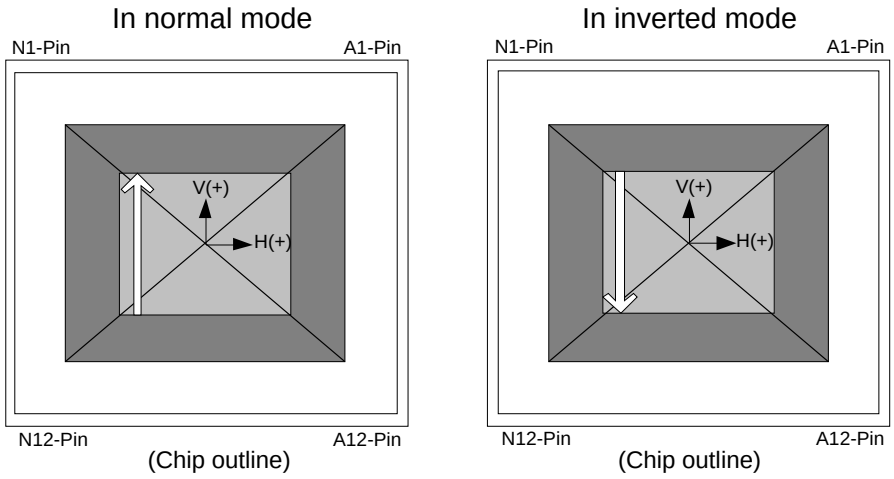
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
BLKLEVEL [8:0]	BLKLEVEL [7:0]	0Ah (300Ah)	[7:0]	0F0h	000h to 1FFh
	BLKLEVEL [8]	0Bh (300Bh)	[0]		

Vertical Normal Operation and Inverted Drive

The sensor readout direction (normal/inverted) in vertical direction can be switched by the VREVERSE (address 07h (I^2C: 3007h) [0]) register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Vertical Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
VREVERSE	—	07h (3007h)	[0]	0h	0: Normal (Initial value) 1: Inverted



Normal and Inverted Drive Outline in Vertical Direction (Top View)

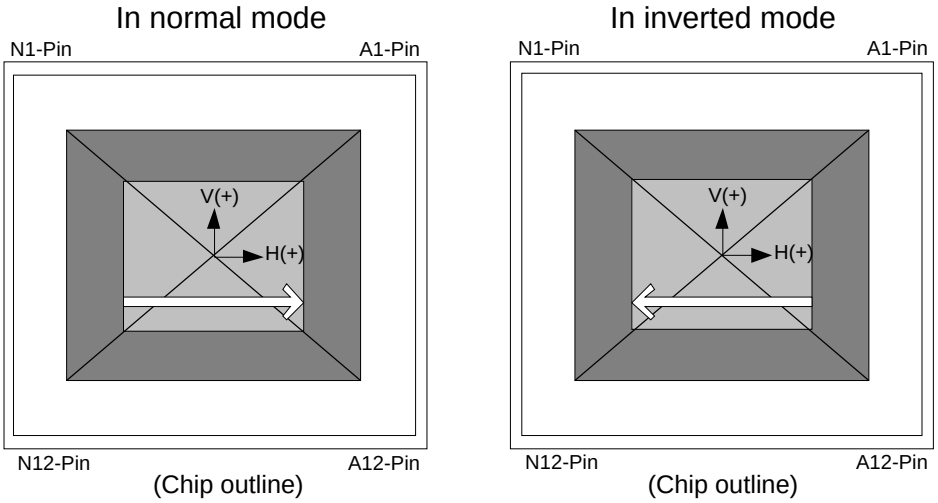
TENTATIVE

Horizontal Normal Operation and Inverted Drive

The sensor readout direction (normal/inverted) in vertical direction can be switched by the HREVERSE (address 07h (I^2C: 3007h) [1]) register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes.

List of Horizontal Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
HREVERSE	—	07h (3007h)	[1]	0h	0: Normal (Initial value) 1: Inverted



Normal and Inverted Drive Outline in Horizontal Direction (Top View)

TENTATIVE

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1 + 1) × (1H period) + t_{OFFSET}

Note) 1. The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
2. See “Operating Modes” for the 1H period.
3. t_{OFFSET} is 2.64 [µs] (10 bit output) or 3.85 [µs] (12 bit output).

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

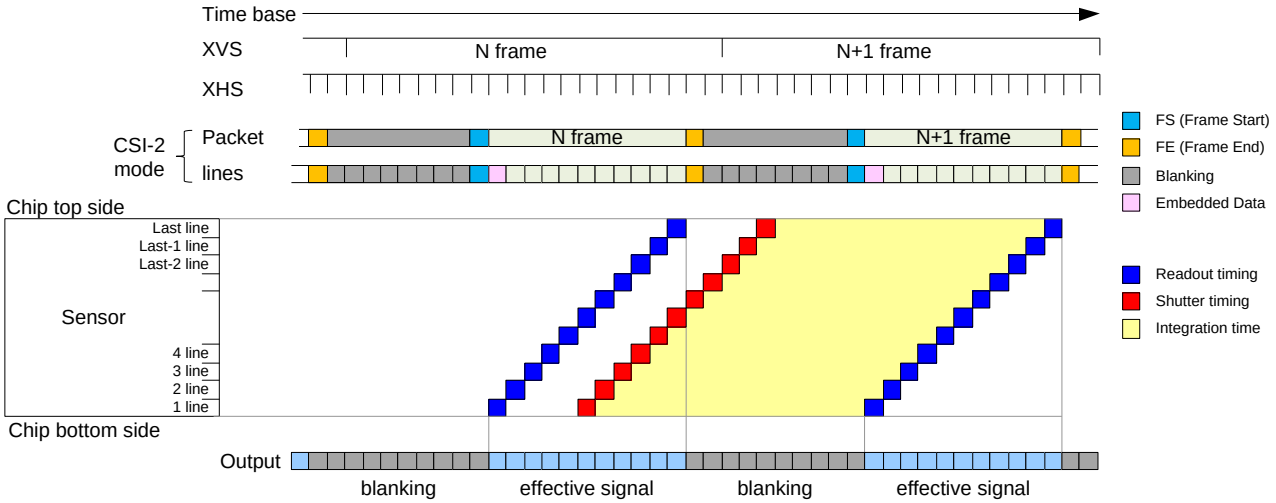


Image Drawing of Shutter Operation

TENTATIVE

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 [16:0] register (address: 20h (I^2C: 3020h) [7:0], 21h (I^2C: 3021h) [7:0], 22h (I^2C: 3022h) [0]).

Set SHS1 [16:0] to a value between 0 and (Number of lines per frame - 2). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register (address: 18h (I^2C: 3018h) [7:0], 19h (I^2C: 3019h) [7:0], 1Ah (I^2C: 301Ah) [0]).
The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
SHS1 [16:0]	SHS1 [7:0]	20h (3020h)	[7:0]	00000h	Set the shutter sweep time. 0 to (Number of lines per frame - 2) *(Number of lines per frame - 1) : Setting prohibited
	SHS1 [15:8]	21h (3021h)	[7:0]		
	SHS1 [16]	22h (3022h)	[0]		
VMAX [16:0]	VMAX [7:0]	18h (3018h)	[7:0]	00465h	Set the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	19h (3019h)	[7:0]		
	VMAX [16]	1Ah (301Ah)	[0]		

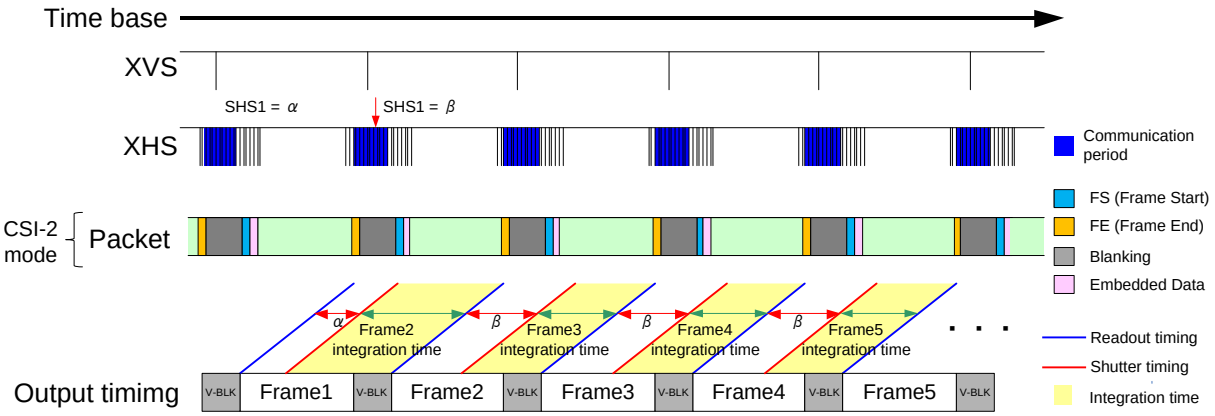


Image Drawing of Integration Time Control within a Frame

TENTATIVE

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [16:0] (address: 18h (I^2C: 3018h) [7:0], 19h (I^2C: 3019h) [7:0], 1Ah (I^2C: 301Ah) [0]) value compared to normal operation.
When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

The maximum VMAX value is 131071d, and the maximum SHS1 value is 131069d. When the number of lines per frame is set to the maximum value, the integration time in 1080p-HD mode at 120 frame/s is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

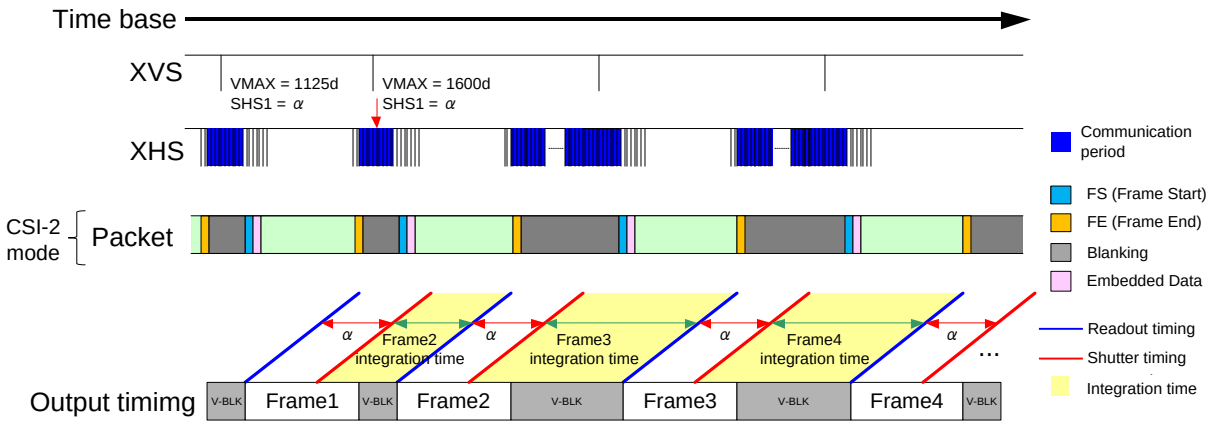


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

TENTATIVE

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Setting (2.3 M pixels in all-pixel mode at 100 frame/s)

Operation	Sensor setting (register)		Integration time
	VMAX*	SHS1**	
Normal frame rate	1320	1318	1H + t_{OFFSET}
		⋮	⋮
		N	(1320 - (N + 1)) H + t_{OFFSET}
		⋮	⋮
		1	1318H + t_{OFFSET}
		0	1319H + t_{OFFSET}
Long-time exposure operation	M	N	(M - (N + 1)) H + t_{OFFSET}

* In sensor master mode. In slave mode, the interval is same as XVS input.
** The SHS1 setting value (N) is set between “0” and “the VMAX value (M) – 2”.

TENTATIVE

Signal Output

Output Pin Settings

The output formats of this sensor support the following modes.

Low voltage LVDS parallel DDR output
Low voltage LVDS serial (2 ch / 4 ch switching) DDR output
CSI-2 serial data output (2 Lane / 4 Lane, RAW10/RAW12 output)

The switching is made by the OMODE pin. Establish the OMODE pin status before canceling the system reset. (Do not switch this pin status during operation.)

Settings OMODE pin for Output Format

Pin name	Pin processing	Operation mode	Remarks
OMODE pin	High fixed	Low voltage LVDS parallel DDR output / Low voltage LVDS serial DDR output	High: OV_{DD} Low: GND
	Low fixed	CSI-2 serial data output	

Each mode is set using the register OPORTSEL [3:0] (Address: 44h (I^2C: 3044h) [7:4]). The table below shows the output format settings.

Settings Register for Output Format

Register name	Register details (Chip ID = 02h)		Initial value	Setting value	Description
	Address ( ) : I^2C	bit			
OPORTSEL [3:0]	44h (3044h)	[7:4]	Eh	6h	Low voltage LVDS parallel DDR output
				Dh	Low voltage LVDS serial 2 ch DDR output
				Eh	Low voltage LVDS serial 4 ch DDR output / CSI-2 serial data output

Each output pin is shown in the table below when setting low-voltage LVDS serial 2 ch/4 ch output.

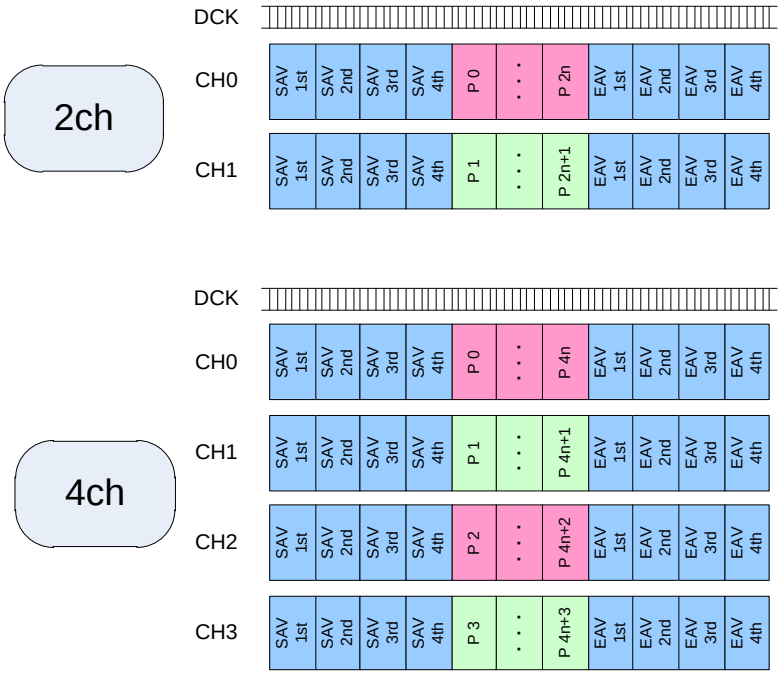
Output Pins for Low voltage LVDS Serial mode

DOP/DOM	Low voltage LVDS serial DDR output	
	2 ch	4 ch
DOP11 to 8 / DOM11 to 8	Hi-Z	Hi-Z
DOP7 / DOM7	Hi-Z	CH4
DOP6 / DOM6	CH2	CH2
DOP5 / DOM5	CH1	CH1
DOP4 / DOM4	Hi-Z	CH3
DOP3 to 0 / DOM3 to 0	Hi-Z	Hi-Z

TENTATIVE

Low-voltage LVDS serial 2 ch/4 ch output format is shown in the figure below.

When setting 2 ch, after four data of SAV is output in the order of CH0 and CH1 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH0 and CH1 respectively.
When setting 4 ch, after four data of SAV is output in the order of CH0, CH1, CH2 and CH3 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH0, CH1, CH2 and CH3 respectively.
Data is sent MSB first.
For details, see drive timing in each mode in the section of "Operation Mode".



Output Format of Low voltage LVDS Serial 2 ch/4 ch

TENTATIVE

CSI-2 serial Output Setting

The output formats of this sensor support the following modes.

CSI-2 serial data output　2 Lane / 4 Lane, RAW10 / RAW12

The 2 Lane / 4 Lane serial signal output method using the IMX185LQJ is described below.
Complied with the CSI-2 Rev.1.0, data is output using 2 Lane / 4 Lane.
The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal, the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DMCKP/DMCKN of the CSI-2 pins.
In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4. The bit rate maximum value is 444.5 Mbps/Lane.

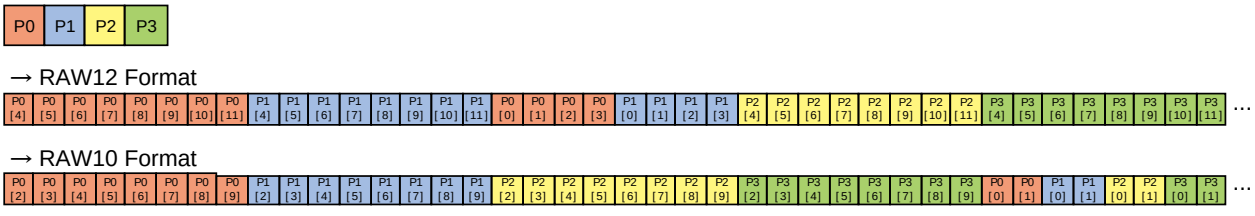
The select of RAW10 / RAW12 is set by the register: CSI_DT_FMT [15:0] (address: (Chip ID05h) : 3Eh (I^2C : 333Eh) [7:0], 3Fh (I^2C : 333Fh) [7:0]).

The number of output lanes is set by the register: CSI_Lane_MODE [1:0] (address: (Chip ID05h) : 40h (I^2C: 3340h) [1:0]). The number of lanes physically connected is set by PHYSICAL_Lane_NUM [1:0] (address: (Chip ID05h) : 05h (I^2C: 3305h) [1:0]).
Unused lanes (when setting 2 lanes; DMO3P/DMO3N, DMO4P/DMO4N) are set to Hi-Z output by the setting.
When the number of lanes more than CSI_Lane_MODE is set by PHYSICAL_Lane_NUM, unused lanes output signals conformed to MIPI standard.

Settings for Output Format

Register name	Register details (Chip ID = 05h)			Initial value	Setting value	Function	Remarks
	Register	Address ( ) : I^2C	bit				
CSI_DT_FMT [15:0]	CSI_DT_FMT [7:0]	3Eh (333Eh)	[7:0]	0C0Ch	0A0Ah	RAW10	
	CSI_DT_FMT [15:8]	3Fh (333Fh)	[7:0]		0C0Ch	RAW12	
PHYSICAL_Lane _NUM [1:0]	—	05h (3305h)	[1:0]	3	1	2 Lane	0,2: Setting prohibited
					3	4 Lane	
CSI_Lane _MODE [1:0]	—	40h (3340h)	[1:0]	3	1	2 Lane	0,2: Setting prohibited
					3	4 Lane	

The formats of RAW12 and RAW10 are shown below.

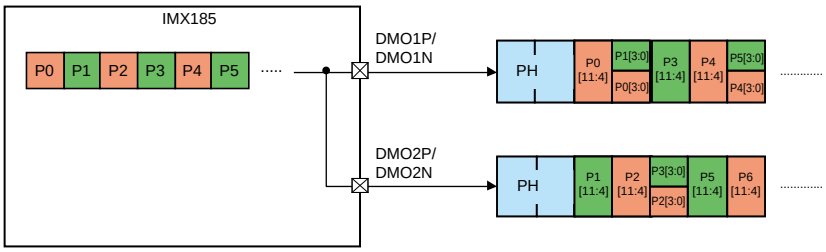


The example of formats of RAW12 and RAW10

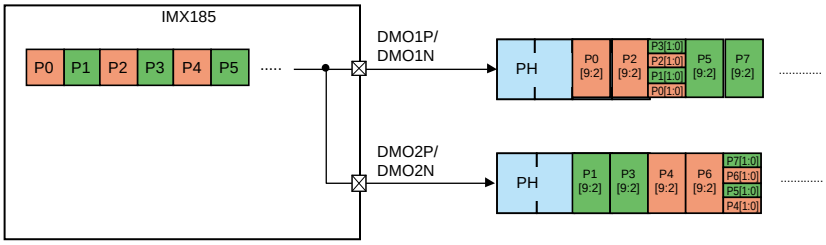
TENTATIVE

The each formal of 2 Lane and 4 Lane are shown below.

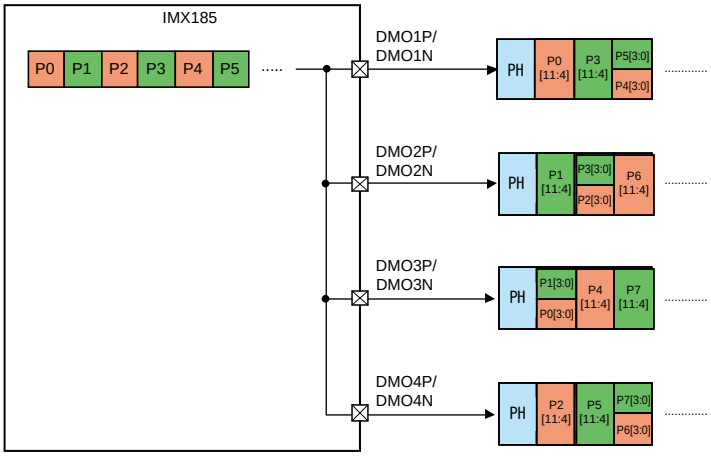
a) 2 Lane-RAW12



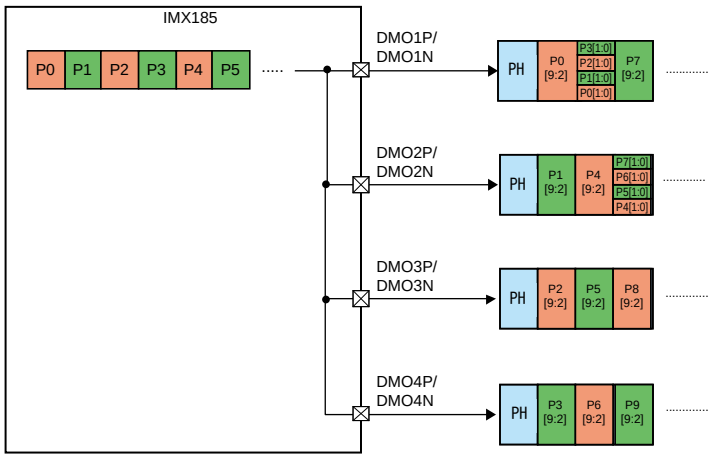
b) 2 Lane-RAW10



c) 4 Lane-RAW12



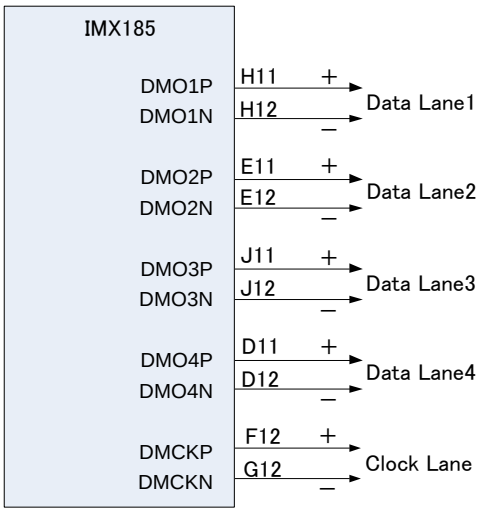
d) 4 Lane-RAW10



Output Format of 2 Lane / 4 Lane

MIPI Transmitter

Output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DMCKP, DMCKN) are described in this section.

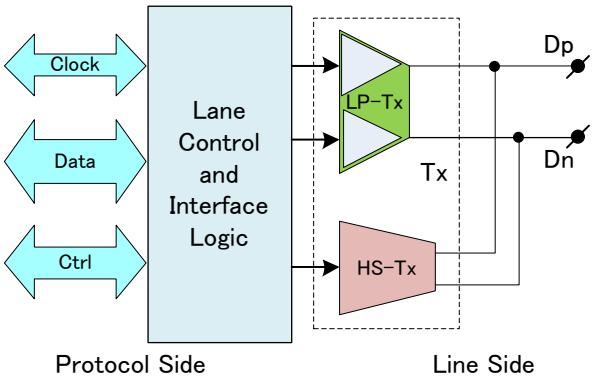


Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard

- MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01.00
- MIPI Alliance Specification for D-PHY Version 0.90.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Reciever side. When inserting an external resistor, as close as possible to the Receiver.
The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 445.5 Mbps/Lane.



Universal Lane Module Functions

TENTATIVE

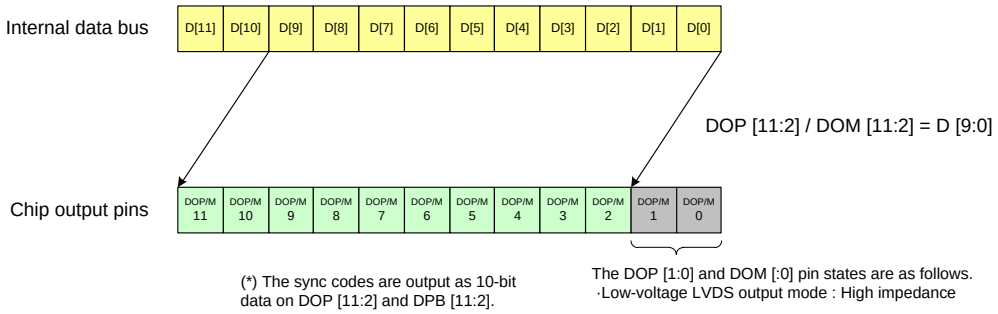
Output Pin Bit Width Selection (Low voltage LVDS output)

The output pin width can be selected from 10 bit or 12 bit output using the register ODBIT (address 44h (I^2C: 3044h), bit [0]).
In parallel output mode, when ODBIT = 0 (10 bit output), the lower 2 bits are high impedance in low voltage LVDS output mode. Therefore, when using only 10 bit, the pins corresponding to the lower 2 bits can be left open on the board by setting ODBIT = 0.
When low voltage LVDS serial output, continuous data is output MSB first by 10 bit and 12 bit output setting respectively.
10 bits sync code are output when ODBIT = 0 (10 bit output), and 12 bit sync codes are output when ODBIT = 1 (12 bit output).

Output Pin Bit Width Selection Setting Register

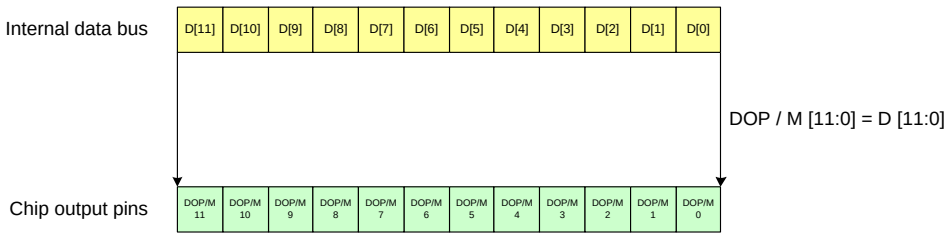
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
ODBIT	—	44h (3044h)	[0]	1h	0: 10 bit 1: 12 bit

ODBIT = 0 (parallel 10 bit output)
The lower 10 bits of the internal data bus are output with left justified on the chip output pins DO.



Bit Assignments in Parallel 10 bit Output Mode

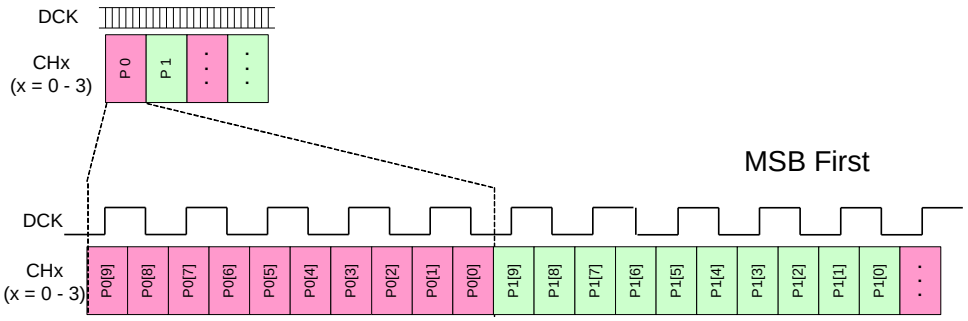
ODBIT = 1 (parallel 12 bit output)
The lower 12 bits of the internal data bus are output on the chip output pins DO.



Bit Assignments in Parallel 12 bit Output Mode

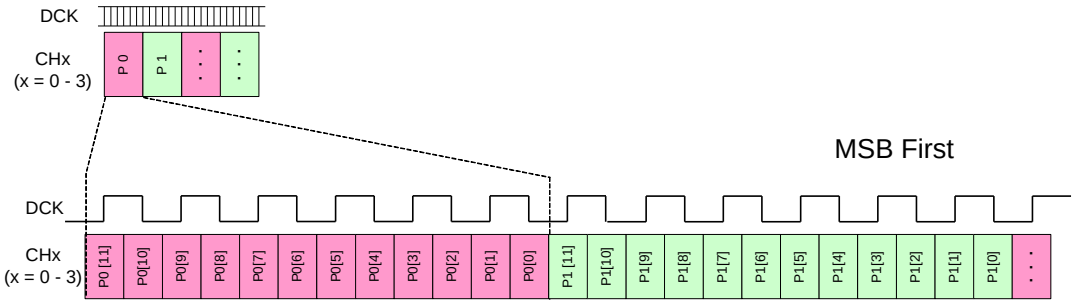
TENTATIVE

ODBIT = 0 (low voltage LVDS serial 10 bit output)



Example of Data format in low voltage LVDS serial 10 bit output

ODBIT = 1 (low voltage LVDS serial 12 bit output)



Example of Data format in low voltage LVDS serial 12 bit output

TENTATIVE

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bit or 12 bit by the register ADBIT (address 05h (I^2C: 3005h), bit [0]). See the section of “Operating Modes” for the correspondence with each mode.
12 bit right justified output is possible by setting 12 bit to only output width under the condition of ODBIT = 1 in the mode of ADBIT = 0 (10 bit setting).

In LVDS output mode, 12 bit right justified output is possible by setting 12 bit to only output width under the condition of ODBIT = 1 in the mode of ADBIT = 0 (10 bit setting).

Internal A/D Conversion Resolution Setting (LVDS / CSI-2 Output)

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
ADBIT	—	05h (3005h)	[0]	1h	0: 10 bit 1: 12 bit

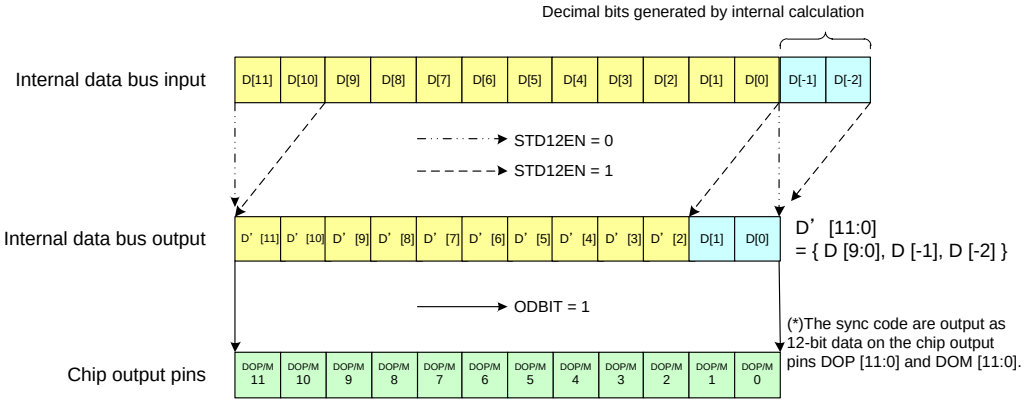
TENTATIVE

Output Bit Shift (Low voltage LVDS output)

When internal A/D conversion is set to 10 bit mode (ADBIT = 0h), the sensor has a function that shifts the sensor internal 10 bit data by 2 bits to the MSB side and outputs by register STD12EN address 05h (I^2C: 3005h), bit [4]). This time, the register ODBIT is set to 1 (12 bit output), 2 decimal bits generated by the internal calculation are output in the 2 LSB side bits.
The output consists of upper 10 bits (step accuracy) and lower 2 bits (remainder). The step accuracy is equivalent to 10 bit.
When the register STD12EN is set to 1 (bit shift), 12 bit sync codes are output on the chip output pins DOP [11:0] and DOM [11:0].

Bit Shift Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
STD12EN	—	05h (3005h)	[4]	0h	0: No bit shift 1: 2 bits shift to MSB side



Bit Assignment when 12 bit Shift is Set

TENTATIVE

Output Rate Setting

The sensor output rate is determined uniformly by the sensor operating mode and the output format. See the section of “Operating Modes” for the relationship between each setting and the frame rate, data rate and data bit rate.
The registers related to mode setting are shown in the table below.

Related Registers for Setting Operation Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
MODE [5:0]	—-	06h (3006h)	[5:0]	00h	00h: All-pix scan mode 33h: Horizontal / vertical 2/2-line bining readout mode Others: Setting prohibited
WINMODE [3:0]	—	07h (3007h)	[7:4]	1h	Window mode setting 0: WUXGA mode 1: 1080p mode 2: 720p mode 4: Window cropping mode (from WUXGA mode) 5: Window cropping mode (from 1080p mode) 6: Window cropping mode (from 720p mode)
FRSEL [1:0]	—	09h (3009h)	[1:0]	2h	Frame rate grade setting 0: High speed mode, 1: Middle speed mode, 2: Low speed mode 3: Setting prohibited See the detailed description in register list for each mode

Output Signal Range

In LVDS output mode, the sensor output has either a 10 bit or 12 bit gradation, but output is not performed over the full range, and the maximum output value is the (3FFh -1) value (10 bit output) and the (FFFh -1) one (12 bit output). When serial output, the minimum value is 001h. The output range for each output gradation is shown in the table below.
See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range (LVDS Output)

Output gradation	Output value		
	Min.		Max.
	Parallel output	Serial output	
10 bit	000h	001h	3FEh
12 bit	000h	001h	FFEh

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, but output is not performed over the full range, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

TENTATIVE

INCK Setting

The available operation mode varies according to INCK frequency. Input either 27 MHz or 54 MHz or 37.125 MHz or 74.25 MHz for INCK frequency. The value according to the combination of input INCK and output format is set to register INCKSEL1, INCKSEL2, INCKSEL3, INCKSEL4, INCKSEL5, INCK_FREQ and INCK_FREQ2.
Do not change these register values during sensor operation. These regisiter should be set up at the power on sequence.
The register setting of INCK_FREQ and INCK_FREQ2 is only for CSI-2 output mode.
The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register (Low-voltage LVDS Parallel / Serial output)

Register name	Register details			Initial value	Low-voltage LVDS Parallel				Low-voltage LVDS Serial			
	Register	Address [HEX] () : I²C	bit		INCK = 37.125 [MHz]	INCK = 27 [MHz]	INCK = 72.25 [MHz]	INCK = 54 [MHz]	INCK = 37.125 [MHz]	INCK = 27 [MHz]	INCK = 72.25 [MHz]	INCK = 54 [MHz]
		ChipID ; 02h										
INCKSEL1 [7:0]	—	5C (305C)	[7:0]	20h	20h	2Ch	20h	2Ch	20h	2Ch	20h	2Ch
INCKSEL2 [7:0]	—	5D (305CD	[7:0]	00h	00h	00h	10h	10h	00h	00h	10h	10h
INCKSEL3 [7:0]	—	5E (305E)	[7:0]	18h	20h	2Ch	20h	2Ch	18h	21h	18h	21h
INCKSEL4 [7:0]	—	5F (305F)	[7:0]	00h	00h	00h	10h	10h	00h	00h	10h	10h
INCKSEL5 [7:0]	—	63 (3063)	[7:0]	E8h	74h	54h	E8h	A8h	74h	54h	E8h	A8h

INCK Setting Register (CSI-2 Serial output)

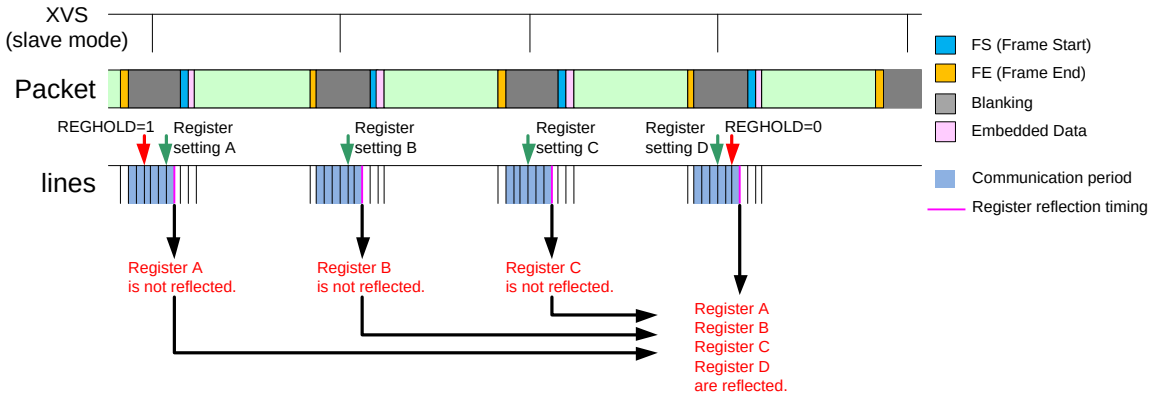
Register name	Register details			Initial value	CSI-2 Serial Output			
	Register	Address [HEX] () : I²C	bit		INCK = 37.125 [MHz]	INCK = 27 [MHz]	INCK = 72.25 [MHz]	INCK = 54 [MHz]
		ChipID ; 02h						
INCKSEL1 [7:0]	—	5C (305C)	[7:0]	20h	20h	2Ch	20h	2Ch
INCKSEL2 [7:0]	—	5D (305CD	[7:0]	00h	00h	00h	10h	10h
INCKSEL3 [7:0]	—	5E (305E)	[7:0]	18h	18h	21h	18h	21h
INCKSEL4 [7:0]	—	5F (305F)	[7:0]	00h	00h	00h	10h	10h
INCKSEL5 [7:0]	—	63 (3063)	[7:0]	E8h	74h	54h	E8h	A8h
		ChipID ; 05h						
INCK_FREQ [15:0]	INCK_FREQ [7:0]	41 (3341)	[7:0]	2520h	2520h	1B00h	4A40h	3600h
	INCK_FREQ [15:8]	42 (3342)	[7:0]					
INCK_FREQ2 [10:0]	INCK_FREQ2 [7:0]	4E (334E)	[7:0]	367h	1B4h	13Dh	367h	279h
	INCK_FREQ2 [10:8]	4F (334F)	[2:0]					

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD (address: 01h (I2C: 3001h) [0]). Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
REGHOLD	—	01h (3001h)	[0]	0h	0: Invalid 1: Valid (register hold)



Register Hold Setting

TENTATIVE

Software Reset (Low voltage LVDS output)

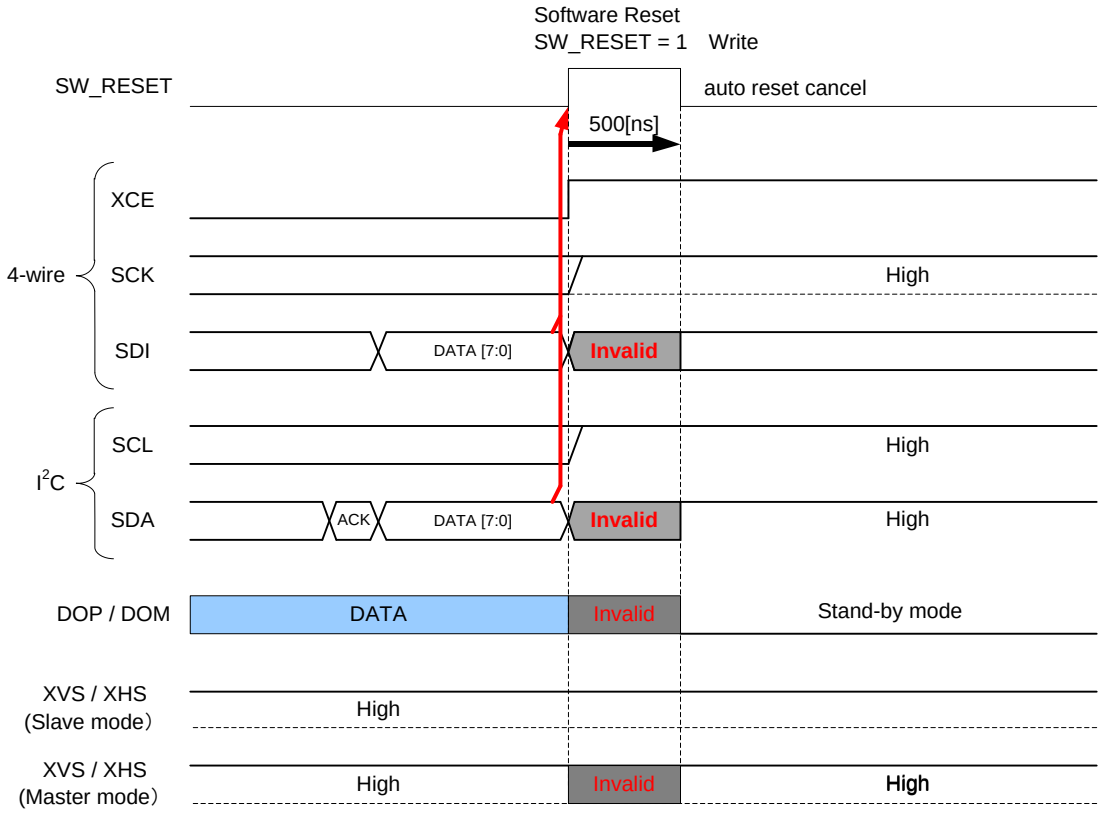
This function is prohibited in CSI-2 output mode.
Software reset can be performed by register setting using the register SW_RESET (address: 03h (I^2C: 3003h) [0]).
Sensor reset is performed by setting SW_RESET = 1. However, the communication to continuous address cannot use. In I2C communication, sensor not return ACK when SW_RESET is transferred.

The registers become initial state and standby 500 ns after setting SW_RESET = 1.
The SW_RESET signal returns to "0" automatically.

The XVS and XHS output High in master mode.
Input High to the XVS and XHS before setting SW_RESET = 1 in slave mode.
Follow the sequence in the item of "Standby Mode" to perform register initial setting and standby cancel from standby state.

Software Reset Register Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
SW_RESET	—	03h (3003h)	[0]	0h	0: Normal operation 1: Reset



Software Reset

TENTATIVE

Mode Transitions (Low-voltage LVDS output)

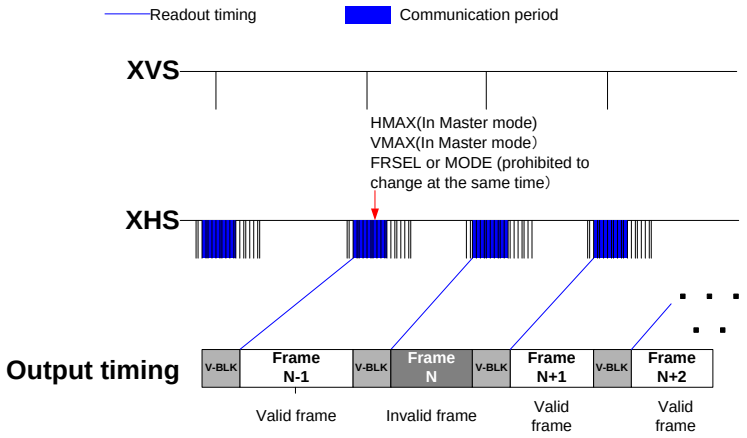
When changing the operating mode during sensor drive operation, first set the sensor to all-pixel scan mode, and then it again to the desired operating mode.
An invalid frame is generated during mode transition.
An invalid frame is generated as well as when changing frame rate in the same operating mode.
The table below shows the number of invalid frames generated by transition between the various modes.
Data is output from sensor during the invalid frame period, but the output values may reflect the integration time or may not be uniform on the screen, or a partially saturated image may be output,

Operating mode (register MODE [5:0]) and frame rate grade setting (register FRSEL [1:0]) cannot be changed at the same time. They must be set at respective frames, and an invalid frame is generated in each mode transition.
In addition, especially when INCK frequency (register INCKSEL1-5), output bit width (register ODBIT) or output format (register OPORTSEL [3:0]) is changed, transition of the operating mode must be done via sensor standby.
When INCK frequency is changed, care should be taken not to be input pulses whose width is shorter than the High/Low level width in front and behind of the INCK pulse at the frequency change.
If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on /off sequence". Execute initial setting again because the register settings become default state after system clear.

Number of Invalid Frames Generated during Mode Transitions

Mode transition			Number of invalid frames
All-pixel scan mode	→	1080p-HD mode	1
All-pixel scan mode	→	Horizontal / vertical 2/2-line bining readout mode	
All-pixel scan mode	→	Window cropping mode	
1080p-HD mode	→	All-pixel scan mode	
Horizontal / vertical 2/2-line bining readout mode	→	All-pixel scan mode	
Window cropping mode	→	All-pixel scan mode	
All-pixel scan mode Horizontal / vertical 2/2-line bining readout mode 1080p-HD mode	→	Same operation mode Frame rate grade change (Note 1)	

(Note 1) Excluded when changing input INCK frequency or the register ODBIT or OPORTSEL [3:0].



* When changing the drive mode also changes the frame period, the number of invalid frames is counted according to the frame period after the change.

Mode Transitions

Mode Transitions (CSI-2 Serial output)

When changing an operating mode during sensor drive, always start operation according to standby cancel sequence after changing the mode during the standby period via sensor standby.
Also when changing the number of Lanes, frame rate and cropping size in Window cropping mode during the same mode, always start operation via sensor standby.

In addition, especially when INCK frequency (register INCKSEL1-5, INCK_FREQ and INCK_FREQ2) is changed, transition of the operating mode must be done via sensor standby.
When INCK frequency is changed, care should be taken not to be input pulses whose width are shorter than the High/Low level width in front and behind of the INCK pulse at the frequency change.
If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Power-on and Power-off Sequences

Power-on Sequence

Follow the sequence below to turn on the power supplies.

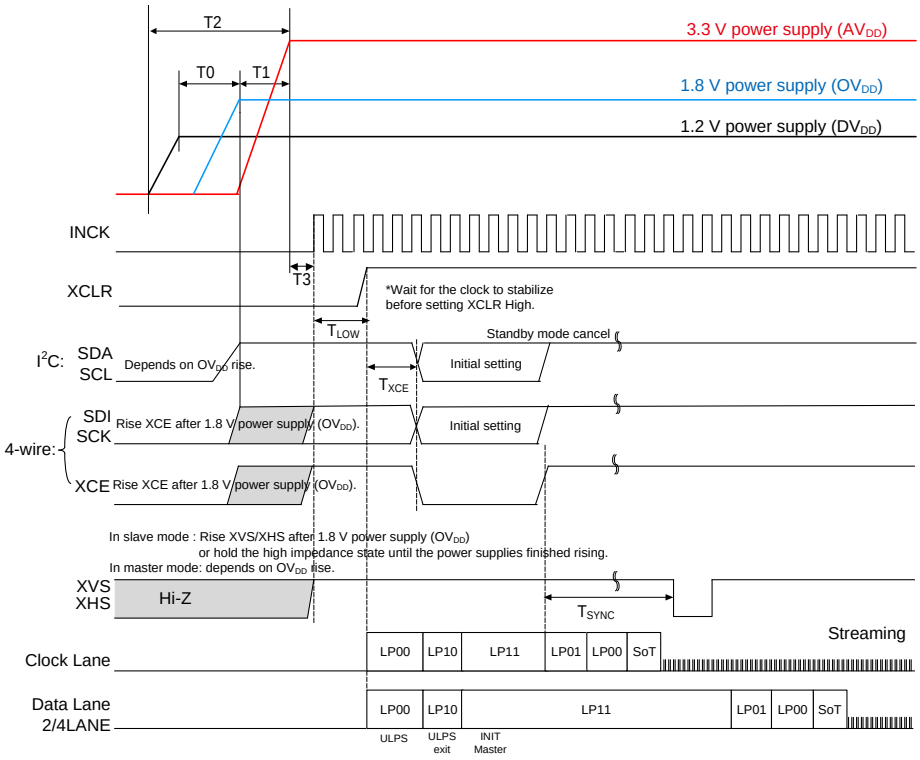
(1) Turn on the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.

(2) Start master clock (INCK) input after turning on the power supplies.

(3) The register values are undefined just after Power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
The system clear is applied by setting XCLR to High level. However, the master clock needs to stabilize before setting the XCLR pin to High level.
After the system clear, Clock Lane (DCK) and Data Lane (Lane1 to 4) are LP00 state.

(4) After 20 µs from the system clear, register communication can be set.

(5) Make the sensor setting by register communication. In case of 4-wire serial control, a period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In case of I^2C serial control, XCE is fixed to High level. After standby mode cancel, when the sensor drive slave mode, input XVS and XHS over 20 ms.



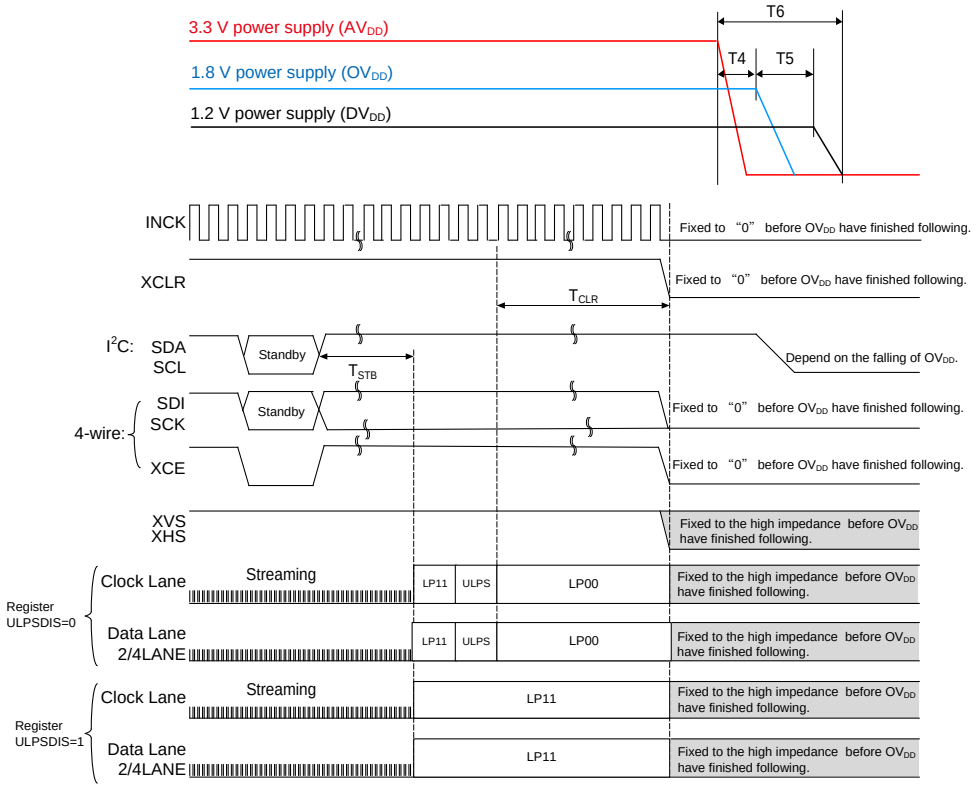
Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T_0	0	—	ns
1.8 V power supply rising → 3.3 V power supply rising	T_1	0	—	ns
Rising time of all power supply	T_2	—	200	ms
All power supply rising → External input time of INCK	T_3	0	—	ns
INCK active → Clear OFF	T_{LOW}	500	—	ns
Clear OFF Communication start	T_{XCE}	20	—	µs
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	20	—	ms

TENTATIVE

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, DMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



Power –off Sequence

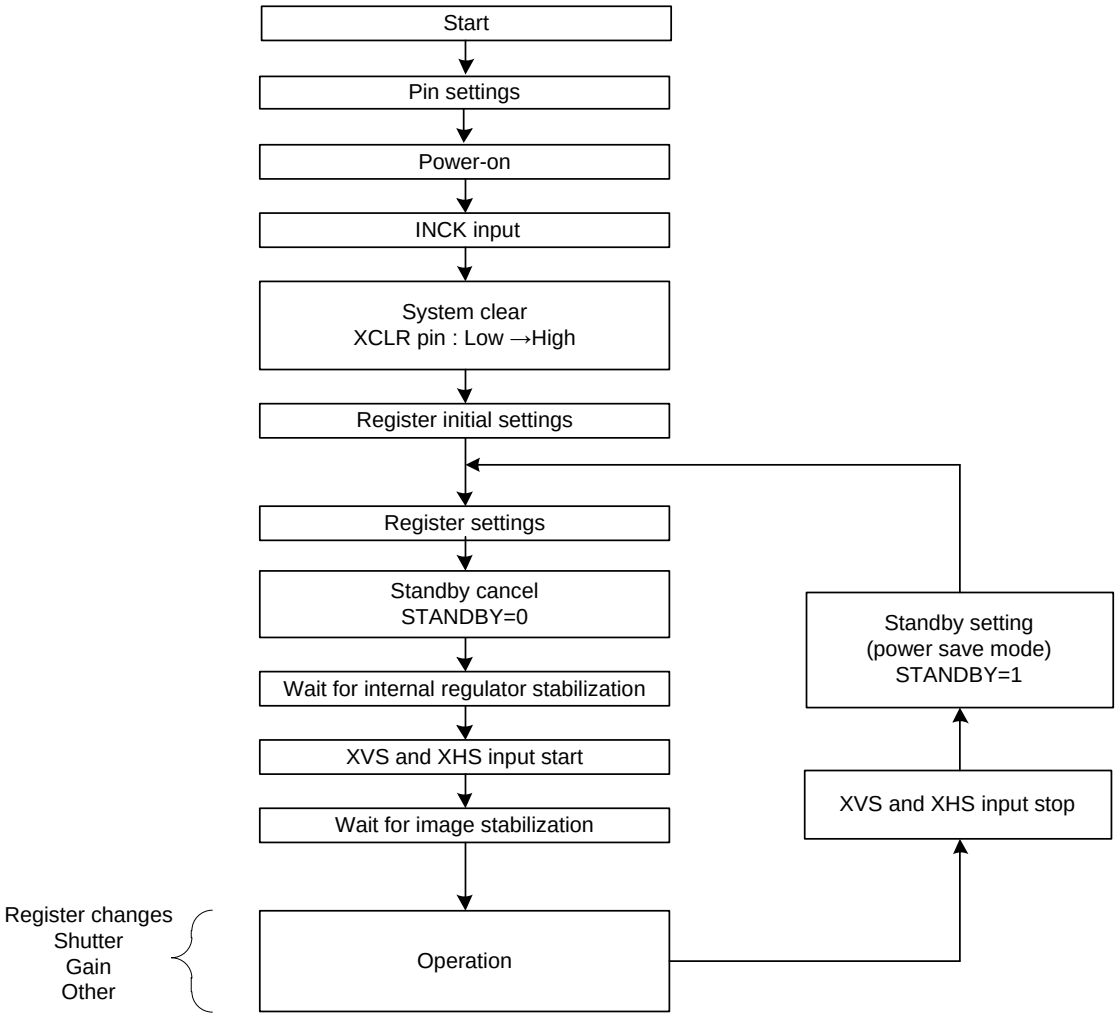
Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	Until FE		—
LP00 → XCLR falling (ULPSDIS = 0)	T_{CLR}	128	—	cycle
3.3 V power shut down → 1.8 V power shut down	T_4	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T_5	0	—	ns
Shut down time of all power supply.	T_6	—	200	ms

TENTATIVE

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.

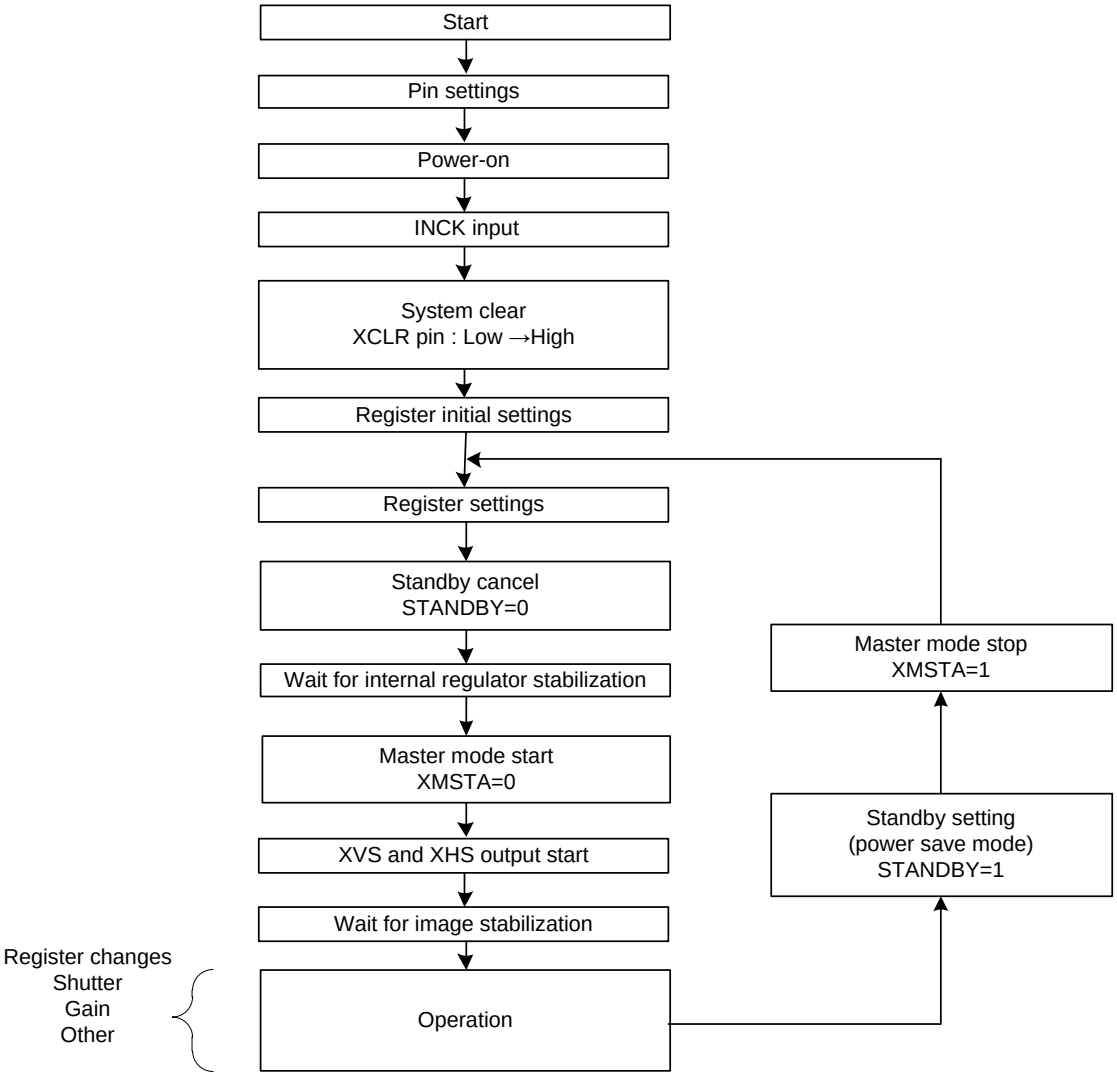


Sensor Setting Flow (Sensor Slave Mode)

TENTATIVE

Setting Flow in Sensor Master Mode

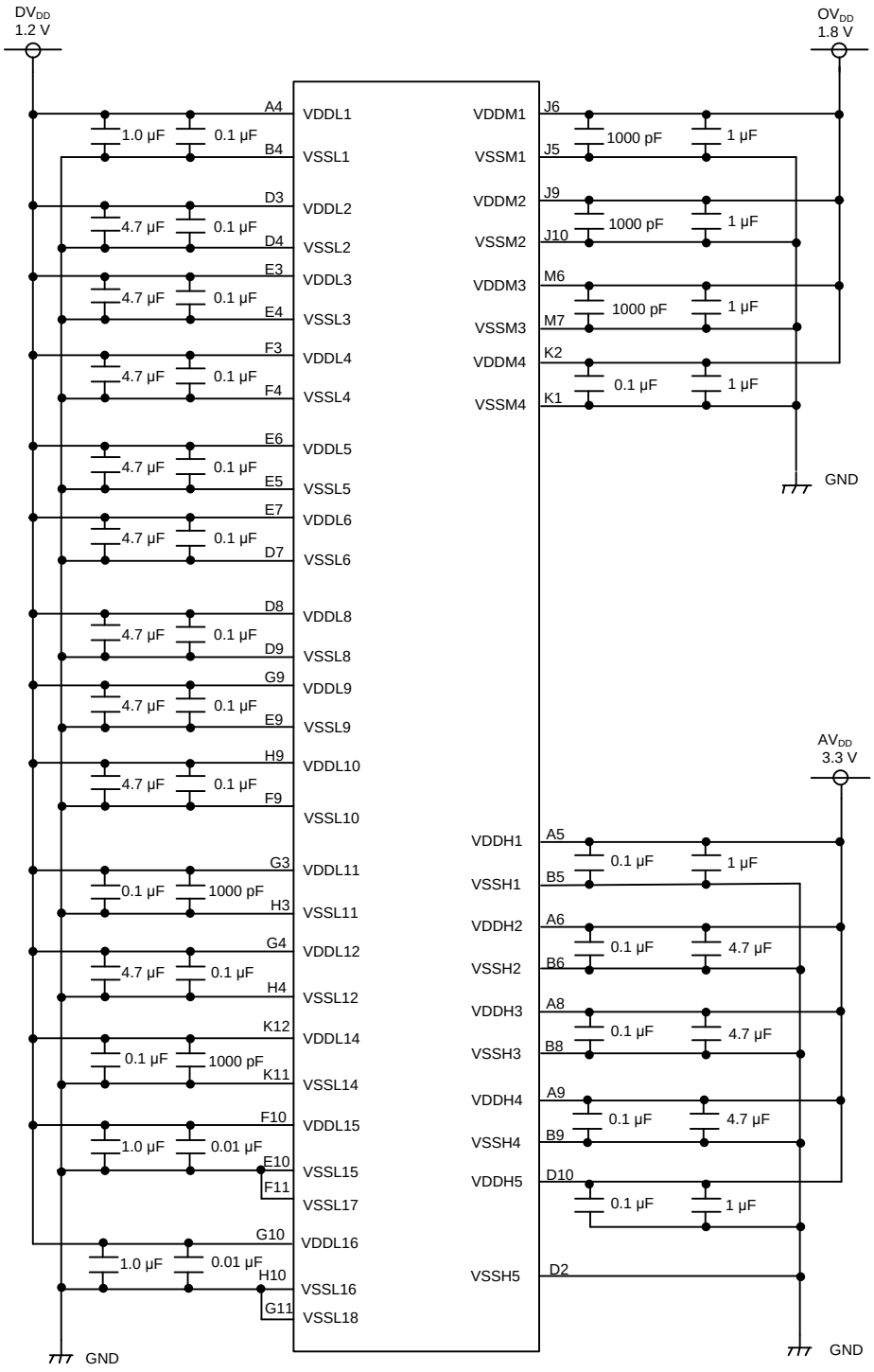
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section.
In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit

Power Pins

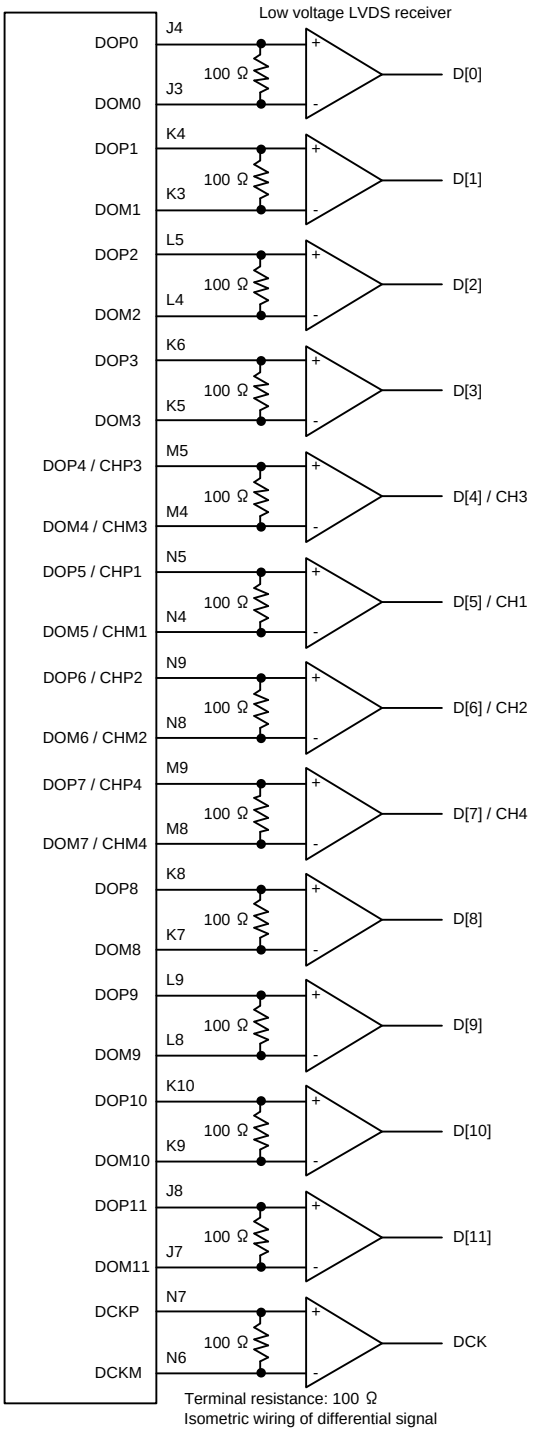


Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

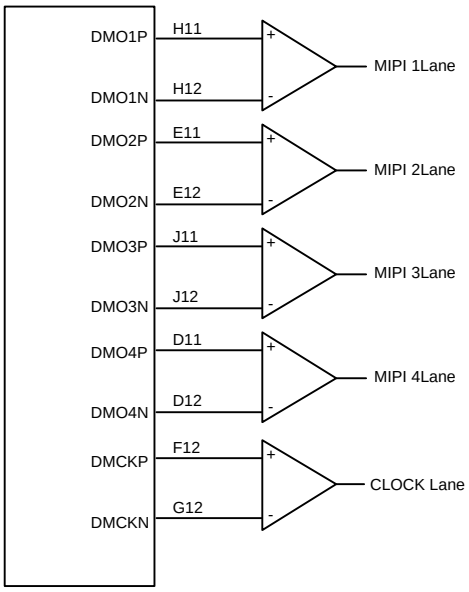
TENTATIVE

Output Pins

Low voltage LVDS output



CSI-2 Serial output

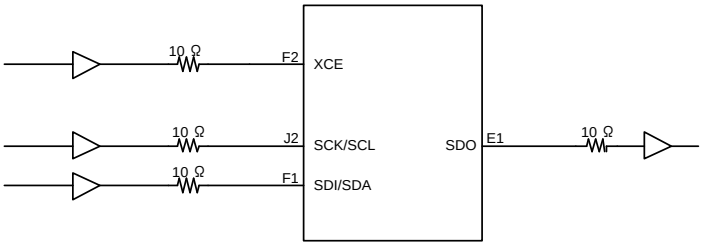


Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

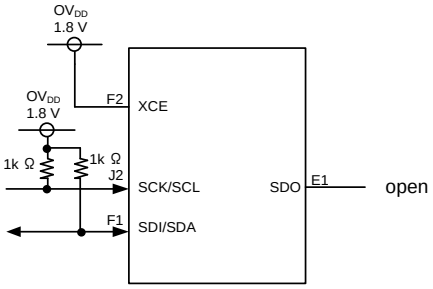
TENTATIVE

Serial Communication Pins

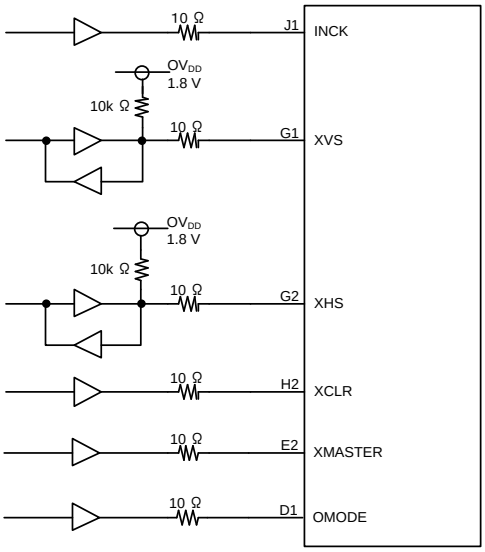
4-wire serial communication

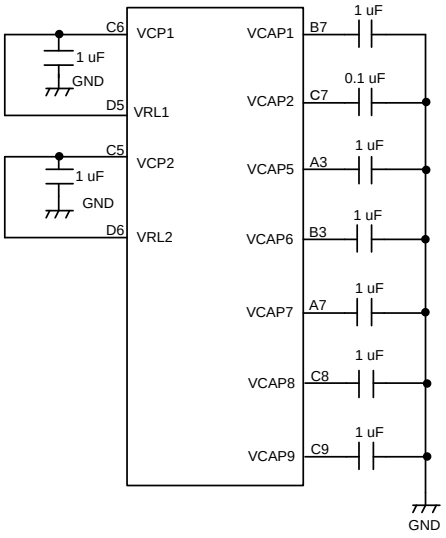


I^2C serial communication



Other Pins





Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

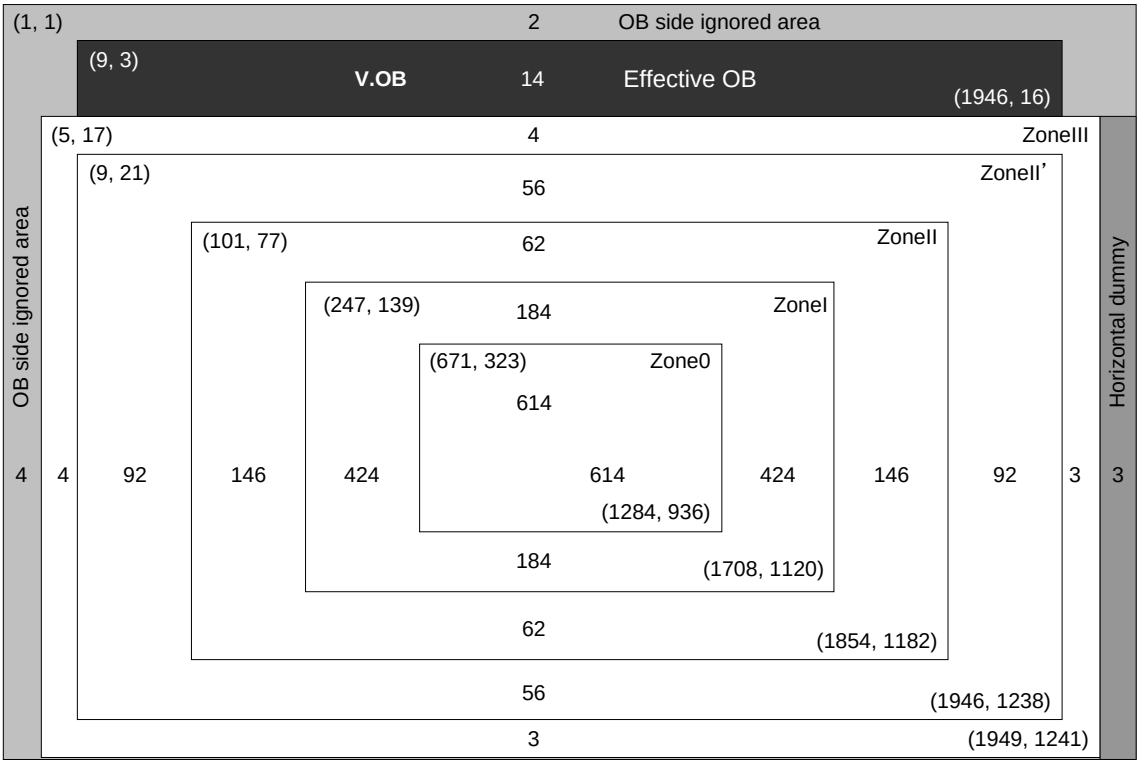
Spot Pixel Specifications

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain = 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	17	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	200		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ 1120 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	7.2 pcs
10.0 mV or higher	4.7 pcs
24.0 mV or higher	2.4 pcs
50.0 mV or higher	1.4 pcs
72.0 mV or higher	1.1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

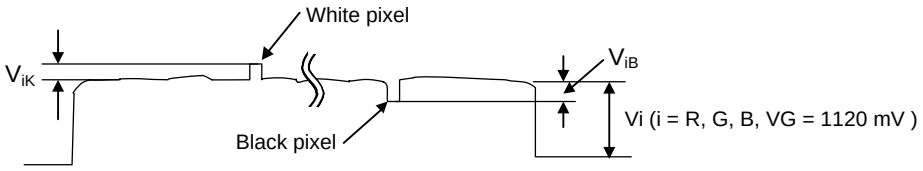
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 1120 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

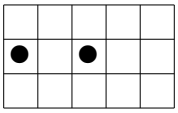
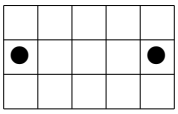
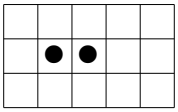
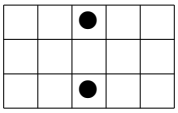
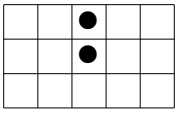
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

Signal output waveform of R/G/B channel

Spot Pixel Pattern Specifications

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

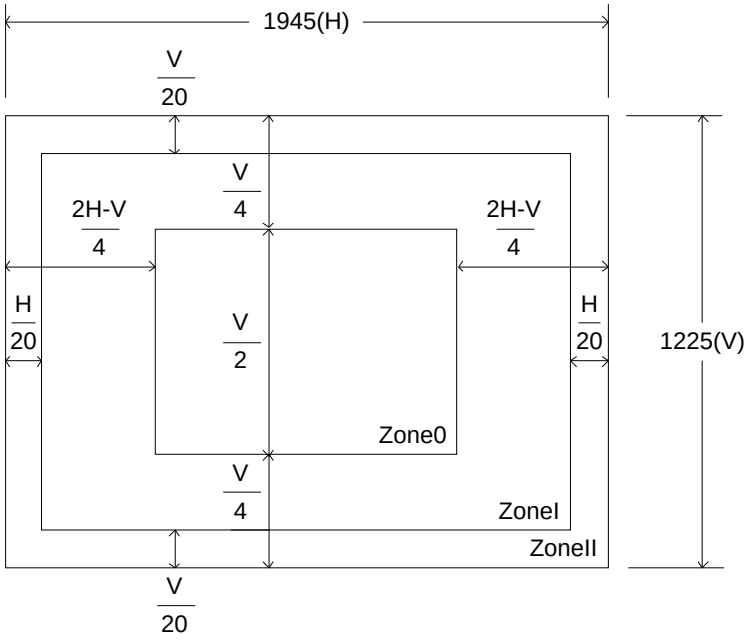
No.	Pattern (R G / G B: Specified in the left pixel array)	White pixel	Black pixel	Bright pixel
1	 Same color	Rejected	Rejected	Rejected
2	 Same color	Rejected	Rejected	Rejected
3	 Different color	Allowed	Allowed	Allowed
4	 Same color	Rejected	Allowed	Allowed
5	 Different color	Allowed	Allowed	Allowed

Note) 1. "● " shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated "Rejected" is selected and removed.
3. Spot pixels indicated "Allowed" are not the subject of selected rejection. They are counted including the number of allowable spot pixels by zone.
4. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Stain Specifications

Zone	Allowable pixels	Size	Level	Lens aperture
0 to II	0	L ≥ 3	R ≥ 8 %	F = 16
Means no stain over 3 lines or more.				

Stain Zone Definition

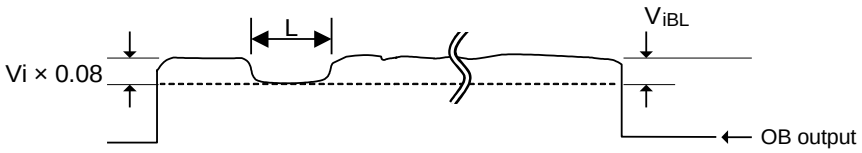


Stain Measurement Method

In the following measurement, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the G channel signal output is 1120 mV. Measure the local dip in the average value of the R / G / B channel signal output (Vi_{BL}), and then calculate the stain level (R) as the ratio of Vi_{BL} to the average value of the R/G/B channel signal output (Vi).

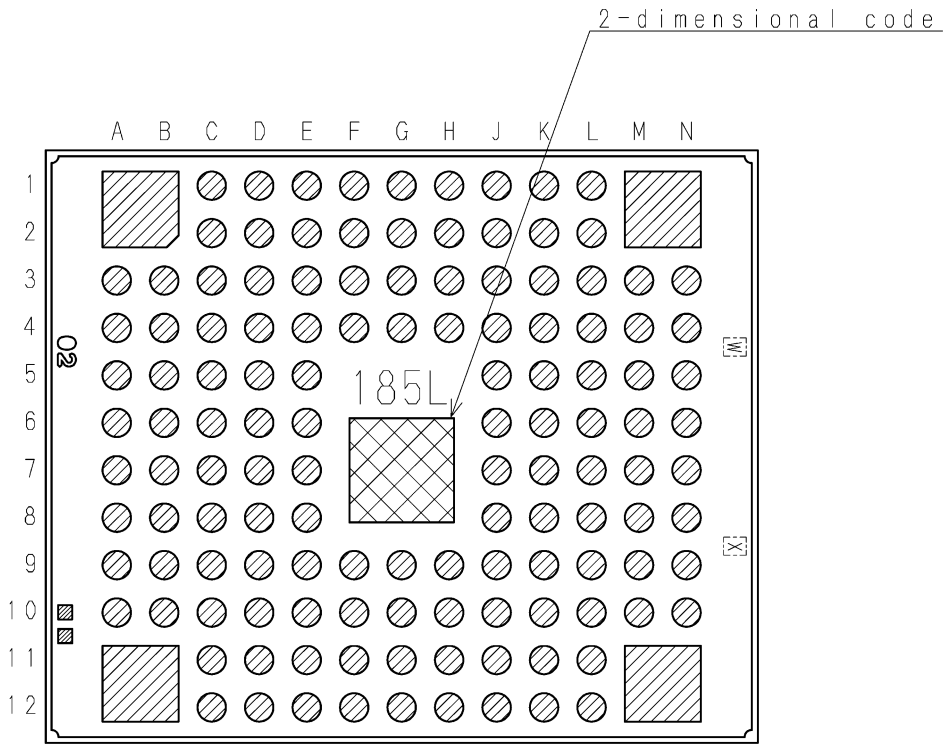
Stain level R = (Vi_{BL} / Vi) × 100 [%] (i = R, G, B)

At the same time, the size (L) of the area where the stain level is 8 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.



Signal output waveform of R/G/B channel

Marking



Note:Following characters enter into "W", and "X". (No Au coat)
W:In English upper case character, One character
X:Number, single number

DRAWING No. AM-B185LQJ(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

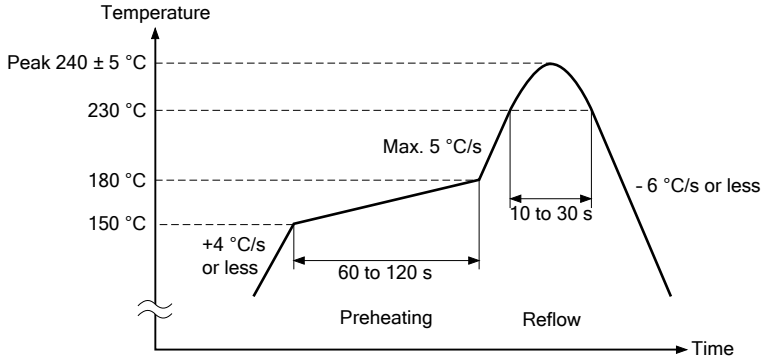
TENTATIVE

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

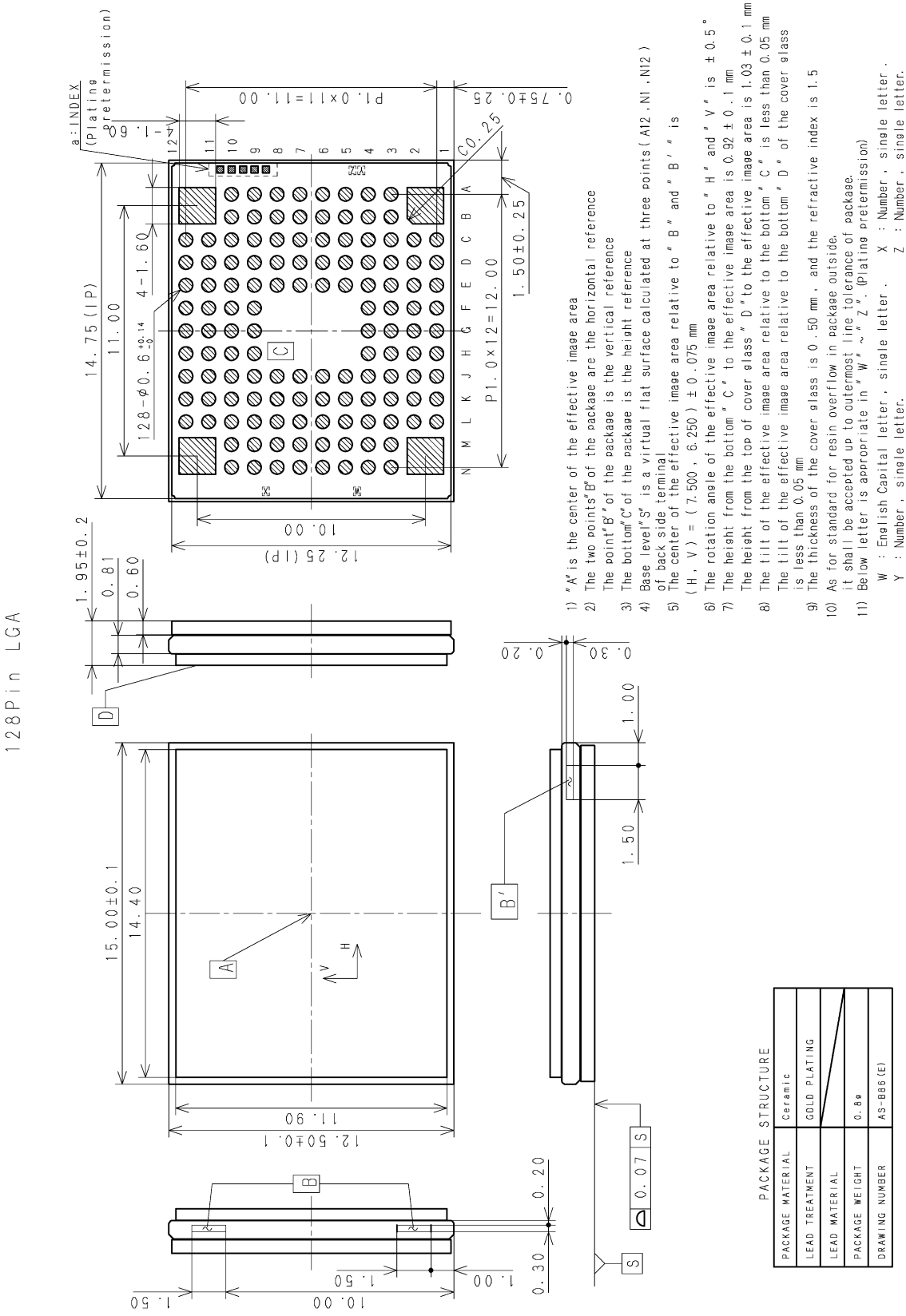
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

TENTATIVE

Package Outline

(Unit: mm)



Revision History

Date of change	Ver	Page	Contain of Change
2012/12/5	0.2.1	10,11,120	D2 pin NC⇒VSSH5(GND) changed
2013/1/10	0.3.0	38,44	Register Chip ID=02h Fixed value changed (Address 1Dh, 1Eh, A1h)
2013/1/10	0.3.0	45,46	Register Chip ID=03h/04h Fixed value changed from TBD
2013/1/10	0.3.0	1,93,94	Gain range changed : Digital Gain=18→24dB、Max Gain 42→48dB
2013/1/10	0.3.0	120	Peripheral Circuit (Numbers of capacitors for 1.2V Power changed)
2013/3/27	0.3.1	3	Operating temperature -10 to 75 ˚C →-30 to 75 ˚C
2013/3/27	0.3.1	23	Spectral Sensitivity Characteristic Graph is indicated from TBD
2013/3/27	0.3.1	97	tOFFSET : Fixed values changed from TBD
2013/4/5	0.4.0	24	Image Sensor Characteristics except R/G,B/G: Fixed values changed from TBD
2013/4/5	0.4.0	26,27	Measurement Method : Fixed values changed from TBD
2013/4/5	0.4.0	123	Spot Pixel Specifications : Fixed values changed from TBD
2013/4/5	0.4.0	125	Measurement Method for Spot Pixel : Fixed values changed from TBD
2013/4/5	0.4.0	127	Stain Measurement Method : Fixed values changed from TBD
2013/4/5	0.4.0	128	Marking : The figure is indicated from TBD
2013/4/5	0.4.0	131	Package Outline : The figure is updated
2013/5/31	0.4.1	8	“Physical Image” is deleted on the title of figure.
2013/5/31	0.4.1	16	Power Consumption : Fixed values changed from TBD
2013/5/31	0.4.1	21	Low Voltage LVDS DDR Output : Fixed values changed from TBD
2013/5/31	0.4.1	41	Correction ; Fixed value 00h→01h at register of “40h” & “42h”
2013/5/31	0.4.1	49	CCP_DT_FMT ; Changed “Readout setting value” in Description
2013/5/31	0.4.1	50	Lane_MODE ; Changed “Readout setting value” in Description
2013/5/31	0.4.1	53	List of Operation Modes 2/2-line bining : RAW10 → RAW12
2013/5/31	0.4.1	63,68,74,80	CCP_DT_FM and Lane_MODE are deleted at Detailed Register List table.
2013/5/31	0.4.1	68,71	RAW10→RAW12 at Detailed Register List (CSI-2)
2013/5/31	0.4.1	68	CCP_DT_FMT ; 0A0Ah→0C0Ch at Detailed Register List
2013/5/31	0.4.1	74	Correction ; HMAX and VMAX value at Detailed Register List (1080p)
2013/5/31	0.4.1	85	Correction ; WINPV + WINWV ≤ 1049 → WINPV + WINWV ≤ 1225
2013/5/31	0.4.1	88	Correction ; 6 ≤ WINWV_OB = OB_SIZE_V + 4 ≤ 16 → 6 ≤ WINWV_OB = OB_SIZE_V + 2 ≤ 16
2013/5/31	0.4.1	95	Correction ; Initial Value at BLKLEVEL
2013/5/31	0.4.1	103	CCP_DT_FM and Lane_MODE are deleted at CSI-2 serial Output Setting.
2013/5/31	0.4.1	103	CCP_DT_FM and Lane_MODE are deleted at Settings table.
2013/5/31	0.4.1	103,105	The maximum bit rate: Fixed values changed from TBD
2013/5/31	0.4.1	106,108	Correction ; Initial Value at ODBIT, ADBIT
2013/5/31	0.4.1	108	A/D Conversion Bits Setting LVDS Output/CSI-2 Output

Date of change	Ver	Page	Contain of Change
2013/5/31	0.4.1	113	Addition the sentence as below at the section of Software Rest, “However, the communication to continuous address can not use. In I2C communication, sensor not return ACK when SW_RESET is transferred.”
2013/5/31	0.4.1	113	Addition the figures of 4-wire and I2C to “Software Reset’s figure”.
2013/5/31	0.4.1	113	Switching time of “Software Reset’s figure”: Fixed values changed from TBD.
2013/7/5	0.4.2	44	Changing Setting Value at Register [Address] CID=02h [A1h] Set to “45h” ⇒ Do not rewrite (Default Value “44h”)
2013/7/5	0.4.2	45	Changing Setting Value at Register [Address] CID=03h [23], [26], [E0], [E1], [E2], [E5], [E6], [E7], [E8]
2013/7/5	0.4.2	46	Changing Setting Value at Register [Address] CID=04h [61], [66], [67]