

B6FS Serializer Chip Datasheet

SUMMARY DESCRIPTION

The high-performance Ambarella B6 companion chips enable the transmission of HD and 4K video from remote camera modules via coaxial cables, without the introduction of latency or a loss of video quality. The B6 family of chips enables a wide range of automotive camera applications, including surround view, electronic mirrors, ADAS, and multi-channel video recording.

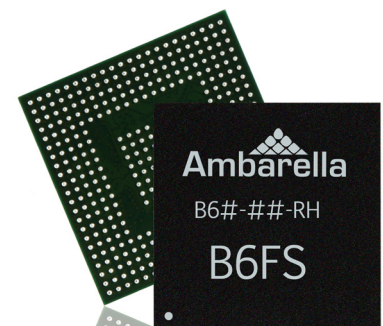
The Ambarella B6FS serializer chip captures Bayer RGB sensor input, serving as a bridge between a remotely-located sensor and an Ambarella B6NS de-serializer chip or A9AQ SoC.

KEY FEATURES

- MIPI / SLVS combination PHY
- Captures full HD-resolution Bayer RGB sensor data, which is subsequently transferred using a simple coaxial cable
- Capable of transmitting up to 3 Gb/s of aggregated throughput to the B6NS de-serializer chip or to the A9AQ SoC
- Back-channel communication for programming sensor settings.
- Programmable video compression for reducing video data rate
- Up to 10 General Purpose Input / Output pins
- Multi-bit error correction
- 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm)
- Operating temperature: -20 C to +85 C

CONTENTS

1. Overview	1
2. Peripheral Interfaces	5
3. Pins	6
4. Electrical Characteristics	12
5. Package	15
6. Contact and Order Information.....	17
7. Important Notice	18
8. Revision History.....	19



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1. OVERVIEW

This datasheet for the B6FS automotive serializer chip from Ambarella begins with a brief introduction to the B6 family of co-processors ([Section 1.1](#)) and a summary of the key features of the B6FS chip ([Section 1.2](#)). Chapter 2 describes the B6FS modules and interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

1.1 Introduction to B6 Co-Processors from Ambarella

Ambarella B6 companion chips enable multi-stream capture of up to 4Kp30 video for high-performance automotive applications including surround view, electronic mirrors, ADAS, and multi-channel video recording. Designed to support complex systems requiring multiple image sensors deployed over a vehicle, the B6 family of co-processors serves as a highly efficient bridge between the digital signal processor (DSP) and up to four image sensors, allowing 360-degree coverage without the introduction of latency or a loss of video quality. Moreover, B6 chips enable high-resolution Bayer RGB sensor data to be transferred using a simple coaxial cable. The 5x5-mm B6S family is composed of the following co-processor types.

1. **B6FS:** (Far-end) The B6FS serializer chip captures Bayer RGB sensor input, serving as a bridge between a remotely-located sensor and a B6NS co-processor (or an A9AQ chip).
2. **B6NS:** (Near-end) The B6NS de-serializer chip combines the 1- or 2 channels of video stream from B6FS and sends it via MIPI-CSI or SLVS interface to an Ambarella SoC.
3. **B6DFS:** (Far-End) The B6DFS chip transfers the SERDES data received from A9AQ in MIPI-DSI- and Open LDI format to connect to remote external displays. Refer to [Figure 1-3](#) below.

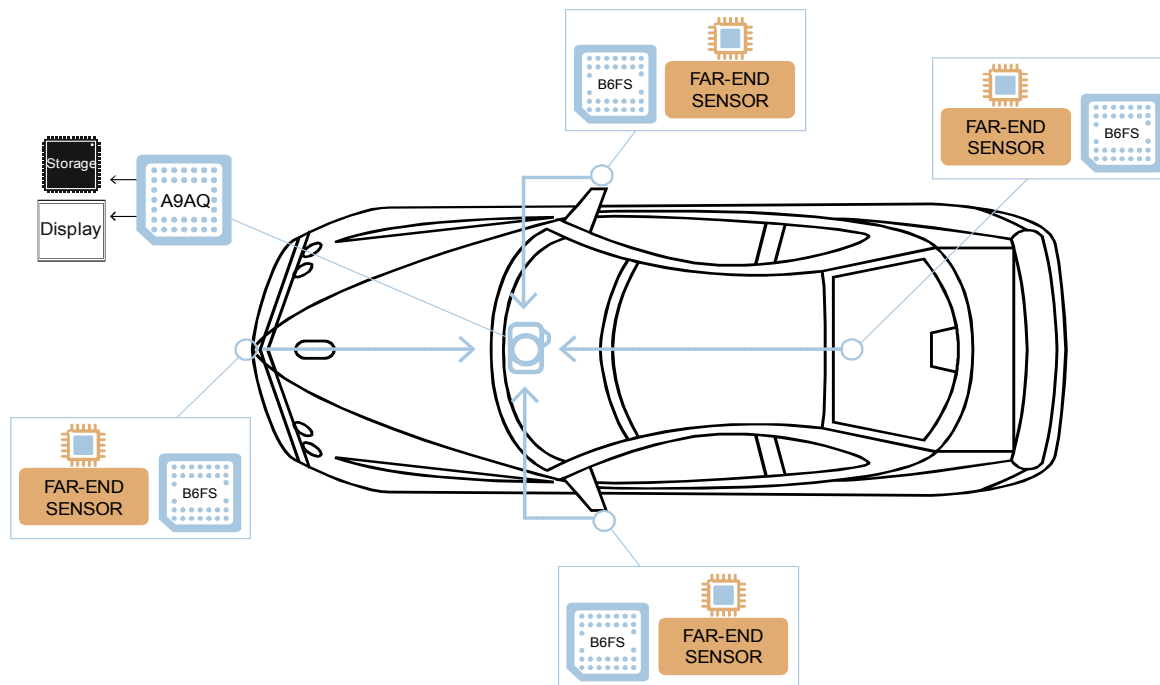


Figure 1-1. Surround View with Recording: Automotive Video Application with an Ambarella A9AQ SoC and Four B6FS Chips.

The figure on the previous page illustrates a four-channel Surround View system (Figure 1-1), while the figures below represent an electronic mirror system (Figure 1-2) and a two-channel recorder (Figure 1-3).

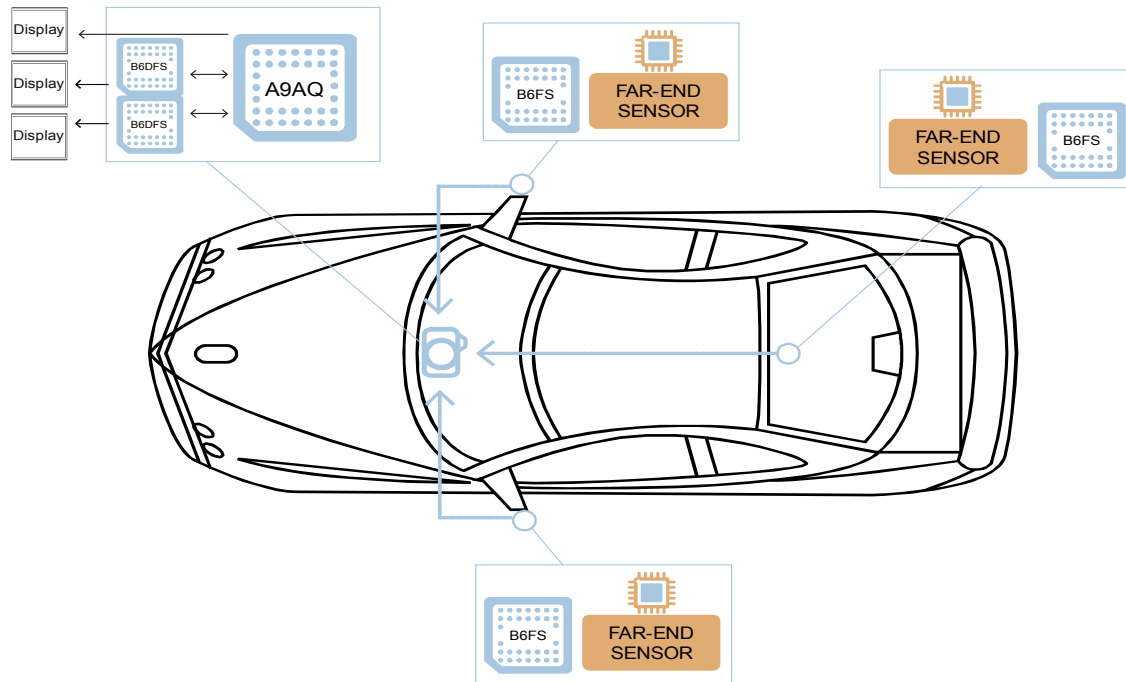


Figure 1-2. Electronic Mirror: Automotive Video Application with an Ambarella A9AQ SoC, Three B6DFS Chips, and two B6DFS Chips.

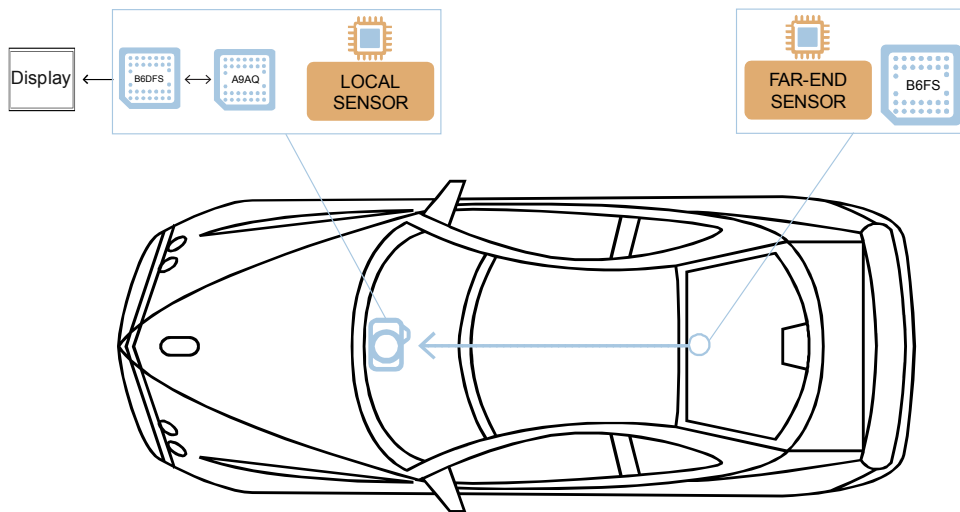


Figure 1-3. Two-Channel Recorder: Automotive Video Application with One B6DFS Chip, One A9AQ Chip and One B6DFS Chip.

Notes:

- The B6FS serializer chip captures Bayer RGB sensor input, serving as a bridge between a remotely-located sensor and a B6NS chip (required to convert the SERDES stream into a MIPI-CSI or SLVS stream) or an A9AQ chip (B6NS is not required when using A9AQ).
- B6DFS (far-end) display chip is required when outputting to one or two remote displays using A9AQ. For a single local display, no display chips are required.
- Coaxial cables (up to 10m) can be used to connect remote cameras/ displays using the B6 SERDES solution. In a multi-channel use case, if the cable is disconnected while the system is active, the specific channel will be dropped; while the rest of the system operation will not be disrupted.

1.2 Introduction to the B6FS

Features of the B6FS serializer chip are as follows:

- MIPI / SLVS combination PHY
 - Supports:
 - Up to 4-lane MIPI sensors
 - Up to 4-lane SLVS sensors
 - Includes support for popular CMOS image sensor brands (RGB Bayer output)
 - Built-in termination
- Flexible sensor programming
 - Selectable SSI/SPI or I2C/IDC interface
 - SSI/SPI or I2C/IDC sensor communications occur over the coaxial cable (i.e., no extra control wires are required).
- Resolution Converter (in Bayer RGB domain)
- Video Compression
 - Programmable video compression for reducing video data rate
 - Performs a light level of compression on the sensor data after CFA downsampling.
- Sub-LVDS data serializer
 - Capable of transmitting up to 3 Gb/s of aggregated throughput to the B6N or A9AQ chip over a single coaxial cable
 - Multi-bit pre-emphasis
 - Multi-bit driveability control
 - 8b -10b encoding for DC balancing
- Back-channel communication for programming sensor settings.
- Up to 10 General Purpose Input / Output (GPIO) pins

B6FS Serializer Chip Datasheet

- Multi-bit error correction
- Four PLLs: Core, Sensor, VOUT, Tx0 PHY
- 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm)
- Operating temperature range: -20 C to +85 C

2. PERIPHERAL INTERFACES

2.1 Interfaces: Overview

This chapter provides summary information regarding the B6FS peripheral interfaces. The chapter is organized as follows:

- [\(Section 2.2\) Video / Sensor Input \(VIN\) Interface](#)
- [\(Section 2.3\) Serializer Module](#)

2.2 Video / Sensor Input (VIN) Interface

The features of the B6FS VIN interface are provided below.

- Two types of sensors are supported:
 - Up to 4-Lane SLVS
 - Up to 4-Lane MIPI
- Includes support for popular CMOS image sensor brands (RGB Bayer output)
- Built-in termination
- Master (external) sync generation

2.3 Serializer Module

The B6FS serializer module is capable of transmitting 3 Gb/s of aggregated throughput to the B6NS co-processor via a simple coaxial cable. Features of the Sub-LVDS serializer interface include:

- Multi-bit pre-emphasis and driveability control
- 8b-10b encoding for DC balancing

3. PINS

3.1 Overview of the B6FS Pins

This section provides a list of the 49 external pins according to their location on the B6FS chip. The figure below indicates the orientation of the pins by column (numbers) and row (letters).

	1	2	3	4	5	6	7	
A	gpio_1	clk_si	por_l	NC	NC	NC	vsync0	A
B	gpio_0	test_mode	VDD18	NC	AVDD	hsync0	rest	B
C	i2c0_scl	i2c0_sda	VSSi	VSSi	VDD18	xin	VSSi	C
D	mipi_dn_clk	mipi_dp_clk	VDD18	AVDD	VSSi	VSSi	tx_hsp_0	D
E	mipi_dp0	mipi_dn0	spi_mosi	VDDi	VDDi	efuse_vqps	tx_hs_n_0	E
F	mipi_dn1	mipi_dp1	mipi_dn3	spi_miso	VDD18	cfg_spi_en	cfg_spi_miso	F
G	mipi_dn2	mipi_dp2	mipi_dp3	spi_clk	spi_en0	cfg_spi_clk	cfg_spi_mosi	G
	1	2	3	4	5	6	7	

Figure 3-1. Pin Map for the B6FS Chip.

The following table lists all of the external pins on the B6FS chip in order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Multiplexed Functions					GPIO
			First	Second	Third	Fourth	Fifth	
A1	GPIO_1	Board Control	spi_clk	efuse_vqps_en			clk_si	23
A2	CLK_SI	System	pll_obsrv_core	clk_si				
A3	POR_L	System						
A4	NC							
A5	NC							
A6	NC							

Loc.	Pin Name	Group	Multiplexed Functions					
			First	Second	Third	Fourth	Fifth	GPIO
A7	VSYNCO	Sensor	vin_vsync0	irq				11
B1	GPIO_0	Board Control	pll_obsrv_sensor	irq	phy_bist_ahb_fail_comb	hsync_ext	clk_si	22
B2	TEST_MODE	System						
B3	VDD18	1.8-V Power						
B4	NC							
B5	AVDD	Analog Power						
B6	HSYNCO	Sensor	vin_hsync0					12
B7	REXT	Band Gap						
C1	I2C0_SCL	Camera Interface	pll_obsrv_vo	i2c0_scl	uart_ahbm_rx	data_ls0		9
C2	I2C0_SDA	Camera Interface		i2c0_sda	uart_ahbm_tx	data_ls1	phy_bist_ahb_test_done_comb	10
C3	VSSI	Ground						
C4	VSSI	Ground						
C5	VDD18	1.8-V Power						
C6	XIN	System						
C7	VSSI	Ground						
D1	MIPI_DN_CLK	MIPI CSI						
D2	MIPI_DP_CLK	MIPI CSI						
D3	VDD18	1.8-V Power						
D4	AVDD	Analog Power						
D5	VSSI	Ground						
D6	VSSI	Ground						
D7	TX_HSP_0	SERDES						
E1	MIPI_DPO	MIPI CSI						
E2	MIPI_DNO	MIPI CSI						
E3	SPI_MOSI	Sensor Config	pll_obsrv_sensor	spi_mosi	i2c1_scl3			7
E4	VDDI	Power						
E5	VDDI	Power						
E6	EFUSE_VQPS	eFUSE						
E7	TX_HSN_0	SERDES						
F1	MIPI_DN1	MIPI CSI						
F2	MIPI_DP1	MIPI CSI						
F3	MIPI_DN3	MIPI CSI						
F4	SPI_MISO	Sensor Config		spi_miso	i2c1_sda3			8
F5	VDD18	1.8-V Power						

Loc.	Pin Name	Group	Multiplexed Functions					
			First	Second	Third	Fourth	Fifth	GPIO
F6	CFG_SPI_EN	DSP Config		cfg_spi_en	idcs_ahbm_sda			
F7	CFG_SPI_MISO	DSP Config		cfg_spi_miso				
G1	MIPI_DN2	MIPI CSI						
G2	MIPI_DP2	MIPI CSI						
G3	MIPI_DP3	MIPI CSI						
G4	SPI_CLK	Sensor Config	pll_obsrv_phy	spi_clk	i2c1_scl2	uart_ahbm_clk		4
G5	SPI_EN0	Sensor Config		spi_en0	i2c1_sda2	lstx_din2		5
G6	CFG_SPI_CLK	DSP Config		cfg_spi_clk	idcs_ahbm_scl			
G7	CFG_SPI_MOSI	DSP Config	pll_obsrv_phy	cfg_spi_mosi				

Table 3-1. Pin List and Mapping Table for the B6FS Chip.

3.2 Pin Tables

The pins for the B6FS chip are classified according to interface as follows:

- (Section 3.2.1) Input Pins
- (Section 3.2.2) Video Output Pins
- (Section 3.2.3) SERDES TX Pins
- (Section 3.2.4) I2C / IDC Pins
- (Section 3.2.5) SSI / SPI Pins
- (Section 3.2.6) GPIO Pins
- (Section 3.2.7) System Pins
- (Section 3.2.8) Power, Ground and PLL Pins

Each pin table below provides the functional pin name, location, pin direction, pad type, and a brief description.

3.2.1 Input Pins

Name	Location	Description
CLK_SI	A2	Sensor master clock output
HSYNCO	B6	Sensor master sync
VSYNCO	A7	

Table 3-2. Video Input Sensor Interface Pins.

3.2.2 Video Output Pins

Name	Location	Description	
MIPI_DN_CLK	D1	CSI Clock-N	SLVS Clock-N
MIPI_DN0	E2	CSI Lane 0-N	SLVS Lane 0-N
MIPI_DN1	F1	CSI Lane 1-N	SLVS Lane 1-N
MIPI_DN2	G1	CSI Lane 2-N	SLVS Lane 2-N
MIPI_DN3	F3	CSI Lane 3-N	SLVS Lane 3-N
MIPI_DP_CLK	D2	CSI Clock-P	SLVS Clock-P
MIPI_DP0	E1	CSI Lane 0-P	SLVS Lane 0-P
MIPI_DP1	F2	CSI Lane 1-P	SLVS Lane 1-P
MIPI_DP2	G2	CSI Lane 2-P	SLVS Lane 2-P
MIPI_DP3	G3	CSI Lane 3-P	SLVS Lane 3-P

Table 3-3. Video Output Interface Pins.

Note:

- The pins above support two VOUT modes: MIPI-CSI and SLVS. Note that these formats are not supported by all chips.

3.2.3 SERDES TX Pins

Name	Location	Description
TX_HSN_0	E7	SERDES TX Channel-0 N
TX_HSP_0	D7	SERDES TX Channel-0 P

Table 3-4. SERDES TX Pins.

3.2.4 I2C / IDC Pins

Pin Name	Location	Dir	Type	Description
I2C0_SCL	C1	I/O	CMOS	Camera module interface
I2C0_SDA	C2	I/O	CMOS	

Table 3-5. I2C / IDC Interface Pins.

3.2.5 SSI / SPI Pins

Pin Name	Location	Dir	Type	Description
SPI_CLK	G4	I/O	CMOS	Sensor configuration interface
SPI_EN0	G5	I/O	CMOS	
SPI_MISO	F4	I/O	CMOS	
SPI_MOSI	E3	I/O	CMOS	
CFG_SPI_CLK	G6	I/O	CMOS	DSP configuration interface
CFG_SPI_EN	F6	I/O	CMOS	
CFG_SPI_MISO	F7	I/O	CMOS	
CFG_SPI_MOSI	G7	I/O	CMOS	

Table 3-6. SSI / SPI Pins.

3.2.6 GPIO Pins

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
4	SPI_CLK	pll_obsrv_phy	spi_clk	i2c1_scl2	uart_ahbm_clk	
5	SPI_EN0		spi_en0	i2c1_sda2	lstx_din2	
7	SPI_MOSI	pll_obsrv_sensor	spi_mosi	i2c1_scl3		
8	SPI_MISO		spi_miso	i2c1_sda3		
9	I2C0_SCL	pll_obsrv_vo	i2c0_scl	uart_ahbm_rx	data_ls0	
10	I2C0_SDA		i2c0_sda	uart_ahbm_tx	data_ls1	phy_bist_ahb_test_done_comb
11	VSYNCO	vin_vsync0	irq			
12	HSYNCO	vin_hsync0				
22	GPIO_0	pll_obsrv_sensor	irq	phy_bist_ahb_fail_comb	hsync_ext	clk_si
23	GPIO_1	spi_clk	efuse_vqps_en			clk_si

Table 3-7. General Purpose Input / Output Pins.

3.2.7 System Pins

Name	Location	Dir	Description
TEST_MODE	B2	I	0 - Normal mode 1 - Test mode
POR_L	A3	I	Power-on reset pin (active low)
XIN	C6	I	72-MHz crystal oscillator
VSSI	C7	O	Digital input ground

Table 3-8. System Pins.

3.2.8 Power, Ground and PLL Pins

Name	Location	Dir	Type	Description
VDDI	E4, E5	S	Digital Supply	Digital core power supply
AVDD	D4, B5	S	Analog Supply	Analog core power supply
VDD18	B3,C5,D3, F5	S	Digital Supply	1.8-V power supply
VSSI	C3, C4, D5, D6	G	Digital Ground	Digital input ground

Table 3-9. Power and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Overview of the Electrical Characteristics

This chapter provides information regarding the electrical characteristics of the B6FS co-processor. The chapter is organized as follows:

- (Section 4.2) Absolute Ratings
- (Section 4.3) Recommended Operating Conditions
- (Section 4.4) Fail-Safe Pins
- (Section 4.5) Video Signal Waveforms and Timing

Note that the electrical details provided in this chapter are estimates. Please contact an Ambarella representative for current electrical specifications.

4.2 Absolute Ratings

The following table provides absolute ratings for the nominal analog / digital voltages in [Section 4.3.1](#).

Parameter	Minimum	Maximum
Digital supply voltage (1.8 V)	-0.3 V	2.0 V
Analog supply voltage (1.1 V)	-0.3 V	1.35 V
Digital supply voltage (1.0 V)	-0.3 V	1.35 V
Digital I/O range (V)	-0.3 V	2.0 V
Analog I/O range (V)	-0.3 V	2.0 V
Operating temperature (case) (°C)	-20 C to +85 C	
Storage temperature (°C)	-40 C to +150 C	
Thermal resistance (Θ_{jc}) (°C/W)	TBD	

Table 4-1. Absolute Ratings.

Note:

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Recommended Operating Conditions

Recommended operating conditions are provided for the following:

- (Section 4.3.1) Power Rails DC
- (Section 4.3.2) Digital I/O

4.3.1 Power Rails DC

Parameter	Comments	Minimum	Typical	Maximum	Ripple
VDDI		1.07 V	1.1 V	1.13 V	2%
-		-	-	-	-
AVDD		1.07 V	1.1 V	1.13 V	2%
VDD18		1.75 V	1.8 V	1.9 V	2%

Table 4-2. Power Rails DC Characteristics (Subject to Change).

Note:

- The DC characteristics shown above are subject to change.

4.3.2 Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.4 V
VIH	Input High Voltage	1.2 V		2.0 V
VOL	Output Low Voltage			0.24 V
VOH	Output High Voltage	1.3 V		

Table 4-3. Digital I/O Characteristics.

4.4 Fail-Safe Pins

All B6FS CMOS pins are fail-safe and can have active signals at or below 2.0 V when the B6FS is powered down.

4.5 Video Signal Waveforms and Timing

This section contains B6FS analog video waveform diagrams for reference purposes. Please ensure that the analog video output from the system board meets desired/standard specifications.

4.5.1 Video Input (VIN) Timing: MIPI / SLVS Mode

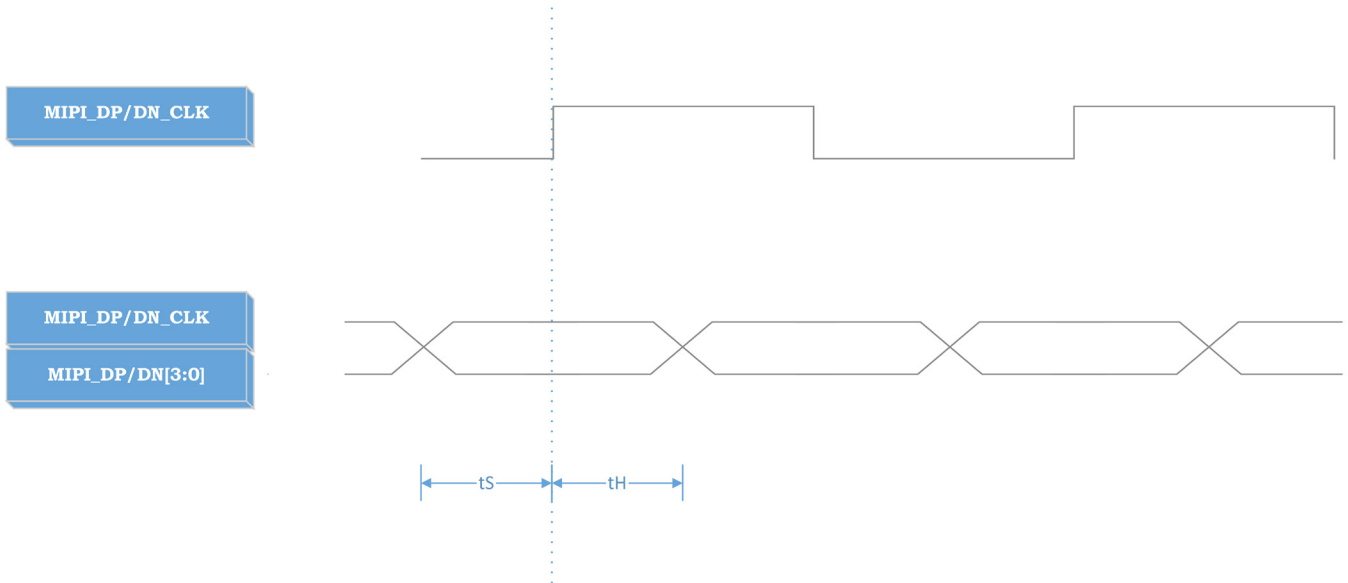


Figure 4-1. Video Input Timing: SLVS / MIPI Mode.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: MIPI_DN/DP_CLK MIPI_DN/DP[3:0]	100 ps	100 ps	

Table 4-4. SLVS / MIPI Video Input Timing Setup/Hold.

5. PACKAGE

The B6FS chip has a 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm).

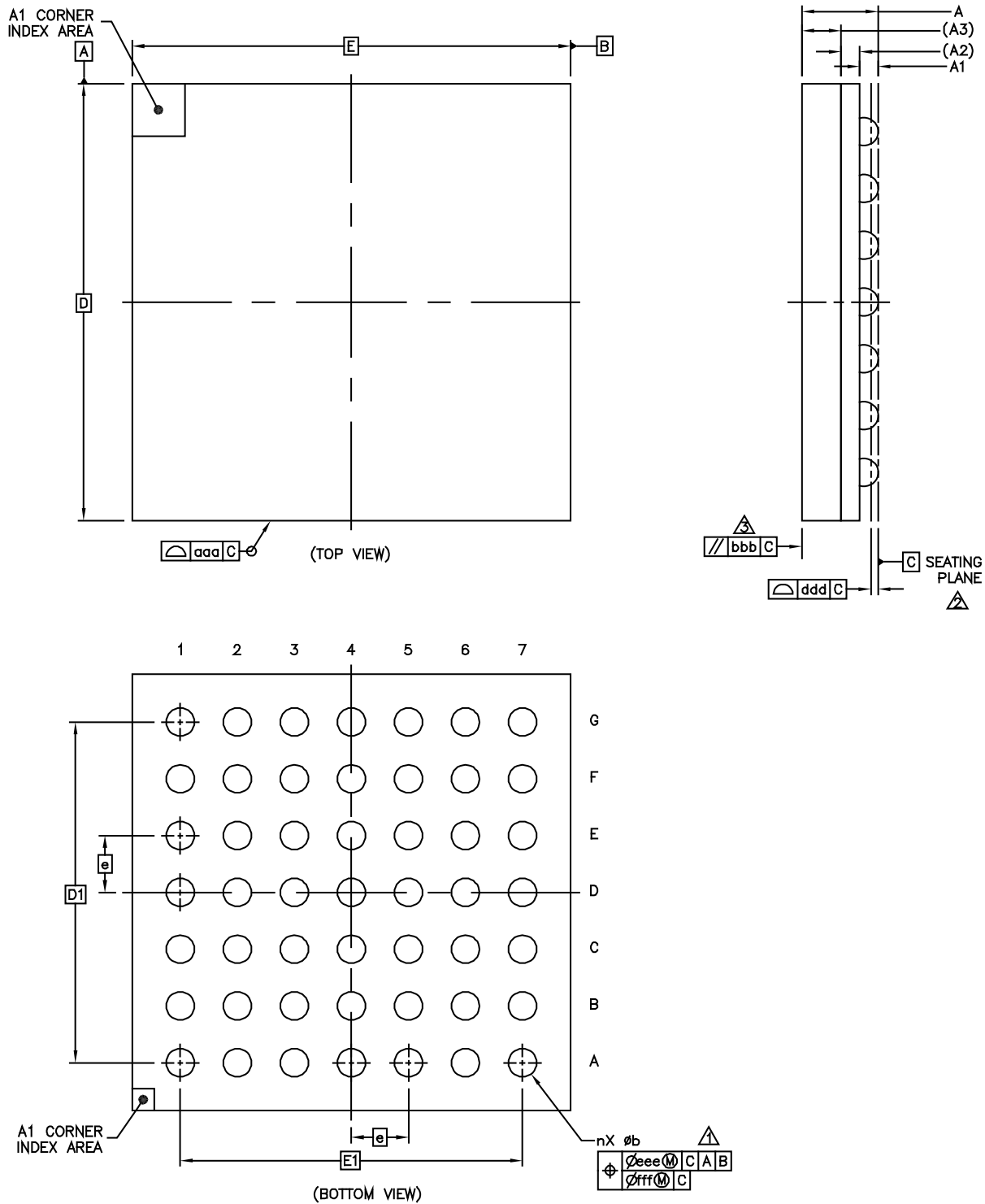


Figure 5-1. The B6FS Package.

Parameter	Symbol	Minimum	Nominal	Maximum
Total Thickness	A			1
Stand Off	A1	0.16		0.26
Substrate Thickness	A2		0.21 REF	
Mold Thickness	A3		0.45 REF	
Body Size	D		5 BSC	
	E		5 BSC	
Ball Diameter			0.3	
Ball Opening			0.275	
Ball Width	b	0.27		0.37
Ball Pitch	e		0.65 BSC	
Ball Count	n		49	
Edge Ball Center to Center	D1		3.9 BSC	
	E1		3.9 BSC	
Body Center to Contact Ball	SD			
	SE			
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

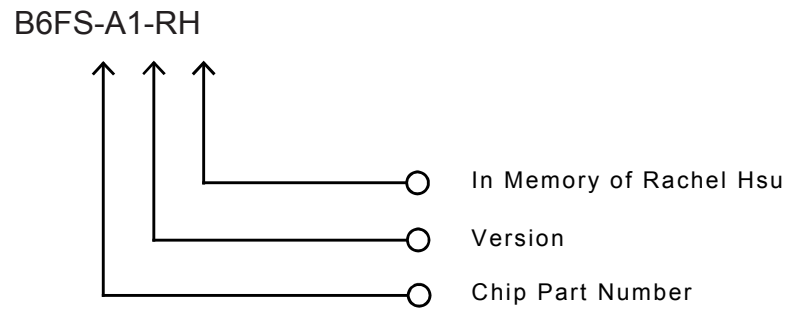
Table 5-1. Dimensions of the B6FS Package (millimeters).

Notes for table and figures:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
2. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

6. CONTACT AND ORDER INFORMATION

All chips in the B6 series are Lead-Free, Halogen-Free and RoHS compliant.



For complete Ambarella contact information, please visit www.ambarella.com.

7. IMPORTANT NOTICE

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8. REVISION HISTORY

Our goal is to provide our customers with the highest-quality documentation possible, and to continuously improve our publications to ensure that your experience with Ambarella’s products is a positive one. If you have any questions or comments regarding this document, please contact the Technical Writing team at docs@ambarella.com. Your feedback is welcomed and appreciated.

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	16 August 2017	New B6 Production Part
0.2	18 December 2017	Updated Pins: AVDD18 & VDDO merged into VDD18, XOUT converted to VSSi Updated Table 3-8: System Pins- Changed description for C6 and C7 Updated Table 4-2 Power Rails DC Characteristics: Values changed for VDDI
1.0	27 April 2018	Deleted all references for B6DNS Updated Figure 1-3 Removed B6DNS, SOC and B6NS, added A9AQ, figure title updated Updated Table 3-1 Pin List and Mapping Table for the B6FS Chip and Table 3-3 Video Output Interface Pins - Deleted open LDI and MIPI-DSI updated to MIPI-CSI Removed “preliminary” wording