B6NS De-Serializer Chip Datasheet

SUMMARY DESCRIPTION

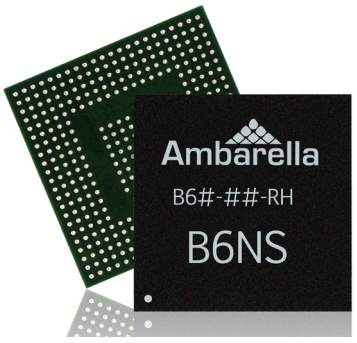
The high-performance Ambarella B6 companion chips enable the transmission of HD and 4K video from remote camera modules via coaxial cables, without the introduction of latency or a loss of video quality. The B6 family of chips enables a wide range of automotive camera applications, including surround view, electronic mirrors, ADAS, and multi-channel video recording.

The Ambarella B6NS two-channel de-serializer chip receives one or two video streams from B6FS serializer chips or CMOS sensors, then outputs the combined video via an SLVS interface to an Ambarella SoC.

KEY FEATURES

- Supports up to two channels of Serializer-Deserializer (SERDES) input
- Supports up to 4Kp30 per input, or 1080p60 with HDR
- Performs all sensor synchronization tasks
- Back-channel communication for programming sensor settings.
- Programmable video compression for reducing video data rate
- 10 General Purpose Input / Output (GPIO) pins
- Multi-bit error correction
- 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm)

CONTENTS



1. OVERVIEW

This datasheet for the B6NS automotive de-serializer chip from Ambarella begins with a brief introduc-tion to the B6 family of co-processors (Section 1.1) and a summary of the key features of the two-channel-capable(Section 1.2). Chapter 2 describes the B6NS modules and interfaces. For pin details and electrical character-istics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

1.1 Introduction to B6 Co-Processors from Ambarella

Ambarella B6 companion chips enable multi-stream capture of up to 4Kp30 video for high-performance automo-tive applications including surround view, electronic mirrors, ADAS, and multi-channel video recording. Designed to support complex systems requiring multiple image sensors deployed over a vehicle, the B6 family of co-proces-sors serves as a highly efficient bridge between the digital signal processor (DSP) and up to four image sensors, allowing 360-degree coverage without the introduction of latency or a loss of video quality. Moreover, B6 chips enable high-resolution Bayer RGB sensor data to be transferred using a simple coaxial cable. The 5x5-mm B6S family is composed of the following co-processor types.

1. **B6FS**: (Far-end) The B6FS serializer chip captures Bayer RGB sensor input, serving as a bridge between a remotely-located sensor and a B6NS co-processor (or an A9AQ chip).
2. **B6NS**: (Near-end) The B6NS de-serializer chip combines the 1- or 2 channels of video stream from B6FS and sends it via MIPI-CSI or SLVS interface to an Ambarella SoC.
3. **B6DFS**: (Far-End) The B6DFS chip transfers the SERDES data received from A9AQ in MIPI-DSI or Open LDI format to connect to remote external displays. Refer to Figure 1-3 below.

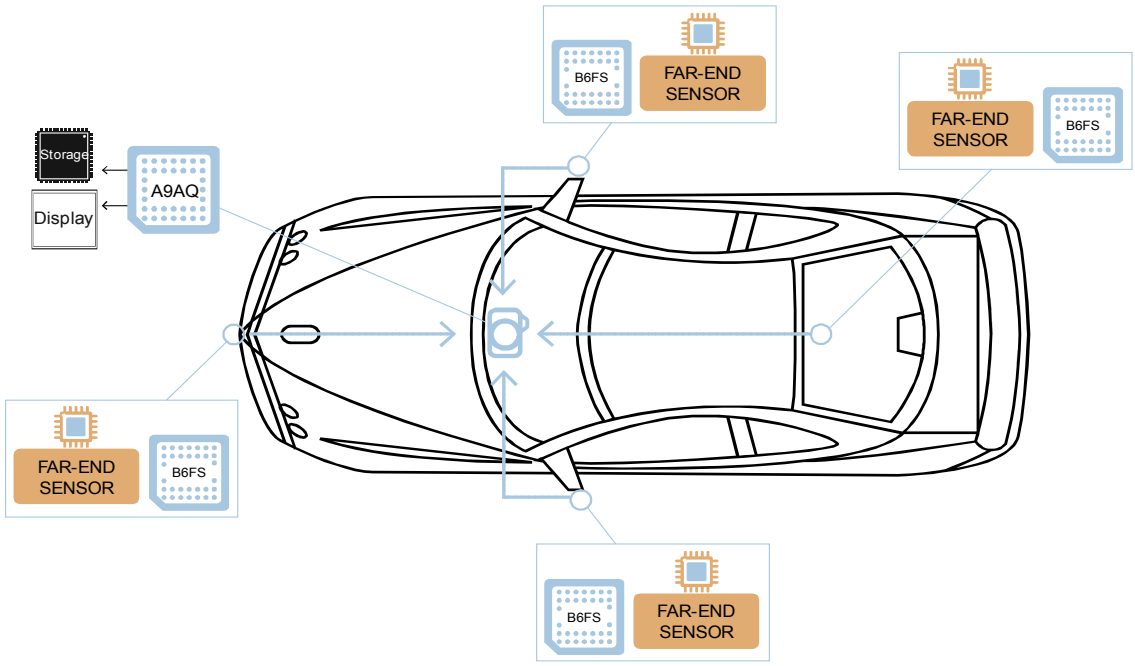


Figure 1-1. Surround View with Recording: Automotive Video Application with an Ambarella A9AQ SoC and Four B6FS Chips.

The figure on the previous page illustrates a four-channel Surround View system (Figure 1-1), while the figures

below represent an electronic mirror system (Figure 1-2) and a two-channel recorder (Figure 1-3).

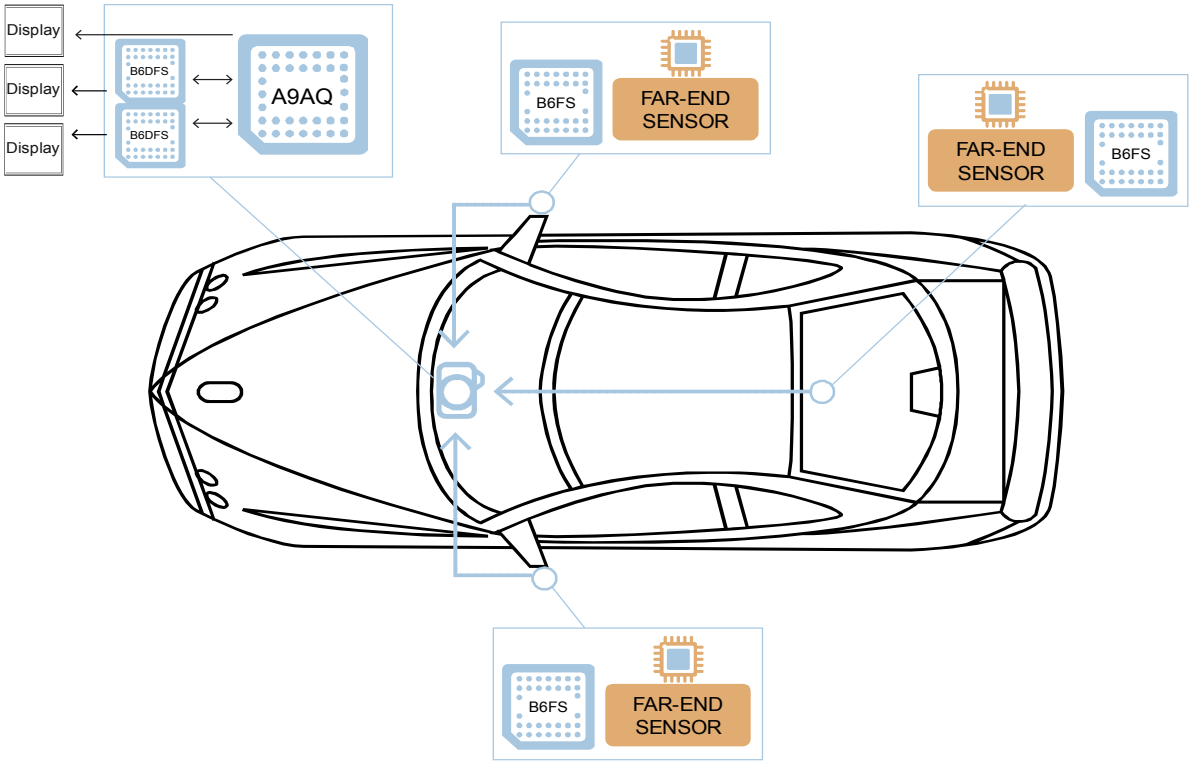


Figure 1-2. Electronic Mirror: Automotive Video Application with an Ambarella A9AQ SoC, Three B6FS Chips, and two B6DFS Chips.

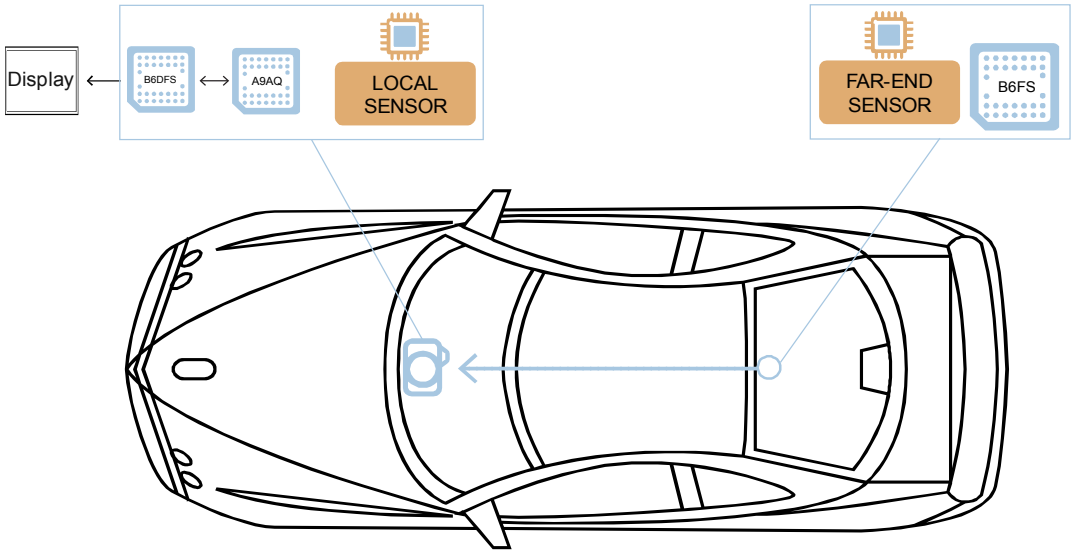


Figure 1-3. Two-Channel Recorder: Automotive Video Application with One B6DFS Chip, One A9AQ Chip, and One B6FS Chip.

Notes:

- The B6FS serializer chip captures Bayer RGB sensor input, serving as a bridge between a remotely-located sensor and a B6NS chip (required to convert the SERDES stream into a MIPI-CSI or SLVS stream) or an A9AQ chip (B6NS is not required when using A9AQ).
- B6DFS (far-end) display chip is required when outputting to one or two remote display using A9AQ. For a single local display, no display chips are required.
- Coaxial cables (up to 10m) can be used to connect remote cameras/ displays using the B6 SERDES solution. In a multi-channel use case, if the cable is disconnected while the system is active, the specific channel will be dropped; while the rest of the system operation will not be disrupted.

1.2 Introduction to the B6NS

Features of the B6NS de-serializer chip are as follows:

- Data Path
  - Serializer-Deserializer (SERDES) Input Mode: the Sensor → B6FS VIN → B6FS SERDES TX→ B6NS SERDES RX → B6NS MIPI-CSI
  - The Merger Module reassembles SERDES data into a single video channel
  - Supports up to 4Kp30 or 1080p60 video resolution
- Video Stream Output (VOUT) Module.
  - Supports two output modes: MIPI-CSI and SLVS
  - Flexible back-channel communication
  - Selectable SSI/SPI or I2C/IDC interface
  - SSI/SPI or I2C/IDC sensor communications occur over the coaxial cable (i.e., no extra control wires required)
  - Supports multi-channel/sensor synchronization
  - Coaxial cable (up to 10 m) required for connection to B6FS
- Programmable video decompressor
- 10 General Purpose Input / Output (GPIO) pins
- Multi-bit error correction
- ECC encoder and decoder
- Five PLLs: Core, VOUT,Rx PHY, Tx0 PHY, and Tx1 PHY
- 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm)
- Operating temperature range: -20 C to +85 C

2. PERIPHERAL INTERFACES

2.1 Interfaces: Overview

This chapter provides summary information regarding the B6NS peripheral interfaces. The chapter is organized as follows:

2.2 Input Interface

The B6NS input interface supports two separate input instances simultaneously, each with independent programming and operation.

The features of the B6NS input interface are provided below.

- Two channels of input
- Serializer-Deserializer (SERDES) Input Mode: Up to 2-lane SERDES input from B6 far-side chips
  - Up to 4Kp30 per input
- Pixel Reordering module allows programmable sequencing of the YUV (Y, Cb, Cr) components into the desired output order.
  - Support for RGB format included

2.3 Video Output (VOUT) Interface

The B6NS VOUT interface supports output modes: MIPI-CSI MIPI DSI, SLVS, and Open LDI. and SLVS

2.4 IDCS Bridge Module

The IDCS module is an I2C / IDC slave device that serves as a bridge between the B6NS internal bus and the Ambarella DSP. Features of the IDCS module include:

- Three operational modes:
  - Standard mode: up to 100 kb/s data transfer rate
  - Fast mode: up to 400 kb/s data transfer rate
  - High-speed (Hs) mode: up to 3.4 Mb/s data transfer rate
- Minimum clock frequency: 1.34 MHz in standard mode

2.5 SSI Host Interface

The B6NS chip provides a SSI host interface module, a slave interface which receives commands from the chip and transfers them into a AHB master signal (The data path is Ambarella SoC → B6NS SSI2 AHB interface → B6NS AHB bus → B6NS AHB peripherals). Features of the SSI host interface include:

- Support for 8-bit data frames
- Support for **scph** = 0, indicating that the serial clock toggles in the middle of the first data bit, and **scpol** = 0, indicating a low inactive state.

3. PINS

3.1 Overview of the B6NS Pins

This section provides a list of the 49 external pins according to their location on the B6NS chip. The figure below indicates the orientation of the pins by column (numbers) and row (letters).

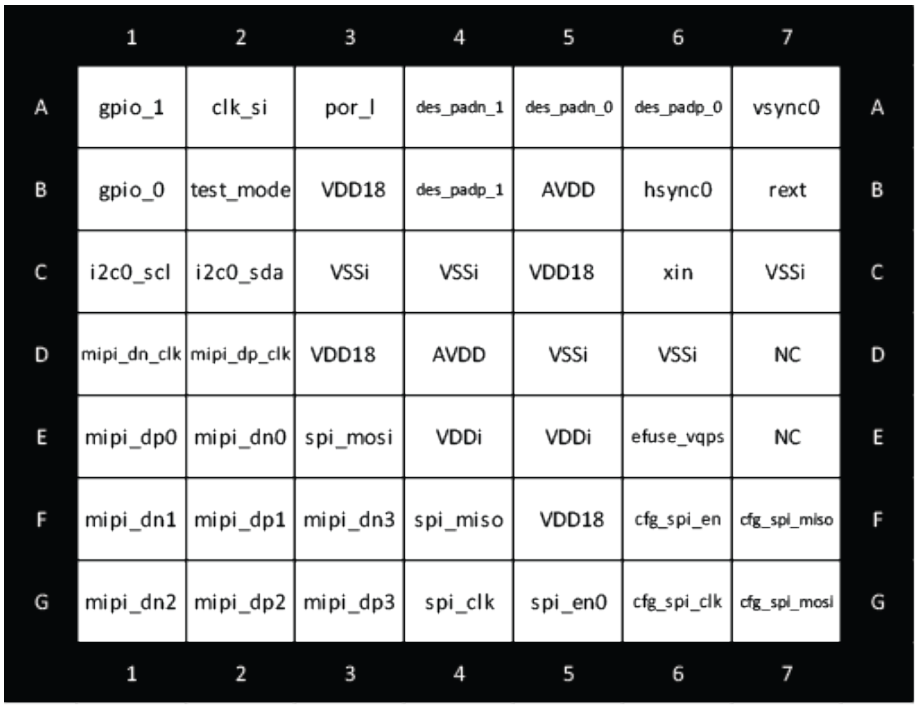


Figure 3-1. Pin Map for the B6NS Chip.

The following table lists all of the external pins on the B6NS chip in order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Multiplexed Functions					
			First	Second	Third	Fourth	Fifth	GPIO
A1	**GPIO_1**	Board Control	spi_clk	efuse_vqps_en			clk_si	23
A2	**CLK_SI**	System	pll_obsv_core	clk_si				
A3	**POR_L**	System						
A4	**DES_PADN_1**	SERDES						
A5	**DES_PADN_0**	SERDES						
A6	**DES_PADP_0**	SERDES						
A7	**VSYNC0**	Sensor	vin_vsync0	irq				11

Loc.	Pin Name	Group	Multiplexed Functions					
			First	Second	Third	Fourth	Fifth	GPIO
B1	**GPIO_0**	Board Control	pll_obsv_ sensor	irq	phy_bist_ ahb_fail_ comb	hsync_ext	clk_si	22
B2	**TEST_MODE**	System						
B3	**VDD18**	1.8-V Power						
B4	**DES_PADP_1**	SERDES						
B5	**AVDD**	Analog Power						
B6	**HSYNC0**	Sensor	vin_hsync0					12
B7	**REXT**	Band Gap						
C1	**I2C0_SCL**	Camera Interface	pll_obsv_vo	i2c0_scl	uart_ahbm_ rx	data_ls0		9
C2	**I2C0_SDA**	Camera Interface		i2c0_sda	uart_ahbm_tx	data_ls1	phy_bist_ ahb_test_ done_comb	10
C3	**VSSI**	Ground						
C4	**VSSI**	Ground						
C5	**VDD18**	1.8-V Power						
C6	**XIN**	System						
C7	**VSSI**	Ground						
D1	**MIPI_DN_CLK**	MIPI CSI						
D2	**MIPI_DP_CLK**	MIPI CSI						
D3	**VDD18**	1.8-V Power						
D4	**AVDD**	Analog Power						
D5	**VSSI**	Ground						
D6	**VSSI**	Ground						
D7	**NC**							
E1	**MIPI_DP0**	MIPI CSI						
E2	**MIPI_DN0**	MIPI CSI						
E3	**SPI_MOSI**	Sensor Config	pll_obsv_ sensor	spi_mosi	i2c1_scl3			7
E4	**VDDI**	Power						
E5	**VDDI**	Power						
E6	**EFUSE_VQPS**	eFUSE						
E7	**NC**							
F1	**MIPI_DN1**	MIPI CSI						
F2	**MIPI_DP1**	MIPI CSI						
F3	**MIPI_DN3**	MIPI CSI						
F4	**SPI_MISO**	Sensor Config		spi_miso	i2c1_sda3			8
F5	**VDD18**	1.8-V Power						
F6	**CFG_SPI_EN**	DSP Config		cfg_spi_en	idcs_ahbm_ sda			

Loc.	Pin Name	Group	Multiplexed Functions					
			First	Second	Third	Fourth	Fifth	GPIO
F7	**CFG_SPI_MISO**	DSP Config		cfg_spi_miso				
G1	**MIPI_DN2**	MIPI CSI						
G2	**MIPI_DP2**	MIPI CSI						
G3	**MIPI_DP3**	MIPI CSI						
G4	**SPI_CLK**	Sensor Config	pll_obsv_phy	spi_clk	i2c1_scl2	uart_ahbm_clk		4
G5	**SPI_EN0**	Sensor Config		spi_en0	i2c1_sda2	lstx_din2		5
G6	**CFG_SPI_CLK**	DSP Config		cfg_spi_clk	idcs_ahbm_scl			
G7	**CFG_SPI_MOSI**	DSP Config	pll_obsv_phy	cfg_spi_mosi				

Table 3-1. Pin List and Mapping Table for the B6NS Chip.

3.2 Pin Tables

The pins for the B6NS chip are classified according to interface as follows:

- (Section 3.2.1) Input Pins
- (Section 3.2.2) Video Output Pins
- (Section 3.2.3) I2C / IDC Pins
- (Section 3.2.4) SSI / SPI Pins
- (Section 3.2.5) GPIO Pins
- (Section 3.2.6) System Pins
- (Section 3.2.7) Power, Ground and PLL Pins

Each pin table below provides the functional pin name, location, pin direction, pad type, and a brief description.

3.2.1 Input Pins

3.2.1.1 Input: SERDES + SERDES

Name	Location	Description
DES_PADP_0	A6	SERDES RX Channel-0
DES_PADN_0	A5	
DES_PADP_1	B4	SERDES RX Channel-1
DES_PADN_1	A4	

Table 3-2. Video Input Interface Pins: SERDES/SERDES Dual-Channel.

3.2.1.2 Input: Sensor Interface

Name	Location	Description
CLK_SI	A2	Sensor master clock output
HSYNC0	B6	Sensor master sync
VSYNC0	A7	

Table 3-3. Video Input Sensor Interface Pins.

3.2.2 Video Output Pins

Name	Location	Description	
MIPI_DN_CLK	D1	CSI Clock-N	SLVS Clock-N
MIPI_DN0	E2	CSI Lane 0-N	SLVS Lane 0-N
MIPI_DN1	F1	CSI Lane 1-N	SLVS Lane 1-N
MIPI_DN2	G1	CSI Lane 2-N	SLVS Lane 2-N
MIPI_DN3	F3	CSI Lane 3-N	SLVS Lane 3-N
MIPI_DP_CLK	D2	CSI Clock-P	SLVS Clock-P
MIPI_DP0	E1	CSI Lane 0-P	SLVS Lane 0-P
MIPI_DP1	F2	CSI Lane 1-P	SLVS Lane 1-P
MIPI_DP2	G2	CSI Lane 2-P	SLVS Lane 2-P
MIPI_DP3	G3	CSI Lane 3-P	SLVS Lane 3-P

Table 3-4. Video Output Interface Pins.

Note:

- The pins above support two VOUT modes: MIPI-CSI and SLVS. Note that these formats are not supported by all chips.

3.2.3 I2C / IDC Pins

Pin Name	Location	Dir	Type	Description
I2C0_SCL	C1	I/O	CMOS	Camera module interface
I2C0_SDA	C2	I/O	CMOS	

Table 3-5. I2C / IDC Interface Pins.

3.2.4 SSI / SPI Pins

Pin Name	Location	Dir	Type	Description
SPI_CLK	G4	I/O	CMOS	Sensor configuration interface
SPI_EN0	G5	I/O	CMOS	
SPI_MISO	F4	I/O	CMOS	
SPI_MOSI	E3	I/O	CMOS	
CFG_SPI_CLK	G6	I/O	CMOS	DSP configuration interface
CFG_SPI_EN	F6	I/O	CMOS	
CFG_SPI_MISO	F7	I/O	CMOS	
CFG_SPI_MOSI	G7	I/O	CMOS	

Table 3-6. SSI / SPI Pins.

3.2.5 GPIO Pins

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
4	**SPI_CLK**	pll_obsv_phy	spi_clk	i2c1_scl2	uart_ahbm_clk	
5	**SPI_EN0**		spi_en0	i2c1_sda2	lstx_din2	
7	**SPI_MOSI**	pll_obsv_sensor	spi_mosi	i2c1_scl3		
8	**SPI_MISO**		spi_miso	i2c1_sda3		
9	**I2C0_SCL**	pll_obsv_vo	i2c0_scl	uart_ahbm_rx	data_ls0	
10	**I2C0_SDA**		i2c0_sda	uart_ahbm_tx	data_ls1	phy_bist_ahb_ test_done_comb
11	**VSYNC0**	vin_vsync0	irq			
12	**HSYNC0**	vin_hsync0				
22	**GPIO_0**	pll_obsv_sensor	irq	phy_bist_ahb_ fail_comb	hsync_ext	clk_si
23	**GPIO_1**	spi_clk	efuse_vqps_en			clk_si

Table 3-7. General Purpose Input / Output Pins.

3.2.6 System Pins

Name	Location	Dir	Description
TEST_MODE	B2	I	0 - Normal mode 1 - Test mode
POR_L	A3	I	Power-on reset pin (active low)
XIN	C6	I	72-MHz crystal oscillator
VSSI	C7	O	Digital input ground

Table 3-8. System Pins.

3.2.7 Power, Ground and PLL Pins

Name	Location	Dir	Type	Description
VDDI	E4, E5	S	Digital Supply	Digital core power supply
AVDD	D4, B5	S	Analog Supply	Analog core power supply
VDD18	B3,C5,D3,F5	S	Digital Supply	1.8-V power supply
VSSI	C3, C4, D5, D6	G	Digital Ground	Common ground

Table 3-9. Power and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Overview of the Electrical Characteristics

This chapter provides information regarding the electrical characteristics of the B6NS co-processor. The chapter is organized as follows:

- (Section 4.2) Absolute Ratings
- (Section 4.3) Recommended Operating Conditions
- (Section 4.4) Fail-Safe Pins
- (Section 4.5) Video Signal Waveforms and Timing

Note that the electrical details provided in this chapter are preliminary estimates. Please contact an Ambarella representative for current electrical specifications.

4.2 Absolute Ratings

The following table provides absolute ratings for the nominal analog / digital voltages in Section 4.3.1.

Parameter	Minimum	Maximum
Digital supply voltage (1.8 V)	-0.3 V	2.0 V
Analog supply voltage (1.1 V)	-0.3 V	1.35 V
Digital supply voltage (1.0 V)	-0.3 V	1.35 V
Digital I/O range (V)	-0.3 V	2.0 V
Analog I/O range (V)	-0.3 V	2.0 V
Operating temperature (case) (^{o}C)	-20 C to +85 C	
Storage temperature (^{o}C)	-40 C to +150 C	
Thermal resistance (Θ_{jc}) (^{o}C/W)	TBD	

Table 4-1. Absolute Ratings.

Note:

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Recommended Operating Conditions

Recommended operating conditions are provided for the following:

- (Section 4.3.1) Power Rails DC
- (Section 4.3.2) Digital I/O

4.3.1 Power Rails DC

Parameter	Comments	Minimum	Typical	Maximum	Ripple
VDDI		1.07 V	1.1 V	1.13 V	2%
-		-	-	-	-
AVDD		1.07 V	1.1 V	1.13 V	2%
VDD18		1.75 V	1.8 V	1.9 V	2%

Table 4-2. Power Rails DC Characteristics (Subject to Change).

Note:

- The DC characteristics shown above are subject to change.

4.3.2 Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.4 V
VIH	Input High Voltage	1.2 V		2.0 V
VOL	Output Low Voltage			0.24 V
VOH	Output High Voltage	1.3 V		

Table 4-3. Digital I/O Characteristics.

4.4 Fail-Safe Pins

All B6NS CMOS pins are fail-safe and can have active signals at or below 2.0 V when the B6NS is powered down.

4.5 Video Signal Waveforms and Timing

This section contains B6NS analog video waveform diagrams for reference purposes. Please ensure that the analog video output from the system board meets desired/standard specifications.

4.5.1 Video Output (VOUT) Timing

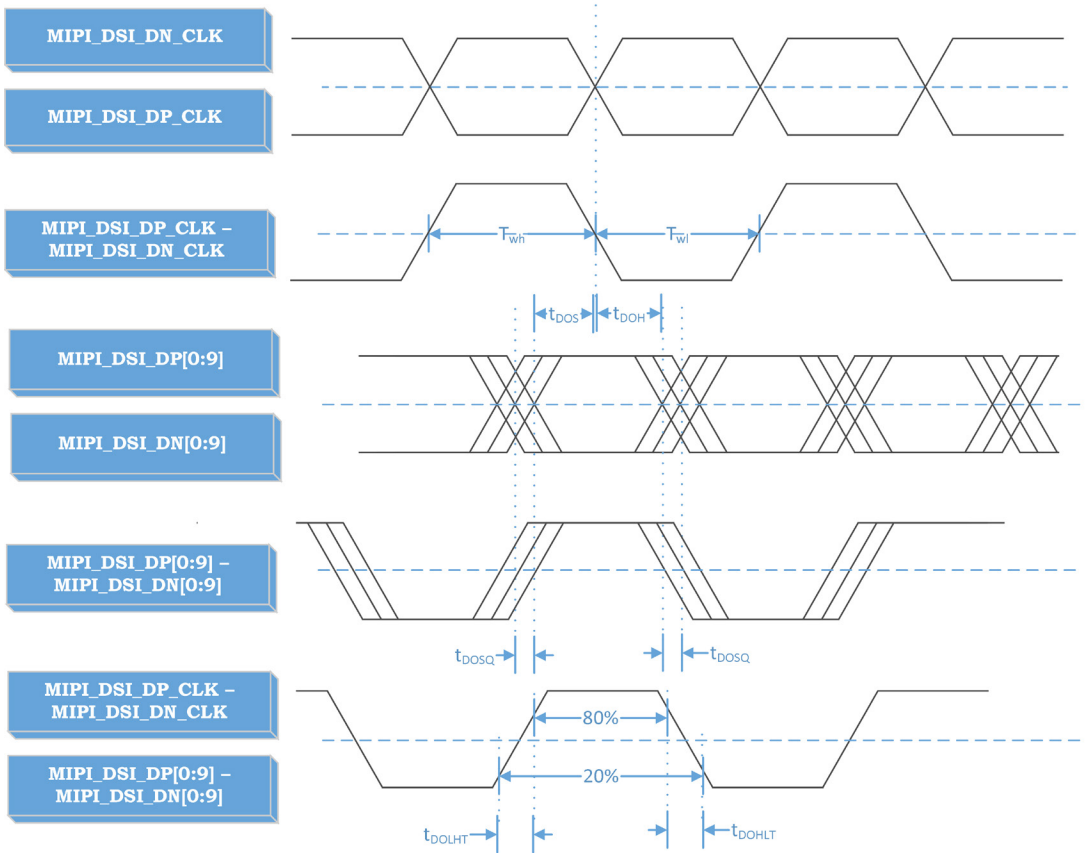


Figure 4-1. Video Output Timing.

Item	Symbol	Min.	Typ.	Max.	Unit	Comments
DO skew time (including jitter)	t_{DOSQ}			150	ps	Data rate 900 MHz DDR (1.8 Gbs)
DO setup time	t_{DOS}	100			ps	Data rate 900 MHz DDR (1.8 Gbs)
DO hold time	t_{DOH}	100			ps	Data rate 900 MHz DDR (1.8 Gbs)
DO rise time	t_{DOLHT}		200		ps	Simulated value with load capacitance (4 pF)
DO fall time	t_{DOHLT}		200		ps	Simulated value with load capacitance (4 pF)
DCK duty cycle	D_{DCDCK}	45	50	55	%	
DCK pulse width	T_{wh} T_{wl}	300			ps	Including period jitter

Table 4-4. Video Output Timing Values..

While the diagram shows pins **MIPI_CSI_DP/N[0:9]**, note that the B6NS pins are **MIPI_DP/DN[0:3]**.

5. PACKAGE

The B6NS chip has a 49-pin, 0.65-mm pitch BGA package (5 mm x 5 mm).

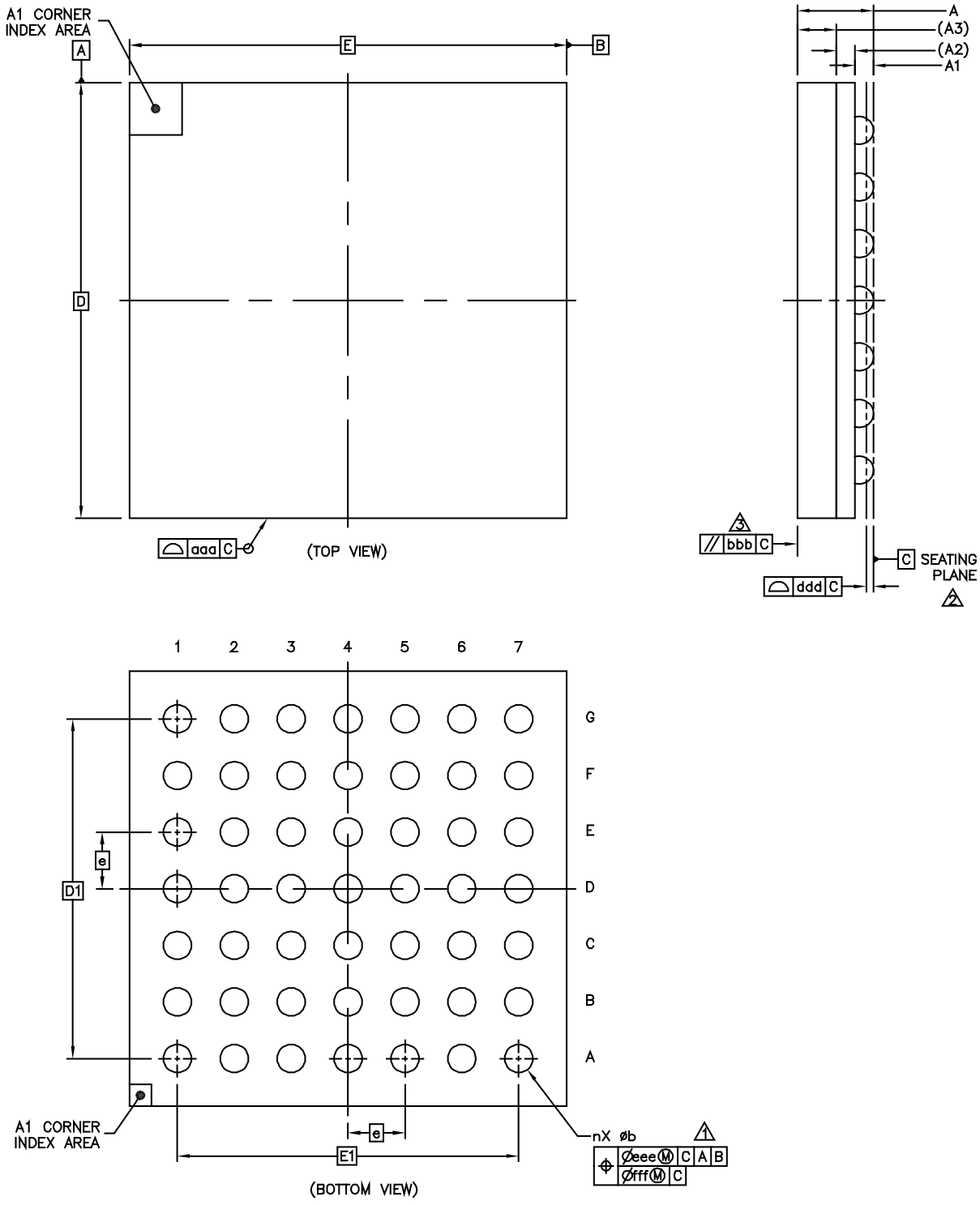


Figure 5-1. The B6NS Package.

Parameter	Symbol	Minimum	Nominal	Maximum
Total Thickness	A			1
Stand Off	A1	0.16		0.26
Substrate Thickness	A2		0.21 REF	
Mold Thickness	A3		0.45 REF	
Body Size	D		5 BSC	
	E		5 BSC	
Ball Diameter			0.3	
Ball Opening			0.275	
Ball Width	b	0.27		0.37
Ball Pitch	e		0.65 BSC	
Ball Count	n		49	
Edge Ball Center to Center	D1		3.9 BSC	
	E1		3.9 BSC	
Body Center to Contact Ball	SD			
	SE			
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

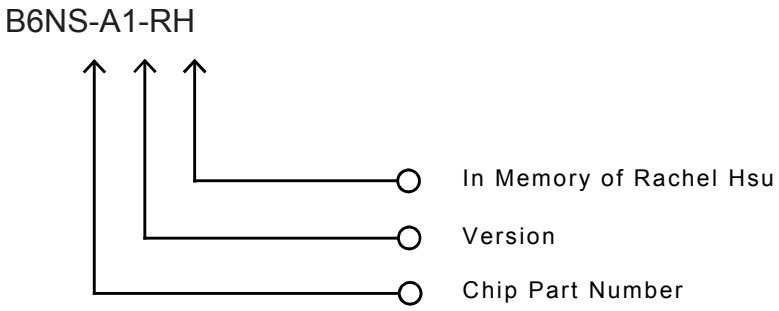
Table 5-1. Dimensions of the B6NS Package (millimeters).

Notes for table and figures:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
2. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.

6. CONTACT AND ORDER INFORMATION

All chips in the B6 series are Lead-Free, Halogen-Free and RoHS compliant.



For complete Ambarella's sales contact information, please visit www.sunnywale.com,search those keyword "B6SN" , "B6FN" or "Ambarella"

7. IMPORTANT NOTICE

All Ambarella design specifications, datasheets, drawings, files, and other documents (together and separately, "materials") are provided on an "*as is*" basis, and Ambarella makes no warranties, expressed, implied, statutory, or otherwise with respect to the materials, and expressly disclaims all implied warranties of noninfringement, merchantability, and fitness for a particular purpose. The information contained herein is believed to be accurate and reliable. However, Ambarella assumes no responsibility for the consequences of use of such information.

Ambarella Incorporated reserves the right to correct, modify, enhance, improve, and otherwise change its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

All products are sold subject to Ambarella's terms and conditions of sale supplied at the time of order acknowledgment. Ambarella warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used to the extent Ambarella deems necessary to support this warranty.

Ambarella assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Ambarella components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Ambarella does not warrant or represent that any license, either expressed or implied, is granted under any Ambarella patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Ambarella products or services are used. Information published by Ambarella regarding third-party products or services does not constitute a license from Ambarella to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Ambarella under the patents or other intellectual property of Ambarella.

Reproduction of information from Ambarella documents is not permissible without prior approval from Ambarella.

Ambarella products are not authorized for use in safety-critical applications (such as life support) where a failure of the product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Customers acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Ambarella products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by Ambarella. Further, Customers must fully indemnify Ambarella and its representatives against any damages arising out of the use of Ambarella products in such safety-critical applications.

Ambarella products are neither designed nor intended for use in military/aerospace applications or environments. Customers acknowledge and agree that any such use of Ambarella products is solely at the Customer's risk, and they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

8. REVISION HISTORY

Our goal is to provide our customers with the highest-quality documentation possible, and to continuously improve our publications to ensure that your experience with Ambarella's products is a positive one. If you have any questions or comments regarding this document, please contact the Technical Writing team at awin@sunnywale.com. Your feedback is welcomed and appreciated.

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	11 August 2017	New B6 Production Part
0.2	16 August 2017	Updated diagrams in Chapter 1 Overview Updated Table 4-2 Power Rails DC Characteristics - VDDI values and added a note
0.3	19 December 2017	Updated Pins AVDD18 & VDDO merged into VDD18, XOUT converted to VSSi Updated Table 3-8 System Pins- Changed description for C6 and C7 Updated Table 4-2 Power Rails DC Characteristics Values changed for VDDI
0.4	30 April 2018	Removed references for B6DNS Removed references for VOUT MIPI-DSI and open LDI Updated Figure 1-3 Removed B6DNS, SOC and B6NS, added A9AQ, Figure title updated. Updated Figure 4-1 Video Output Timing Removed "preliminary" wording