USB 2.0 Video

PC Camera Controller

SN9C5256

Datasheet

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Version: v0.01

Revision	Date	Description
0.01	2013_08_06	Formal Release
		For the latest data sheet, please visit www.sunnywale.com
Apply to		SN9C5256

Table of Contents

1 General Description

The SN9C5256 is a USB 2.0 High-Speed (HS) compatible PC camera controller. The low power design provides extreme low consumption on device standby, operation and even high performance state. The low thermal design gets the module operating temperature inside platform under reasonable range. The SN9C5256 is fully compliant with USB Video Class. The OS systems supported are including Windows XP, Windows Vista, Windows 7 and the coming Windows 8.

The new generation image signal processing engine brings sight video experience. The high performance Motion-JPEG compression engine makes variant compression ratio to consider bandwidth requirement well which output MJPG data format. It is also a high performance and high speed transmission engine on YUV un-compression data format. With the integrated sensor interface and color processing engine, it can supports most available CMOS sensors that range from VGA to QXGA. It is controlled by the embedded micro-controller and the statistics for 3A (AE / AWB / AF) are built-in.

To decrease the BOM cost and PCB area, the SN9C5256 integrates 2 voltage regulators for sensor power. One is for analog part and the other is for I/O power. Futhermore, the built-in Clock Synthesizer for performance and power saving makes an external crystal is not needed.

To fully meet Ultrabook requirement, one of the most significant of SN9C5256 is to save power consumption 40% less than previous backends. The Low Power Management Sleep State(LPM L1) is supported to save power consumption for host controller. The QFN46 4.5x6.5mm package dimension is also for the thin design.

The flexible architecture is consisted of mask ROM, internal RAM and external serial-flash which can stores the customized codes and parameters. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to fulfill customized features.

2 Features

2.1 System

- 3.3V, 1.2V power supply are necessary (Core power 1.2V provide by Backend IC)
- Extreme low power consumption, < 30mA when standby and < 0.5mA when suspend (Power consumption of sensor is not included)
- Built-in Clock Synthesizer for performance and power saving
- Built-in PLL for internal clock generation

- Using external serial flash to store customized code and data
- No external RAM needed
- 1.8V output power source to supply CMOS sensor's I/O power
- 2.8V output power source to supply CMOS sensor's analog power(2.7V~3.3V control by FW setting)
- QFN package of 46-pins

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 compliant
- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- USB Low Power Management Sleep State with RTD3
- 4 endpoints: CONTROL pipe, UVC Interrupt IN and Isochronous-IN (video, 24MB/s max)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Support QXGA(3.0MP, 2048x1536), FHD(2.0MP, 1920x1080), UXGA(2.0MP, 1600x1200), SXGA(1.3MP, 1280x1024), HD(1.0MP, 1280x720), VGA(0.3MP, 640x480) CMOS ISP sensor
- Support YUY2 and RAW (Bayer-Pattern) image data format from sensor
- Output clock: 480/(m*n) MHz output clock request of CMOS sensor silicon.
- Up to 96Mhz pixel clock is acceptable
- Support industrial standard 2-wire serial interface for sensor control

2.4 Color processing

- AE histogram statistics
- AWB window statistics
- AF edge window statistics
- On-the fly defect-pixel cancellation
- Lens shading compensation for R/G/B channel
- Low pass filter
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels

- Programmable color conversion matrix for R/G/B input
- Configurable noise reduction
- De-color aliasing in Edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation
- Auto Gamma for backlight preview
- Auto Frequency for MSOC

2.5 Scaling Engine

- Scale down on Y/Cb/Cr
- For QXGA / UXGA / SXGA / VGA sensors, combined scaling and windowing function provides similar view angle for QXGA / FHD / UXGA / SXGA / HD / SVGA / VGA / CIF / QVGA / QCIF / QQVGA output format
- Fine scaling(128/m, m:128 ~ 2047)

2.6 JPEG Encoder

- JPEG YUV422 baseline format
- Built-in JPEG encoder support USB Video Class MJPEG payload
- 128 bytes quantization tables for Y and C provide programmable compression ratio

2.7 Video / Still Image

- Output video / still image format:
  - USB Video Class Uncompressed YUY2 payload (16bits/pixel)
  - USB Video Class MJPG payload
- Video streaming up to 30fps@FHD at USB2.0 high-speed mode.
- Still Image capture up to QXGA and is able to support UVC still image capture method 1/2

2.8 Frame rate

- Frame rate considering USB bandwidth limitation

	Normal Resolution @ USB High-Speed									
Output format	QXGA	FHD	UXGA	SXGA	HD	SVGA	VGA	CIF	QVGA	QCIF
YUY2	3fps	5fps	6fps	9fps	12fps	25fps	30fps	30fps	60fps	60fps
MJPEG	24fps	30fps	30fps	60fps	60fps	120fps	120fps	120fps	120fps	120fps

- Frame rate considering sensor characteristic
  The maximum frame rate is limited by how many fps that sensor can output under acceptable maximum pixel clock

2.9 GPIO

- 3 GPIOs are predefined as following functions including LED control, serial flash write protect, sensor reset.
- GPIO_3 internal pull low（H:MIPI;L:parallel）..

2.10 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory, and maximum CPU clock rate is 24MHz
- Load extended F/W up to 64KB from external serial flash.
- Load VID/PID, manufacturer, product and serial number string from external serial flash.
- Load UVC parameter definition from external serial flash.
- F/W is upgradeable from PC
- Force USB at FS mode / Force USB disconnect
- Interrupt at the end of H/W windowing
- CPU watch dog

2.11 Pre-Defined for USB Video Class

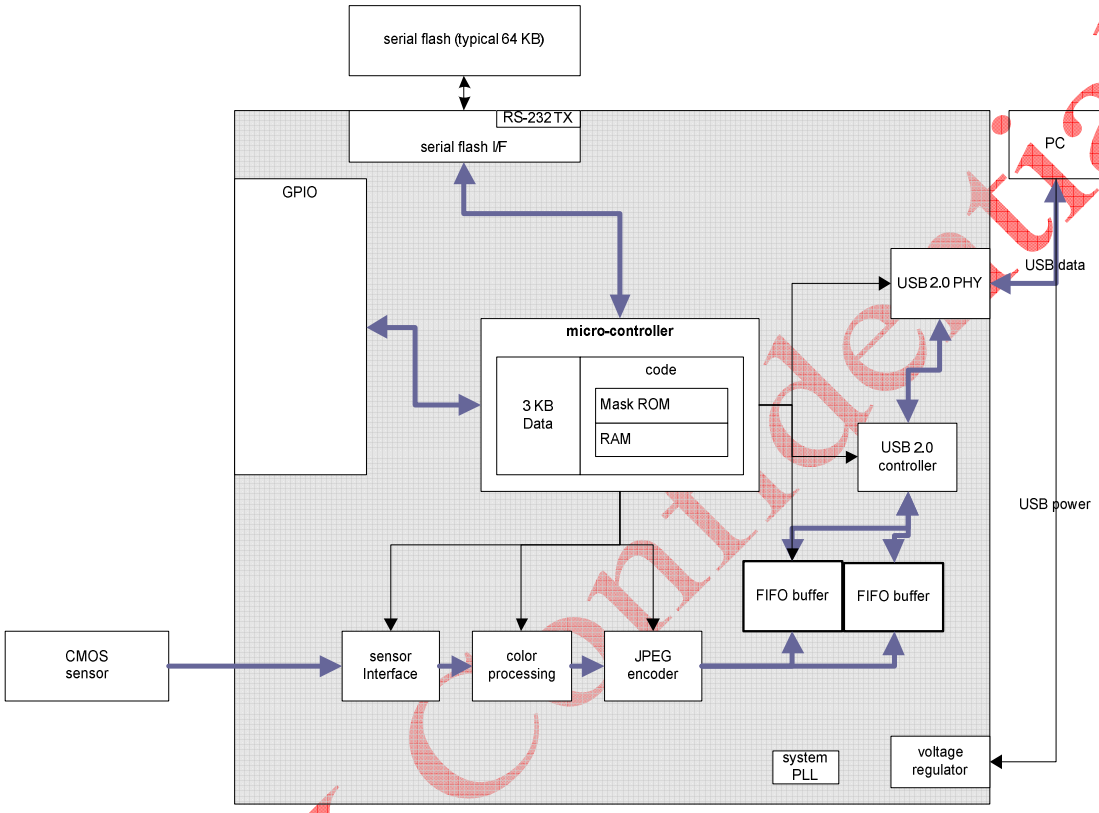
- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)
- LED indicator on video streaming
- UVC Extension unit support

2.12 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit, Microsoft Window 7 32bit, Microsoft Window 7 64bit, Microsoft Window 8
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

3 Function Block Diagram

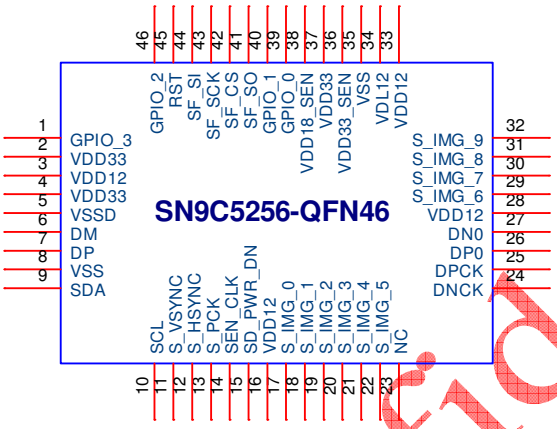
3.1 Block Diagram



4 Pin Assignment

4.1 SN9C5256 – 46 pins QFN

4.1.1 Pin-out Diagram



4.1.2 Pin Description

Pin No.	Pin Name	Description
1	GPIO_3	Internal pull low, H: MIPI; L: parallel.
2	VDD33	3.3V DSP system power
3	VDD12	1.2V DSP core power
4	VDD33	3.3V DSP system power
5	VSSD	GND
6	DM	D- for USB
7	DP	D+ for USB
8	VSS	GND
9	SDA	I²C data
10	SCL	I²C clock
11	S_VSYNC	Sensor vsync
12	S_HSYNC	Sensor hsync
13	S_PCK	Sensor pixel clock
14	SEN_CLK	Sensor clock
15	SD_PWR_DN	General purpose I/O
16	VDD12	1.2V DSP core power
17	S_IMG_0	Sensor image data
18	S_IMG_1	Sensor image data
19	S_IMG_2	Sensor image data

20	S_IMG_3	Sensor image data
21	S_IMG_4	Sensor image data
22	S_IMG_5	Sensor image data
23	NC	NC
24	DNCK	MIPI sensor clock lan n
25	DPCK	MIPI sensor clock lan p
26	DP0	MIPI sensor data lan1 p
27	DN0	MIPI sensor data lan1 n
28	VDD12	1.2V DSP core power
29	S_IMG_6	Sensor image data
30	S_IMG_7	Sensor image data
31	S_IMG_8	Sensor image data
32	S_IMG_9	Sensor image data
33	VDD12	1.2V DSP core power
34	VDL12	Internal LDO VOUT for DSP core power
35	VSS	GND
36	VDDA_SEN	Internal LDO VOUT for sensor analog power
37	VDD33	Internal LDO VIN
38	VDDIO_SEN	Internal LDO VOUT for sensor IO power
39	GPIO_0	General purpose I/O
40	GPIO_1	General purpose I/O
41	SF_SO	SPI data out to serial flash
42	SF_CS	Chip select to serial flash
43	SF_SCK	Clock to serial flash
44	SF_SI	SPI data in from serial flash
45	RST	Chip reset
46	GPIO_2	General purpose I/O

Direction denotation:

O	Output	OU	Output unknown	OH	Output high	OL	Output low
I	Input	B	Bi-direction	F	Firmware control		
A	Analog	P	Power	Po	Power Output		

5 Electrical Characteristics

5.1 DC operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD33_18	Power Supply	-0.3 ~ 3.6	V
DVDD	Power Supply	-0.12 ~ 1.32	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Typ	Units
VDD33	Power Supply	3.3	V
VDD33_18	Power Supply	3.3/1.8	V
DVDD	Power Supply	1.2	V
Vin	Input voltage	3.3	V

5.1.3 Low Dropout Regulator Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 ℃)

Symbol	Parameter	Typ	Units
VDDA1	Power Supply for 2.8V LDO	3.3	V
VO275	Voltage output of 2.8V LDO	2.85	V
IO275	Output current capacity of 2.8V LDO	100	mA
VDD33	Power Supply for 1.8V LDO	3.3	V
VO180	Voltage output of 1.8V LDO	1.85	V
IO180	Output current capacity of 1.8V LDO	150	mA

5.1.4 DC Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, VDD33_18=1.62 ~ 3.6V, Tj=0 to +70 ℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDD33_18)	Input low voltage	CMOS	-0.3		0.2*VDD33_18	V
Vih(VDD33_18)	Input high voltage	CMOS	0.8*VDD33_18		VDD33_18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.1.5 MIPI RX Electrical Characteristics

Low power mode electrical characteristics

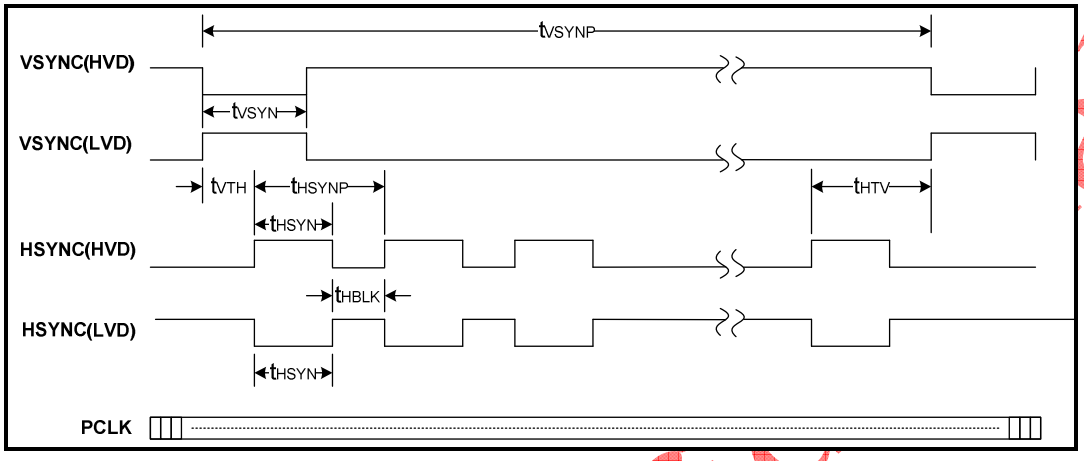
Symbol	Psrsmeter	Min	Typ	Max	Unit
VIH	Logic 1 input voitage	880			mV
VIL	Logic 0 input voltage,not in ULP state			550	mV
VHYST	Input hysteresis	25			mV

High power mode electrical characteristics

Symbol	Psrsmeter	Min	Typ	Max	Unit
VCMRX(DC)	Common mode voitage		200		mV
VID	Differential input voltage		200		mV
ZID	Differential input impedance	80		125	Ω

5.2 AC operating Condition

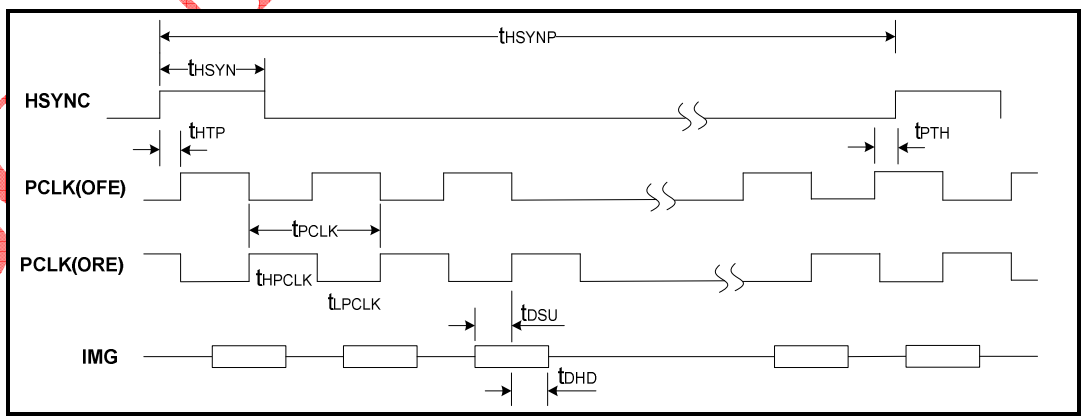
5.2.1 Sensor Interface



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	t_{VSYNC}	t_{PCLK}	-	-	ns
VSYNC to HSYNC	t_{VTH}	t_{PCLK}	-	-	ns
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
Blank time between two HSYNC	t_{HBLK}	t_{PCLK}	-	-	ns
HSYNC to VSYNC	t_{HTV}	t_{HSYNP}			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

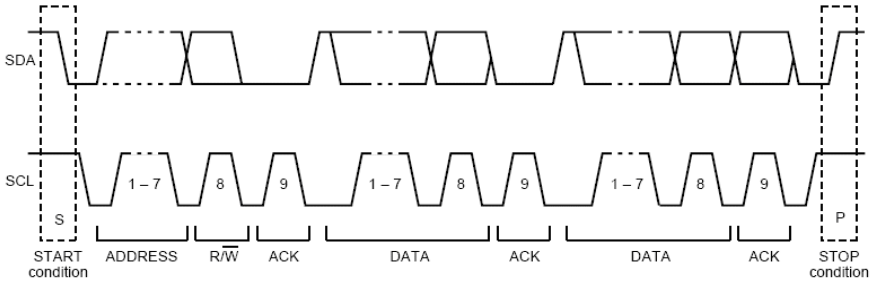


Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}			ns
PCLK to HSYNC	t_{PTH}	t_{SENCK}			ns
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock (YUV Mode)	f_{PCLK}	-	-	96	MHz
Frequency of pixel clock (RAW Data Mode)	f_{PCLK}	-	-	60	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

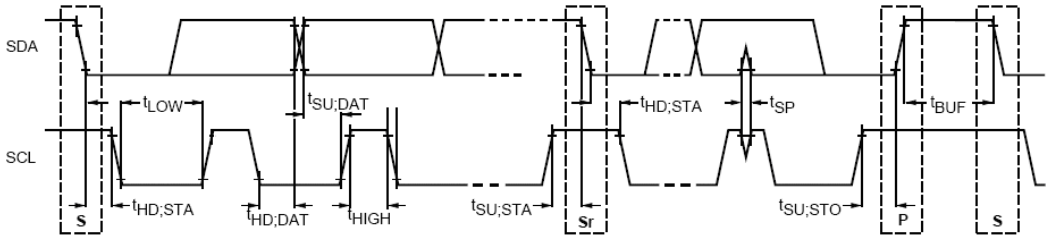
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge

5.2.2 I2C Control Interface



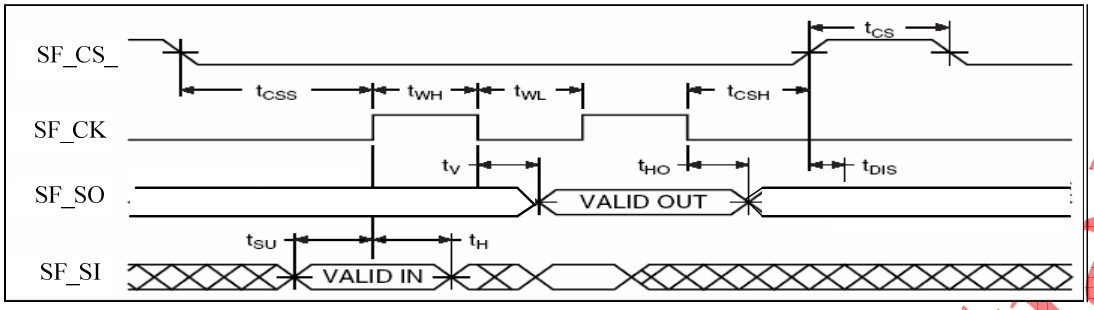
A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write	$t_{HD:DAT}$	-	2533	-	-	633	-	ns
Data hold time: Read	$t_{HD:DAT}$	10	-	-	10	-	-	ns
Data setup time: Write	$t_{SU:DAT}$	-	2533	-	-	633	-	ns
Data setup time: Read	$t_{SU:DAT}$	10	-	-	10	-	-	ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.3 Serial Flash Interface



When f_{SCK} = 24 Mhz (SPEED=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

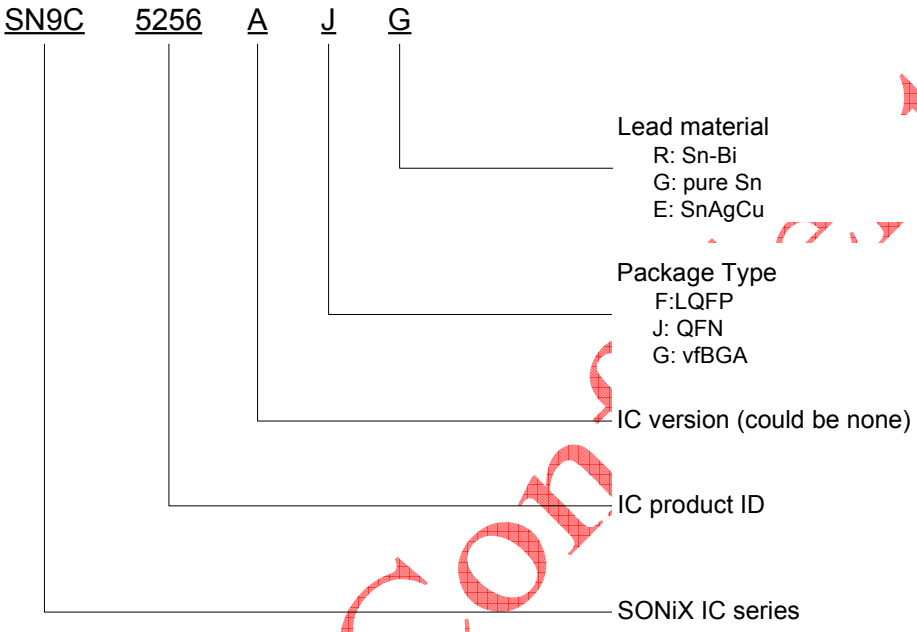
When f_{SCK} = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

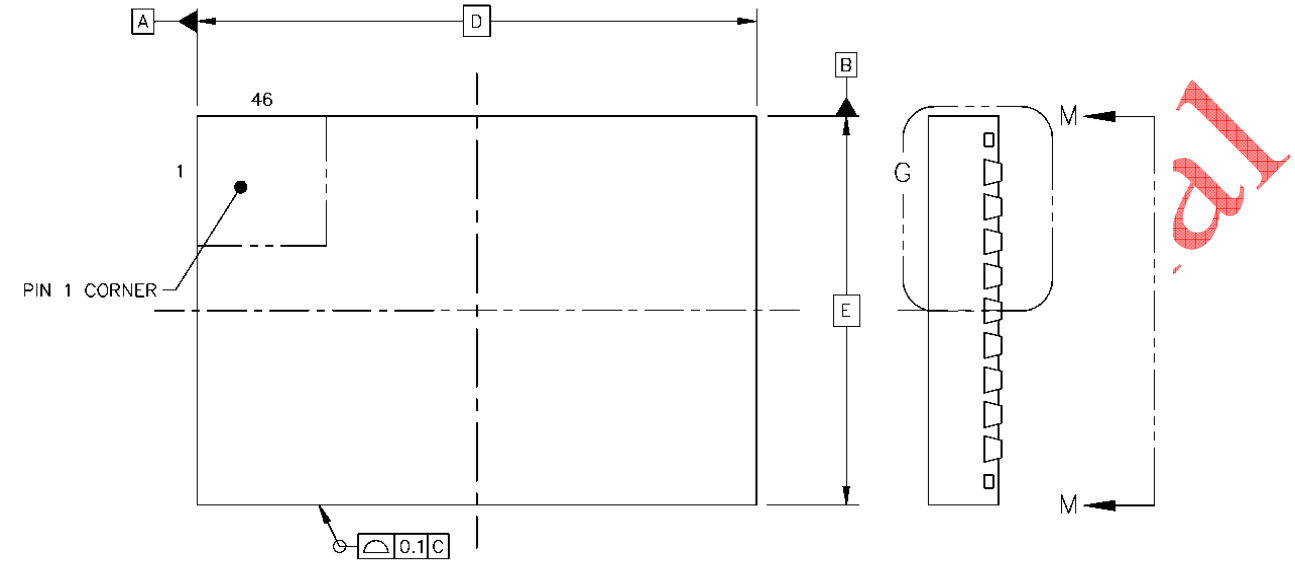
6 Package Information

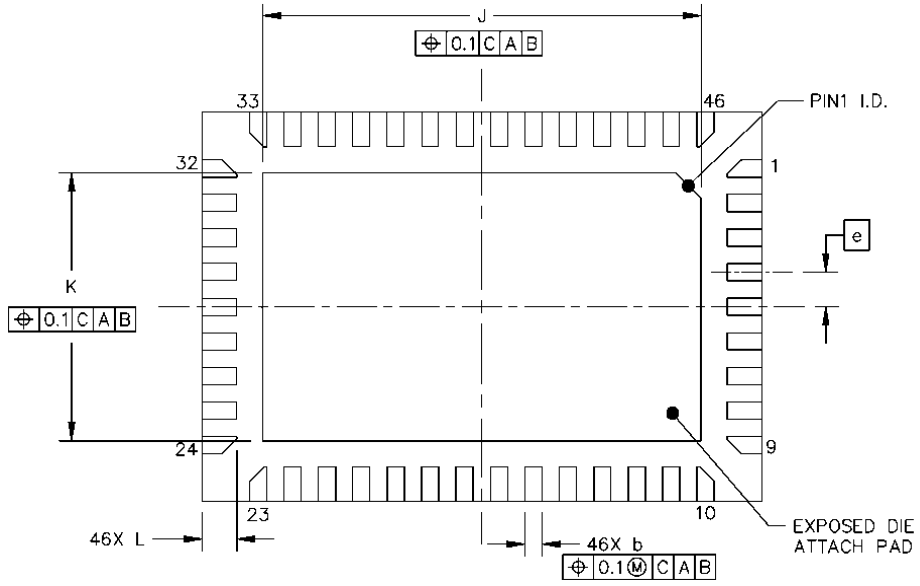
6.1 Nomenclature

Example:

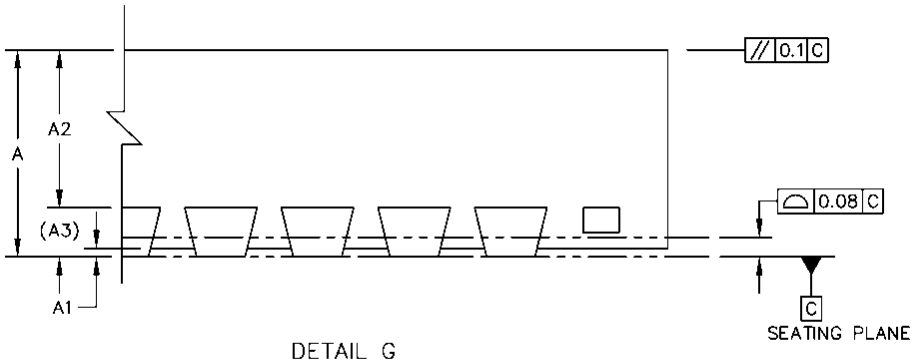


6.2 46 pins QFN





VIEW M–M



DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	0.67
A3		0.203 REF.	
b	0.15	0.2	0.25
D		6.5 BSC	
E		4.5 BSC	
e		0.4 BSC	
J	5	5.1	5.2
K	3	3.1	3.2
L	0.35	0.4	0.45

NOTES

1.0 COPLANRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---

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