I²C Programmable Multi-Channel PMU with Battery Charger for CMOS DSC/DV

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General Description

The RT5024 is a complete power supply solution for digital still cameras and other hand held devices. The RT5024 is composed of multi-channel DC-DC power converter unit, a single-cell linear Li+ ion battery charger, a charger type detector, and an I²C control interface.

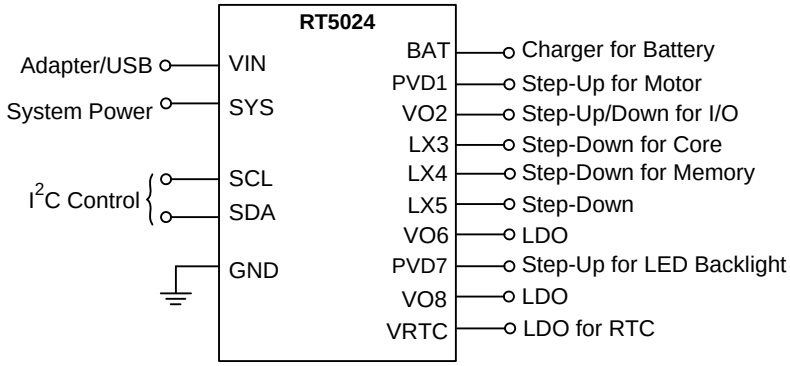
The power converter unit includes one synchronous step-up converter (CH1), one synchronous step-up/down converter (CH2), three synchronous step-down converters (CH3/4/5), two LDOs with input power as low as 1.5V (CH6/8), one WLED driver in synchronous high-voltage step-up mode or low-voltage current regulator mode (CH7), and a keep-alive LDO (CH9) for RTC application. All converters are internally frequency compensated and integrate power MOSFETs. The power converter unit provides complete protection functions : over current, thermal shutdown, over voltage and under voltage protection. The RT5024 has a WAKEUP impulse generation circuitry to monitor VIN or BAT installation event. To fulfill most of applications, the RT5024 has six preset power on/off sequences.

The battery charger includes Auto Power Path Management (APPM). No external MOSFETs are required. The charger can enter sleep mode when power is removed.

Charging tasks are optimized by using a control algorithm to vary the charge rate, including pre-charge mode, fast charge mode and constant voltage mode. The charge current can also be programmed by the I²C control interface. The battery regulation voltage and current can be adjusted by JEITA standard temperature control or other schemes set by the I²C interface. The internal thermal feedback circuitry regulates the die temperature to optimize the charge rate for all ambient temperatures. The charging task will always be terminated in constant voltage mode when the charging current reduces to the termination current of 10% x I_{CHG_FAST}. The charger includes under voltage and over voltage protection for the supply input voltage, VIN. The charger includes USB charger detection circuitry via D+ and D– pins of USB interface to detect USB Standard Downstream Ports (SDP), USB Charging Downstream Port (CDP), Dedicated Charger Port (DCP), or Apple/Sony charger ports. The RT5024 uses some indicators to show charger states : one open drain port $\overline{CHG}$ (charger status), and an interrupt ($\overline{INT}$) to immediately notify the state change.

The RT5024 is available in the WQFN-40L 5x5 package.

Simplified Application Circuit



Features

Power Converter Unit

- CH1 LV Sync Step-Up
  - Support Up to 1A Loading, DVS (Dynamic Voltage Scaling), Load-Disconnect, Up to 95% Efficiency, PSM/PWM Selectable
- CH2 LV Sync Step-Up/Down
  - Support Up to 1A Loading, DVS, Up to 95% Efficiency, PSM/PWM Selectable
- CH3/4 LV Sync Step-Down
  - Support Up to 1.3A Loading, DVS, Up to 95% Efficiency, 100% (max) Duty Cycle, PSM/PWM Selectable
- CH5 LV Sync Step-Down
  - Support Up to 0.6A Loading, Up to 95% Efficiency, 100% (max) Duty Cycle
  - Output Voltage can be Selected from Preset List or Set by External Feedback Network.
- CH6 Low Input Power LDO
  - VIN Range 1.5V to 5.5V
  - Output Voltage Level Selectable in I^2C Register
- CH7 WLED Driver in Either Sync Step-Up Operation or Current Regulator Operation
  - Step-Up Mode with LED Open Protection (OVP7 16V or 25V, Selectable in I^2C Register)
  - Step-Up Mode Support Series 2 to 6 WLED and Load Disconnect Function
  - Current Regulator Mode for 1 WLED
  - 31 WLED Dimming Levels
  - Automatic Mode Selection by External Circuit Topology
- CH8 Generic LDO
  - VIN Range 1.5V to 5.5V
  - Output Voltage Level Selectable in I^2C Register
- CH9 Low Quiescent LDO with Reverse Leakage Prevention for RTC Power Supply
  - Fixed 3.25V Output
- Six Preset Power On/Off Sequences by One Pin SEQ
  - SEQ # 0 : CH2→CH3→CH4
  - SEQ # 1 : CH1→CH3→CH2→CH4
  - SEQ # 2 : CH1→CH3→CH4→CH2
  - SEQ # 3 : CH1→CH2→CH4→CH3
  - SEQ # 4 : CH1→CH4→CH3→CH2→CH5
  - SEQ # 5 : CH1→CH4→CH2→CH3
- All Power Switches Integrated with Internal Compensation
- Discharge Output of Every Channels when Turning Off
- Wake Up Impulse to Monitor BAT and VIN Plug-In
- Fixed 2MHz Switching Frequency for CH1/3/4/5, Fixed 1MHz Switching Frequency for CH2/7

Charger Unit

- 28V Maximum Rating for VIN Power
- Selectable Power Input Current Limit (0.1A / 0.5A / 1A / 1.5A)
- Auto Power Path Management (APPM) with Integrated Power MOSFETs
- Battery Charging Current Control and Regulation Voltage Control
- Programmable Charging Current and Safe Charge Timer
- Optimized Charge Rate via Thermal Feedback
- Under Voltage Protection, Over Voltage Protection
- Charger Status Indicator
- Interrupt Indicator to JEITA Temperature/Fault/Status Events when PMU is Enabled
  - Battery Temperature Events
  - Battery Removing Event
  - Charger in Thermal Regulation Control
  - Safety Timer Timeout
  - End of Charging
  - VIN Power Good
  - VIN < DPM Threshold 4.35V
  - Charger Type Detection Finishing
- Charger Type Detection
  - Dedicated Charger : Support Apple and Sony Charger
  - Secondary Charger Detection to Distinguish CDP and DCP
- I^2C Control Interface : Support Fast Mode up to 400kb/s
- Small 40-Lead WQFN 5x5 Package
- RoHS Compliant and Halogen Free

Applications

- DSC Power Supply System
- CMOS-Sensor DV
- Portable Instruments

Ordering Information

RT5024 □□

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

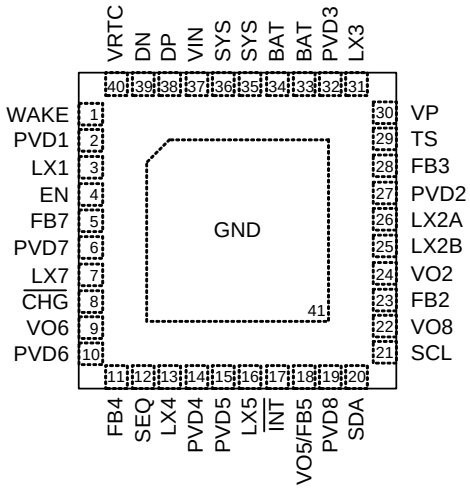
Marking Information

RT5024GQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



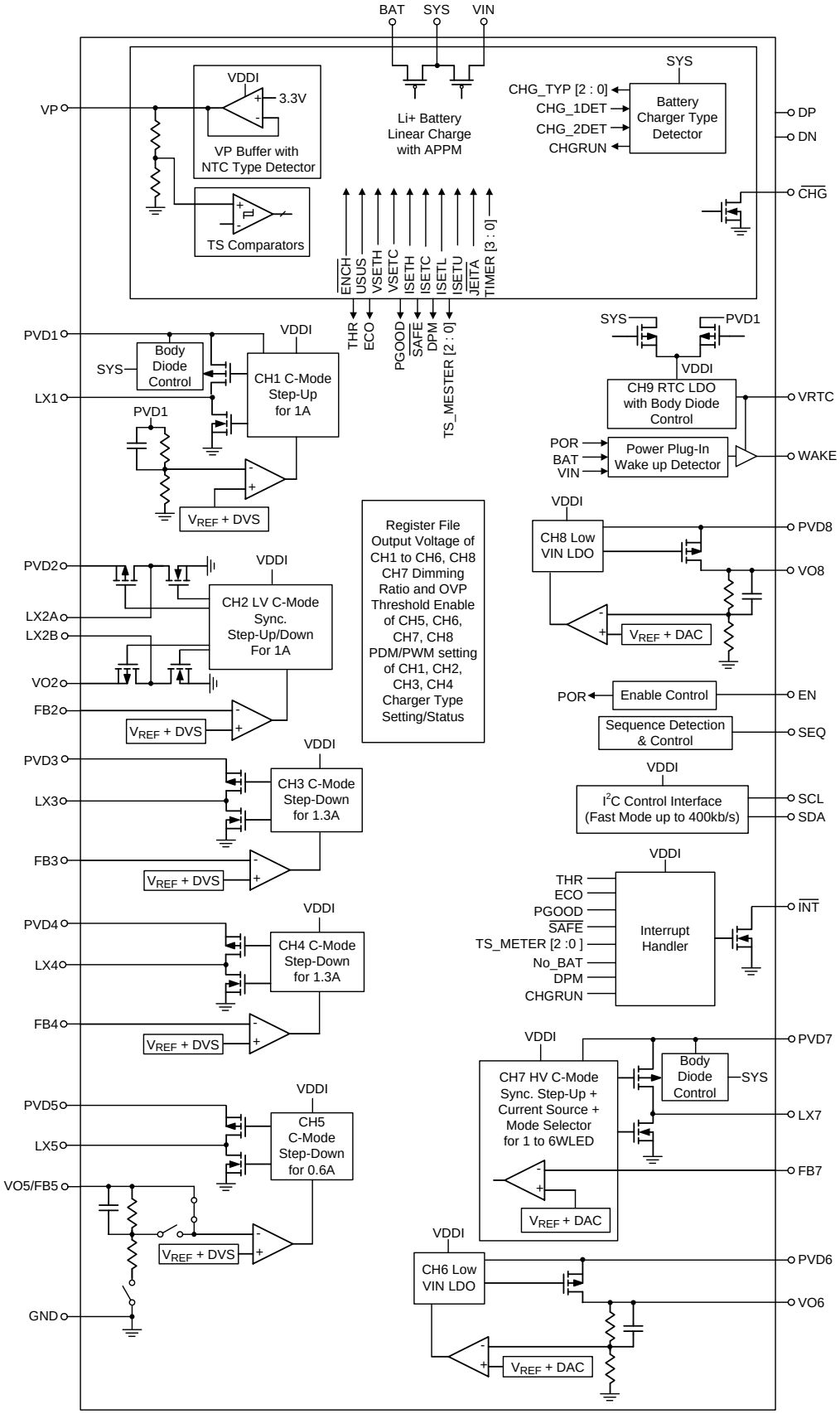
WQFN-40L 5x5

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	WAKE	Wake-Up Impulse Push Pull Output. If VIN or BAT plug in, WAKE pin generates one 90ms width high pulse to notify micro processor.
2	PVD1	Power Output of CH1. To make CH1 stable, the power path from the pin PVD1 to its output capacitors must be as short (≤1mm is better) and wide as possible to reduce its parasitic inductance. The output capacitor must be ceramic capacitor (≥20μF).
3	LX1	Switch Node of CH1.
4	EN	Enable Control Input of Power Converter.
5	FB7	Feedback Input of CH7 in Step-Up Mode or Current Regulator Mode.
6	PVD7	Power Output of CH7 in Step-up or Power input pin of CH7 in current regulator mode.
7	LX7	Switch Node of CH7 in Step-Up Mode. LX7 initial voltage determine CH7 operation mode.
8	$\overline{CHG}$	Charger Status Output. Open-drain port.
9	VO6	Power Output of CH6.
10	PVD6	Power Input of CH6.
11	FB4	Feedback Input of CH4.
12	SEQ	Power Sequence Selection for CH1 to CH4. SEQ #4 included CH5.
13	LX4	Switch Node of CH4.
14	PVD4	Power Input of CH4.
15	PVD5	Power Input of CH5.
16	LX5	Switch Node of CH5.
17	$\overline{INT}$	Interrupt Indicator Open Drain Output. If events of NoBAT, THR, EOC, Battery Temperature Change (TS_METER), PGOOD, $\overline{SAFE}$, VIN DPM, or Charge Type Detection Finishing (CHGRUN) happen, the output $\overline{INT}$ goes low and the INT bit in I^2C register bank 0x9 is set to be “1”. After INT bit is written to be “0”, $\overline{INT}$ goes high.
18	VO5/FB5	Output Voltage Sense or Feedback Network Input of CH5. The function is selected by I^2C register.
19	PVD8	Power Input of CH8.
20	SDA	Data Signal of I^2C Interface.
21	SCL	Clock Signal of I^2C Interface.
22	VO8	Power Output of CH8.
23	FB2	Feedback Input Pin of CH2.
24	VO2	Power Output of CH2.
25	LX2B	Switch Node B of CH2.
26	LX2A	Switch Node A of CH2.
27	PVD2	Power Input of CH2.
28	FB3	Feedback Input of CH3.
29	TS	Temperature Sense Input. The TS pin connects to a battery’s thermistor to determine if the battery is too hot or too cold to charge. If the battery’s temperature is out of range, charging is paused until it re-enters the valid range. TS also detects whether the battery (with NTC) is present or not.

Pin No.	Pin Name	Pin Function
30	VP	Power Output Pin of 3.3V Buffer for Battery Temperature Sensing.
31	LX3	Switch Node of CH3.
32	PVD3	Power Input Pin of CH3.
33, 34	BAT	Charger Output for Battery.
35, 36	SYS	Power Output for System. Connect this pin to System with a minimum 10μF ceramic capacitor to GND.
37	VIN	Supply Voltage Input.
38	DP	USB D+ Input for Charger Type Detection.
39	DN	USB D− Input for Charger Type Detection.
40	VRTC	RTC LDO Power Output Pin.
41 (Exposed pad)	GND	Exposed PAD Should be Soldered to PCB and Connected to GND.

Functional Block Diagram



Operation

The RT5024 is an integrated power solution for digital still cameras and other small handheld devices. It includes six DC-DC converters, a WLED driver, a RTC LDO and a fully integrated single-cell Li-ion battery charger.

CH1 : Step-Up DC-DC Converter

CH1 is a step-up converter for motor driver power. The converter operates at PFM or PWM current mode which can be set by I^2C interface.

CH2 : Step-Up/Down DC-DC Converter

CH2 is a step-up/down converter for I/O power. The converter operates at PFM or PWM current mode which can be set by I^2C interface.

CH3 : Step-Down DC-DC Converter

CH3 is a step-down converter for core power. The converter operates at PFM or PWM current mode which can be set by I^2C interface.

CH4 : Step-Down DC-DC Converter

CH4 is a step-down converter for memory power. The converter operates at PFM or PWM current mode which can be set by I^2C interface.

CH5 : Step-Down DC-DC Converter

CH5 is a step-down converter. The converter operates at PFM/PWM current mode.

CH6 : Generic LDO

CH6 is a generic low voltage LDO for multiple purpose power.

CH7 : WLED Driver

CH7 is a WLED driver that can operate in either current source mode or synchronous step-up mode which is determined by I^2C interface control signal.

CH8 : Generic LDO

CH8 is a generic low voltage LDO for multiple purpose power.

CH9 : Keep Alive LDO and RTC

CH9 is a LDO providing a 3.25V output for real time clock.

Charger Unit

A Li-ion battery charger with automatic power path management is designed to operate in below modes.

Pre-Charge Mode

When the output voltage is lower than 2.8V, the charging current will be reduced to a ratio of fast-charge current set by A8.ISETA [3:0] to protect the battery life-time.

Fast-Charge Mode

When the output voltage is higher than 3V, the charging current will be equal to the fast-charge current set by A8.ISETA [3:0].

Constant Voltage Mode

When the output voltage is near 4.2V and the charging current falls below the termination current for a deglitch time of 25ms, the charger will be turned off and $\overline{CHG}$ will go to high.

Re-Charge Mode

When the chip is in charge termination mode, the charging current gradually goes down to zero. Once the battery voltage drops to below 4.1V for 100ms, the charger will resume charging operation.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, SYS ---------- –0.3V to 6V
- Supply Input Voltage, VIN ---------- –0.3V to 28V
- Switch Node Voltage, LX1, LX2, LX3, LX4, LX5 ---------- –0.3V to 6V
- PVD7, LX7 ---------- –0.3V to 25V
- $\overline{CHG}$ ---------- –0.3V to 28V
- Other Pins ---------- –0.3V to 6V
- $\overline{INT}$, $\overline{CHG}$ Continuous Current ---------- 20mA
- BAT Continuous Current (Total in two pins) ---------- 2.5A
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 27.5°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, BAT ---------- 1.8V to 5.5V
- Supply Input Voltage Range, VIN (A7.ISETL = 1) ---------- 4.4V to 6V
- Supply Input Voltage Range, VIN (A7.ISETL = 0) ---------- 4.5V to 6V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

Power Converter Unit :

(V_{SYS} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
PMU Startup Voltage at SYS	V_{ST}	For bootstrap	2.4	--	--	V
SYS Operating Voltage for PMU	V_{SYS}		2.7	--	5.5	V
VDDI Over Voltage Protection (OVP) (Hysteresis High)			5.82	6	6.18	V
VDDI OVP Hysteresis (Gap)			--	–0.25	--	V
VDDI UVLO (Hysteresis High)		VDDI UVLO takes effect once CH2 soft-start finish	2.2	2.4	2.6	V
VDDI UVLO Hysteresis (Gap)			--	–0.3	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Shutdown Supply Current into BAT (Include I_{DDQ} of RTC LDO)	$I_{OFF-BAT}$	EN = L, and PMU off, BAT = 4.2V	--	10	20	μA
CH1 + CH2 + CH3 + CH4 Supply Current	I_{Q1234}	Non switching, EN = 3.3V	--	--	2000	μA
CH5 Supply Current	I_{Q5}	Non switching, A2.EN5 = 1	--	--	500	μA
CH6 Supply Current	I_{Q6}	A2.EN6 = 1	--	--	100	μA
CH7 in Step-Up Mode Supply Current	I_{Q7b}	Non switching, A2.EN7_DIM7 [4 : 0] = 5'b11111	--	--	500	μA
CH7 in Current Source mode Supply Current	I_{Q7c}	A2.EN7_DIM7 [4 : 0] = 5'b11111 PVD7 = 5V	--	--	400	μA
CH8 Supply Current	I_{Q8}	A2.EN8 = 1	--	--	100	μA
Oscillator						
CH1, 3, 4, 5 Operation Frequency	f_{OSC_1345}		1800	2000	2200	kHz
CH2, 7 Operation Frequency	f_{OSC_27}	CH7 in Step-Up mode	900	1000	1100	kHz
CH1 LV Sync Step-Up						
Output Voltage Accuracy at PVD1		Target voltage defined at A4.VOUT1 [3 : 0]	–1.5	--	1.5	%
Minimum On-Time for PSM			--	100	--	ns
Soft-Start Time		PVD1 = 0 to 5V	--	4	--	ms
Maximum Duty Cycle (Step-Up)		PVD1 < Target defined in A4.VOUT1 [3 : 0]	80	83	86	%
On Resistance of MOSFET	$R_{DS(ON)\_P}$	P-MOSFET, PVD1 = 3.3V	--	200	300	mΩ
	$R_{DS(ON)\_N}$	N-MOSFET, PVD1 = 3.3V	--	150	250	
Current Limitation (Step-Up)	I_{LIM_1}		2.2	3	4	A
Over Voltage Protection at PVD1			5.82	6	6.18	V
Under Voltage Protection -1 at PVD1			--	SYS – 0.8	--	V
Under Voltage Protection -2 at PVD1		Target Voltage is defined in A4.VOUT1 [3 : 0]	--	Target x 0.5	--	V
Over Load Protection at PVD1		Target Voltage is defined in A4.VOUT1 [3 : 0]	--	Target – 0.6	--	V
Off Discharge Current at PVD1		PVD1 = 5V, SYS = 3.3V	--	20	--	mA
Discharge Finishing Threshold at PVD1			--	0.6	--	V
CH2 LV Sync Step-Up/Down						
Feedback Regulation Voltage at FB2		A4.FB2 [2 : 0] = 3'b100	0.788	0.8	0.812	V
Soft-Start Time		FB2 = 0 to 0.8V	--	4	--	ms
Maximum Duty Cycle		LX2B	--	55	--	%
		LX2A	--	--	100	
On Resistance of MOSFET	$R_{DS(ON)\_2A}$	LX2A – GND, N-MOSFET PVD2 = 3.3V	--	200	300	mΩ
		PVD2 – LX2A, P-MOSFET PVD2 = 3.3V	--	150	250	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Resistance of MOSFET	$R_{DS(ON)\_2B}$	VO2 – LX2B, P-MOSFET, VO2 = 3.3V	--	200	300	mΩ
		LX2B – GND, N-MOSFET VO2 = 3.3V	--	150	250	
Current Limitation	I_{LIM_2}	Both P-MOSFET (PVD2 – LX2A) and N-MOSFET (LX2B – GND)	2	2.5	3	A
Over Voltage Protection at VO2			5.82	6	6.18	V
Under Voltage Protection at FB2		Target voltage is the chosen one in A4.FB2 [2 : 0]	--	0.4	--	V
Over Load Protection at FB2			--	Target – 0.1	--	V
Off Discharge Current at VO2		VO2 = 3.3V, SYS = 3.3V	--	20	--	mA
Discharge Finishing Threshold at VO2			--	0.1	--	V
CH3 LV Sync Step-Down						
Feedback Regulation Voltage at FB3		A5.FB3 [2 : 0] = 3'b100	0.788	0.8	0.812	V
Minimum On-Time for PSM			--	50	--	ns
Maximum Duty Cycle		FB3 = 0.75V	--	--	100	%
Soft-Start Time		FB3 = 0 to 0.8V	--	4	--	ms
On Resistance of MOSFET	$R_{DS(ON)\_P}$	P-MOSFET, PVD3 = 3.3V	--	200	300	mΩ
	$R_{DS(ON)\_N}$	N-MOSFET, PVD3 = 3.3V	--	150	250	
Current Limitation	I_{LIM_3}		1.3	1.8	2.4	A
Under Voltage Protection at FB3			0.35	0.4	0.45	V
Over Load Protection at FB3		Target voltage is the chosen one in A5.FB3 [2 : 0]	--	Target – 0.1	--	V
Off Discharge Current at LX3		LX3 = 1V, SYS = 3.3V	--	20	--	mA
Discharge Finishing Threshold at FB3			--	0.1	--	V
CH4 LV Sync Step-Down						
Feedback Regulation Voltage at FB4		A5.FB4 [2 : 0] = 3'b100	0.788	0.8	0.812	V
Minimum On-Time for PSM			--	50	--	ns
Maximum Duty Cycle		FB4 = 0.75V	--	--	100	%
Soft-Start Time		FB4 = 0 to 0.8V	--	4	--	ms
On Resistance of MOSFET	$R_{DS(ON)\_P}$	P-MOSFET, PVD4 = 3.3V	--	300	400	mΩ
	$R_{DS(ON)\_N}$	N-MOSFET, PVD4 = 3.3V	--	200	300	
Current Limitation	I_{LIM_4}		1.3	1.8	2.4	A
Under Voltage Protection at FB4			0.35	0.4	0.45	V
Over Load Protection at FB4		Target voltage is the chosen one in A5.FB4 [2 : 0]	--	Target – 0.1	--	V
Off Discharge Current at LX4		LX4 = 1V, SYS = 3.3V	--	20	--	mA
Discharge Finishing Threshold at FB4			--	0.1	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH5 LV Sync Step-Down						
Output Voltage Accuracy at VO5		Target voltage defined at A6.VOUT5 [3 : 0] = 4'b1000 to 4'b1111	–1.5	--	1.5	%
		Target voltage defined at A6.VOUT5 [3 : 0] = 4'b0001 to 4'b0111	–2	--	2	
Feedback Regulation Voltage at FB5		A6.VOUT5 [3 : 0] = 4'b0000	0.788	0.8	0.812	V
Maximum Duty Cycle			--	--	100	%
Soft-Start Time		VO5 = 0V to Target	--	4	--	ms
On Resistance of MOSFET	$R_{DS(ON)\_P}$	P-MOSFET, PVD5 = 3.3V	--	400	550	mΩ
	$R_{DS(ON)\_N}$	N-MOSFET, PVD5 = 3.3V	--	250	400	
Current Limitation	I_{LIM_5}		1	1.5	2	A
Under Voltage Protection at VO5			--	Target x 0.5	--	V
		Target voltage is the chosen one in A6.VOUT5 [3 : 0] = 0000 (FB5 = 0.8)	--	Target – 0.1	--	
		Target voltage is the chosen one in A6.VOUT5 [3 : 0] = 0001 to 0111	--	Target – 0.167	--	
		Target voltage is the chosen one in A6.VOUT5 [3 : 0] = 0111 to 1111	--	Target – 0.25	--	
Over Load Protection at VO5			--	TBD	--	V
Off Discharge Current at VO5		VO5 = 1.8V, SYS = 3.3V	--	30	--	mA
Discharge Finishing Threshold at VO5			--	0.1	--	V
CH6 LDO						
Input Voltage Range (PVD6)			1.5	--	5.5	V
Quiescent Current into PVD6		PVD6 = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage Accuracy at VO6		A6.VOUT6 [3 : 0] = 4'b1000 to 4'b1111	–1.5	--	1.5	%
		A6.VOUT6 [3 : 0] = 4'b0000 to 4'b0111	-2	--	2	
Drop Out Voltage (PVD6 – VO6)		I_{OUT} = 300mA, VO6 = 1.3V	--	--	0.15	V
PSRR+		I_{OUT} = 10mA, PVD8 = 3.3V at 1kHz	--	–40	--	dB
Max Output Current (Current Limit)		PVD6 = 3.3V	400	550	700	mA
Off Discharge Current at VO6		SYS = 3.3V	--	--	10	mA
CH7 WLED Driver						
Feedback Regulation Voltage at FB7 (Both Step-Up and Current)		A2.EN7_DIM7 [4 : 0] = 5'b11111	0.237	0.25	0.263	V
Minimum On-Time for PSM (Step-Up)			--	300	--	ns
Maximum Duty Cycle (Step-Up mode)		FB7 = 0.15V	91	93	97	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Resistance of MOSFET	$R_{DS(ON)\_P}$	P-MOSFET, PVD7 = 10V	--	2	3	Ω
	$R_{DS(ON)\_N}$	N-MOSFET, SYS = 3.3V	--	0.9	1.1	
Current Limitation (Step-Up mode)		N-MOSFET, SYS = 3.3V	0.6	0.8	1	A
Over Voltage Protection at PVD7 (Step-Up mode)		A0.OVP7 = 0	15	16	17	V
		A0.OVP7 = 1	24	25	26	
Off Discharge Current at PVD7 (Step-Up mode)		PVD7 = 10V, SYS = 3.3V	--	20	--	mA
Discharge Finishing Threshold at PVD7		(Step-Up Mode)	--	SYS–0.4	--	V
CH8 LDO						
Input Voltage Range (PVD8)			1.5	--	5.5	V
Quiescent Current into PVD8	I_{Q_PVD8}	PVD8 = 3.3V, I_{OUT} = 0mA	--	--	75	μA
Regulation Voltage Accuracy at VO8		A3.VOUT8 [3 : 0] = 4'b1000 to 4'b1111	–1.5	--	1.5	%
		A3.VOUT8 [3 : 0] = 4'b0000 to 4'b0111	-2	--	2	
Drop Out Voltage (PVD8 – VO8)		I_{OUT} = 300mA, VO8 = 2.5V	--	--	0.2	V
PSRR+		I_{OUT} = 10mA, PVD8 = 3.3V at 1kHz	--	-40	--	dB
Max Output Current (Current Limit)		PVD8 = 3.3V	300	450	600	mA
Off Discharge Current at VO8		SYS = 3.3V	--	--	10	mA
CH9 RTC LDO						
Standby Quiescent Current		BAT = 4.2V	--	3	6	μA
Lockout Current into VRTC	$I_{LO-VRTC}$	EN = L, and PMU off, BAT = 0V, VRTC = 3.25V, SYS = 0V	--	--	1	μA
Regulation Voltage at VRTC		I_{OUT} = 0mA	3.2	3.25	3.3	V
Max Output Current (Current Limit)		BAT = 4.2V	60	130	200	mA
Dropout Voltage at (BAT-VRTC)		I_{OUT} = 50mA	--	--	1000	mV
		I_{OUT} = 10mA	--	--	150	
		I_{OUT} = 3mA	--	--	60	
Wake Up Detector						
WAKE Impulse High Duration	t_{WAKEUP}	VIN or BAT plug in, VRTC = 3.25V	47	70	93	ms
WAKE UP High Level	V_{WAKE_H}	Source Current 0.5mA, VRTC = 3.25V	--	VRTC –0.3V	VRTC	V
WAKE UP Low Level	V_{WAKE_L}	Sink Current 0.5mA, VRTC = 3.25V	0	0.3	--	V
WAKE UP Rising Time	t_{WAKE_R}	C_{LOAD} 100pF at WAKE pin, 10% to 90% of VRTC, VRTC = 3.25V	--	--	1	μs
BAT Wake Up Threshold Voltage		VRTC = 3.25V	2.6	2.7	2.8	V
BAT Wake Up Threshold Hysteresis Gap		VRTC = 3.25V	--	–0.3	--	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Wake Up Threshold Voltage			VRTC = 3.25V	3.15	3.3	3.45	V
VIN Wake Up Threshold Gap			VRTC = 3.25V	--	–0.24	--	V
Control							
EN Input Voltage	High-Level			1.3	--	--	V
	Low-Level			--	--	0.4	
EN Pull Down Current				--	1	3	μA
SEQ Pull High Threshold for Power Sequence #0				0.2	--	--	V
SEQ Pull Down Resistance for Power Sequence #1			BAT = SYS = 2.7V	25	40	64	kΩ
SEQ Pull Down Resistance for Power Sequence #2			BAT = SYS = 2.7V	6.25	10	16	kΩ
SEQ Pull Down Resistance for Power Sequence #3			BAT = SYS = 2.7V	1.56	2.5	4	kΩ
SEQ Pull Down Resistance for Power Sequence #4			BAT = SYS = 2.7V	--	0.63	1	kΩ
SEQ Pull Low Threshold for Power Sequence #4				--	--	0.2	V
SEQ Pull Down Resistance for Power Sequence #5			BAT = SYS = 2.7V	100	160	--	kΩ
Power Sequence Time Gap			From previous channel starting to next channel starting	9	10	11	ms
Protection							
Protection Fault Delay				--	100	--	ms
Thermal Shutdown		T_{SD}		125	155	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Charger Unit :

(V_{IN} = 5V, V_{BAT} = 4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
VIN Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} = 0V to 4.5V	3.1	3.3	3.5	V
VIN Under Voltage Lockout Hysteresis	ΔV_{UVLO}	V_{IN} = 4.5V to 0V	--	240	--	mV
VIN Supply Current	I_{SUPPLY}	I_{SYS} = I_{BAT} = 0mA, A7.$\overline{ENCH}$ = 0 (V_{BAT} > V_{REGx})	--	1	2	mA
		I_{SYS} = I_{BAT} = 0mA, A7.$\overline{ENCH}$ = 1 (V_{BAT} > V_{REGx})	--	0.8	1.5	
VIN Suspend Current	I_{USUS}	V_{IN} = 5V, A7.USUS = 1	--	195	300	μA
VIN – BAT VOS Rising	V_{OS_H}		--	200	300	mV
VIN – BAT VOS Falling	V_{OS_L}		10	50	--	mV
Voltage Regulation						
System Regulation Voltage	V_{SYS}	I_{SYS} = 800mA, V_{IN} = 5.5V	4.9	5	5.1	V
Battery Regulation Voltage	V_{REG1}	0 to 85°C, Loading = 20mA, When A9.VSETH = 1 and A9.VSETC = 1	4.16	4.2	4.23	V
Battery Regulation Voltage	V_{REG2}	0 to 85°C, Loading = 20mA, When A9.VSETH = 0 and A9.VSETC = 0	4.01	4.05	4.08	V
APPM Regulation Voltage	V_{APPM}		4.05	4.15	4.25	V
DPM Regulation Voltage	V_{DPM}		4.25	4.35	4.45	V
VIN to VSYS MOSFET Ron	$R_{DS(ON)}$	I_{VIN} = 1000mA	--	0.2	0.35	Ω
BAT to VSYS MOSFET Ron	$R_{DS(ON)}$	V_{BAT} = 4.2V, I_{SYS} = 1A	--	0.05	0.1	Ω
Re-Charge Threshold	ΔV_{REGCHG}	Battery Regulation - Recharge level	60	100	140	mV
Current Regulation						
Charge Current Setting Range	I_{CHG}		100	--	1200	mA
Charge Current Accuracy1	I_{CHG1}	V_{BAT} = 4V, A8.ISETA [3 : 0] = 4'b0101	570	600	630	mA
Charge Current Accuracy2	I_{CHG2}	V_{BAT} = 3.8V, A8.ISETA [3 : 0] = 4'b0010	285	300	315	mA
VIN Current Limit	I_{LIM_VIN}	A7.ISETL = 1, A7.ISETU = 1 (1.5A Mode)	1.5	1.8	2.1	A
		A7.ISETL = 1, A7.ISETU = 0 (1.0A Mode)	0.85	0.925	1	A
		A7.ISETL = 0, A7.ISETU = 1 (500mA mode)	450	475	500	mA
		A7.ISETL = 0, A7.ISETU = 0 (100mA Mode)	90	95	100	mA
Pre-Charge						
BAT Pre-Charge Threshold	V_{PRECH}	BAT Falling	2.7	2.8	2.9	V
BAT Pre-Charge Threshold Hysteresis	ΔV_{PRECH}		--	200	--	mV
Pre-Charge Current	I_{CHG_PRE}	V_{BAT} = 2V	5	10	15	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charge Termination Detection						
Termination Current Ratio to Fast Charge (Except USB 100 Mode)	I_{TERM}	A7.ISETL = 0, A7.ISETU = 1 or A7.ISETL = 1, A7.ISETU = X	5	10	15	%
Termination Current Ratio to Fast Charge (USB100 Mode)	I_{TERM2}	A7.ISETL = 0, A7.ISETU = 0	--	3.3	--	%
Login Input/Output						
$\overline{CHG}$ Pull Down Voltage	$V_{\overline{CHG}}$	$I_{\overline{CHG}}$ = 5mA	--	200	--	mV
$\overline{INT}$ Pull Down Voltage	$V_{\overline{INT}}$	$I_{\overline{INT}}$ = 5mA	--	200	--	mV
Protection						
Thermal Regulation Point	T_{REG}		--	125	--	°C
Thermal Shutdown Temperature	T_{SD}		--	155	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Over Voltage Protection	V_{OVP}	V_{IN} Rising	6.25	6.5	6.75	V
Over Voltage Protection Hysteresis	ΔV_{OVP}	V_{IN} = 7V to 5V, VOVP – ΔVOVP	--	100	--	mV
Output Short Circuit Detection Threshold	V_{SHORT}	VBAT – VSYS	--	300	--	mV
Battery Installation Detection Threshold at TS		EN = H (PMU enabled), report at A10. NoBAT bit	--	90	--	% of VP
Time						
Input Over Voltage Blanking Time	t_{OVP}		--	50	--	µs
Pre-Charge to Fast-Charge Deglitch Time	t_{PF}		--	25	--	ms
Fast-Charge to Pre-Charge Deglitch Time	t_{FP}		--	25	--	ms
Termination Deglitch Time	t_{TERMI}		--	25	--	ms
Recharge Deglitch Time	t_{RECHG}		--	100	--	ms
Input Power Loss to SYS LDO Turn-Off Delay Time	t_{NO_IN}		--	25	--	ms
Pack Temperature Fault Detection Deglitch Time	t_{TS}		--	25	--	ms
Short Circuit Deglitch Time	t_{SHORT}		--	250	--	µs
Short Circuit Recovery Time	$t_{SHORT-R}$		--	64	--	ms
Other						
VP Regulation Voltage	V_{VP}	V_{SYS} = 4.2V	3.234	3.3	3.366	V
VP Load Regulation	V_{VP}	VP source out 2mA	--	--	–0.1	V
VP Under Voltage Lockout Threshold		Falling Threshold	--	0.8	--	V
TS Battery Detect Threshold	V_{TS}		2.75	2.85	2.95	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NTC Temperature Sense						
Low Temperature Trip Point (0°C)	V_{TOO_COLD}	NTC = 100kΩ	73	74	75	% of VP
	V_{TOO_COLD}	NTC = 10kΩ	59	60	61	
Low Temperature Trip Point (10°C) for JEITA	V_{COLD}	NTC = 100kΩ	63	64	65	% of VP
	V_{COLD}	NTC = 10kΩ	51	52	53	
High Temperature Trip Point (45°C) for JEITA	V_{HOT}	NTC = 100kΩ	34	35	36	% of VP
	V_{HOT}	NTC = 10kΩ	31	32	33	
High Temperature Trip Point (60°C)	V_{TOO_HOT}	NTC = 100kΩ, A8.TSHT [1 : 0] = 2'b00	27	28	29	% of VP
	V_{TOO_HOT}	NTC = 10kΩ, A8.TSHT [1 : 0] = 2'b00	27	28	29	
High Temperature Trip Point Hysteresis for JEITA			--	1	--	% of VP
Charger Detection						
VDP_SRC Voltage	VDP_SRC	With IDAT_SRC = 0 to 200μA	0.5	--	0.7	V
VDAT_REF Voltage	VDAT_REF		0.25	--	0.4	V
VLGC Voltage	VLGC		0.8	--	2	V
IDP_SRC Current	IDP_SRC		6.6	--	11	μA
D+ and D– Sink Current	ICD+_SINK ICD–_SINK		50	--	150	μA
D– Pull down Resistor	RD-_DWN		14.25	--	24.8	kΩ
Data Contact Detect Debounce	TDCD_DBNC		10	15	20	ms
DCD Time OUT	TDCD_TO		150	--	450	ms
VDAT_SRC ON Time	TDP_SRC_ON		50	--	100	ms

(V_{SYS} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
I²C							
SDA, SCLK Input Voltage	High-Level			1.4	--	--	V
	Low-Level			--	--	0.6	
SCLK Clock Rate		f_{SCL}		--	--	400	kHz
Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		$t_{HD,STA}$		0.6	--	--	µs
LOW Period of the SCL Clock		t_{LOW}		1.3	--	--	µs
HIGH Period of the SCL Clock		t_{HIGH}		0.6	--	--	µs
Set-Up Time for a Repeated START Condition		$t_{SU,STA}$		0.6	--	--	µs
Data Hold Time		$t_{HD,DAT}$		0	--	0.9	µs
Data Set-Up Time		$t_{SU,DAT}$		100	--	--	ns
Set-Up Time for STOP Condition		$t_{SU,STO}$		0.6	--	--	µs
Bus Free Time between a STOP and START condition		t_{BUF}		1.3	--	--	µs
Rise time of both SDA and SCL signals		t_R		20	--	300	ns
Fall Time of Both SDA and SCL Signals		t_F		20	--	300	ns
SDA and SCL Output Low Sink Current		I_{OL}	SDA or SCL voltage = 0.4V	2	--	--	mA

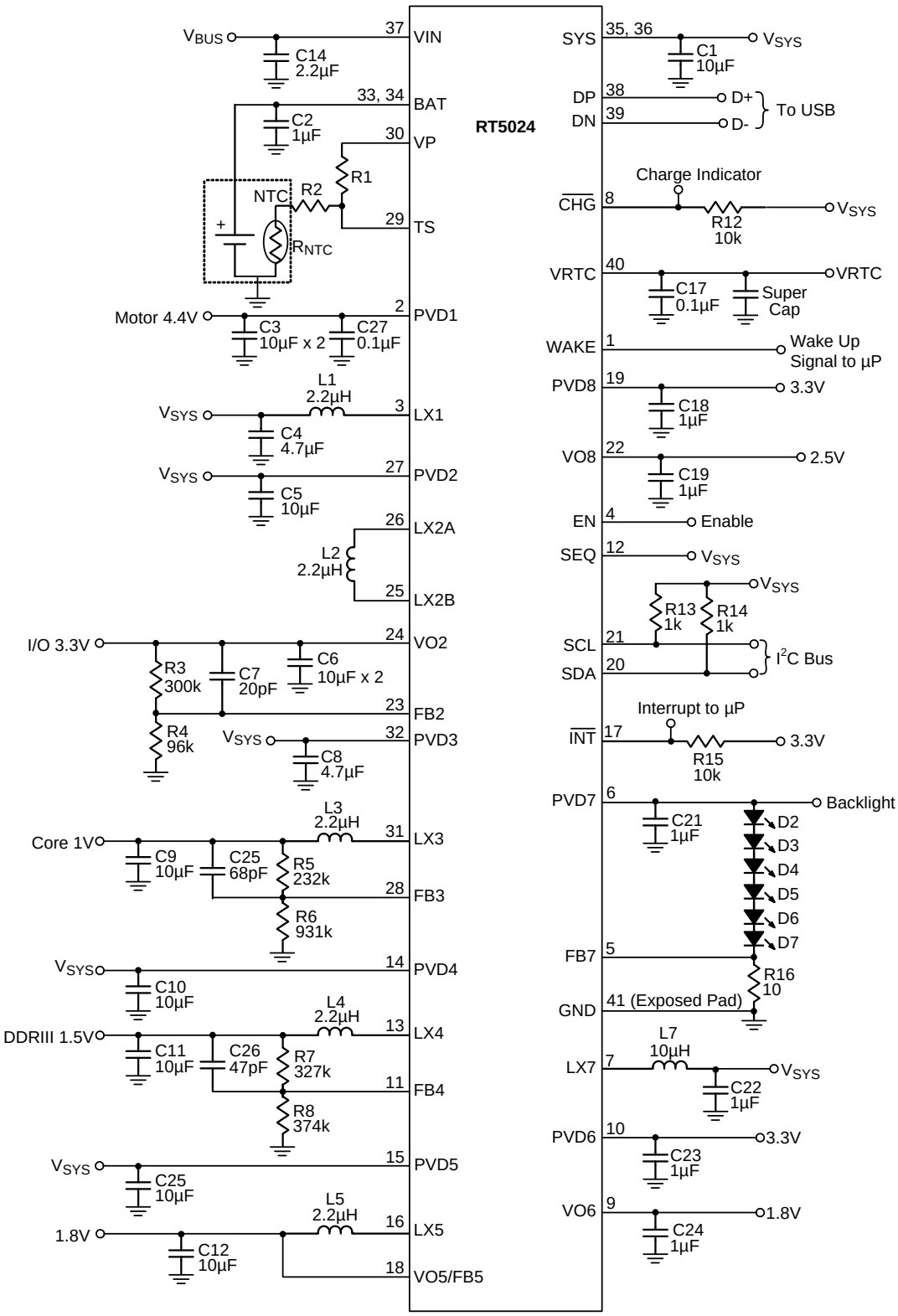
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

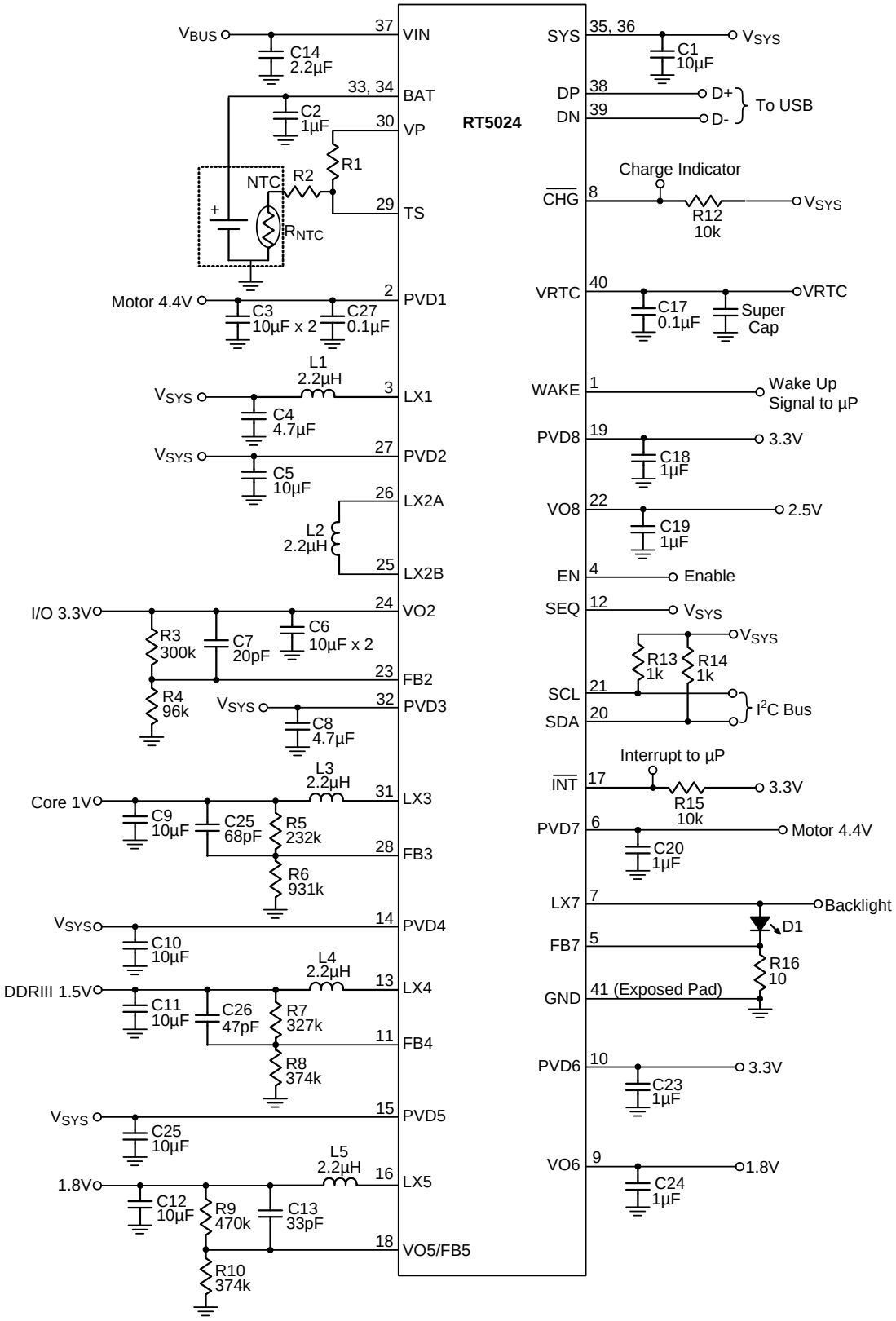
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



Note : To make CH1 stable, C27 must be close to PVD1.

Figure 1. Typical Application Circuit for DSC with 6-LED Backlight



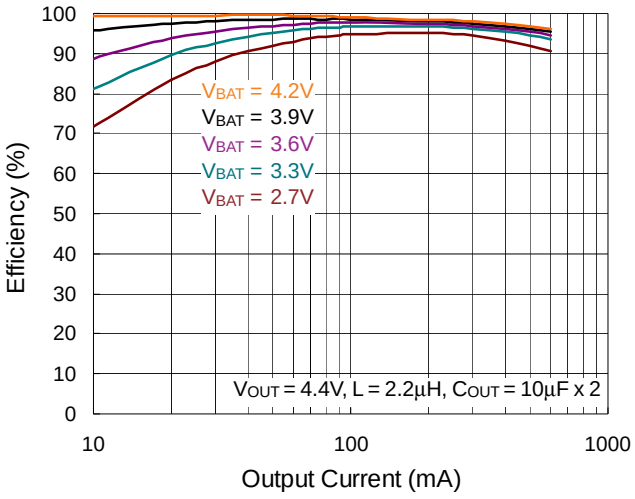
Note : To make CH1 stable, C27 must be close to PVD1.

Figure 2. Typical Application Circuit for DSC with One LED Backlight

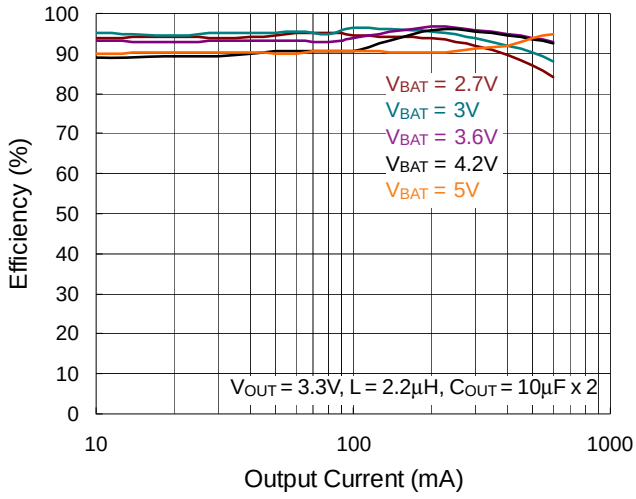
Typical Operating Characteristics

V_{IN} = 5V, unless otherwise specified.

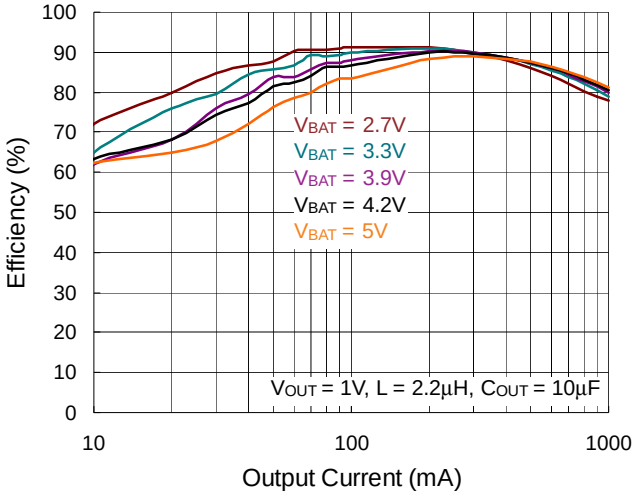
CH1 Step-Up Efficiency vs. Output Current



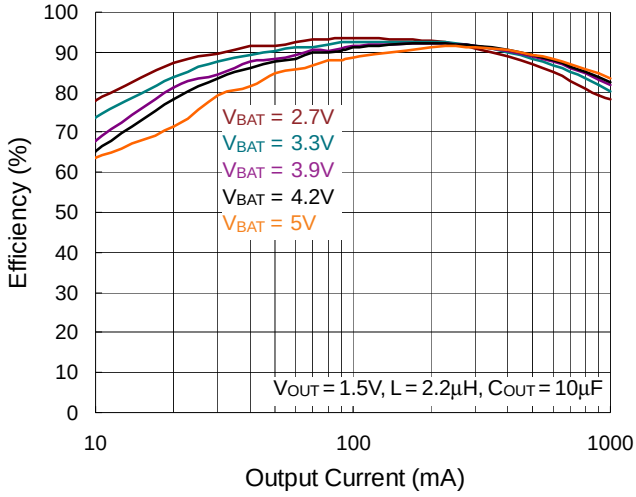
CH2 Step-Up/Down Efficiency vs. Output Current



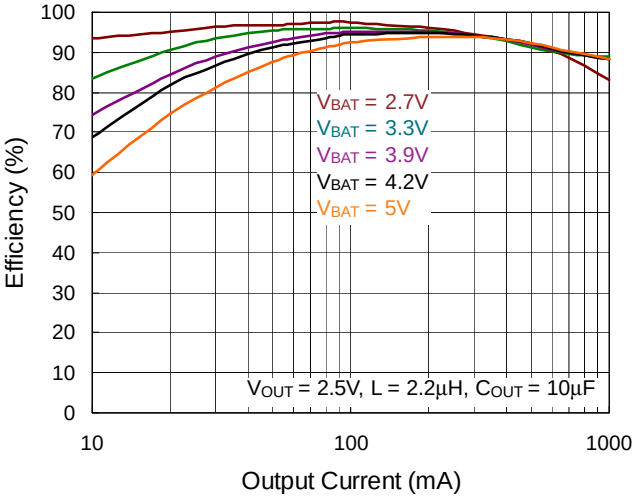
CH3 Step-Down Efficiency vs. Output Current



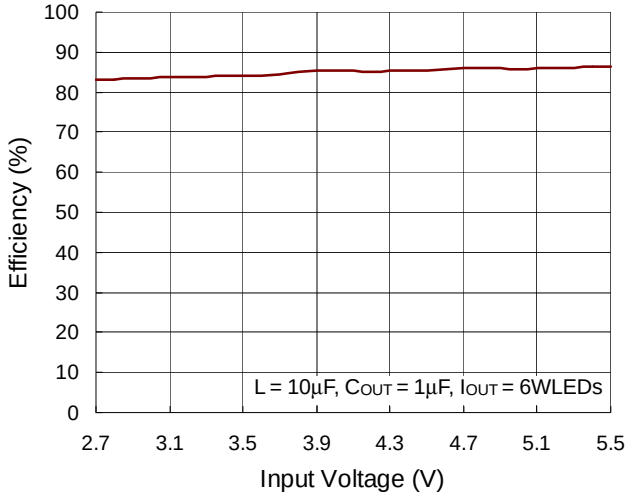
CH4 Step-Down Efficiency vs. Output Current



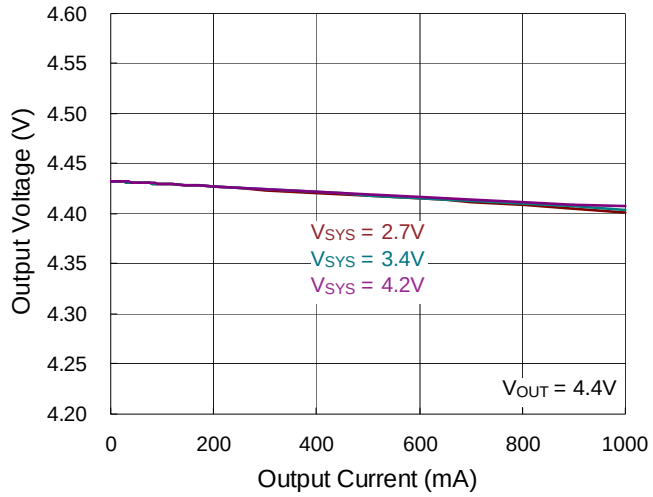
CH5 Step-Down Efficiency vs. Output Current



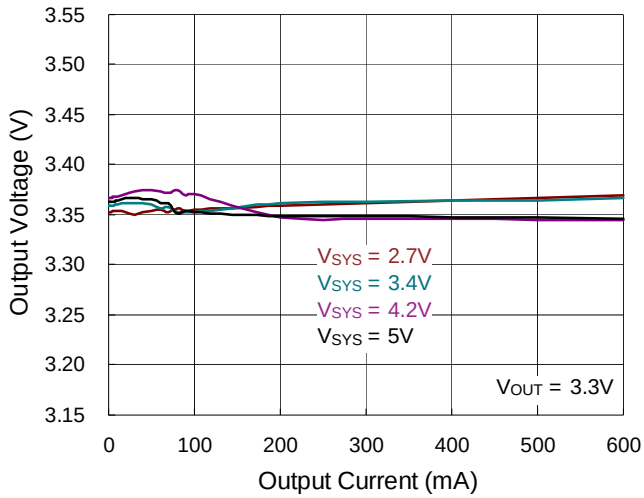
CH7 Efficiency vs. Input Voltage



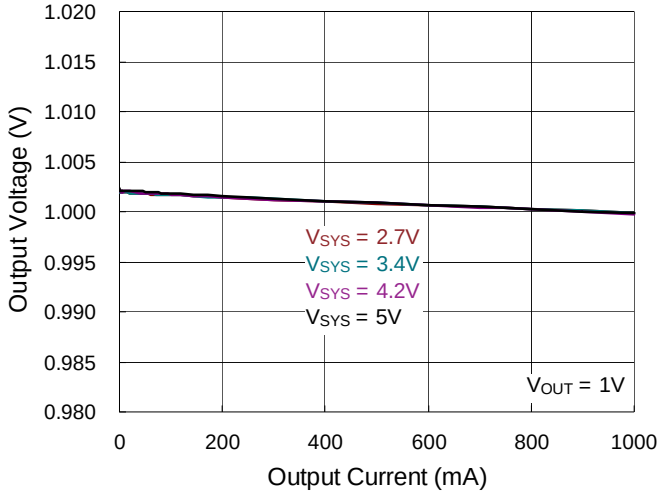
CH1 Step-Up Output Voltage vs. Output Current



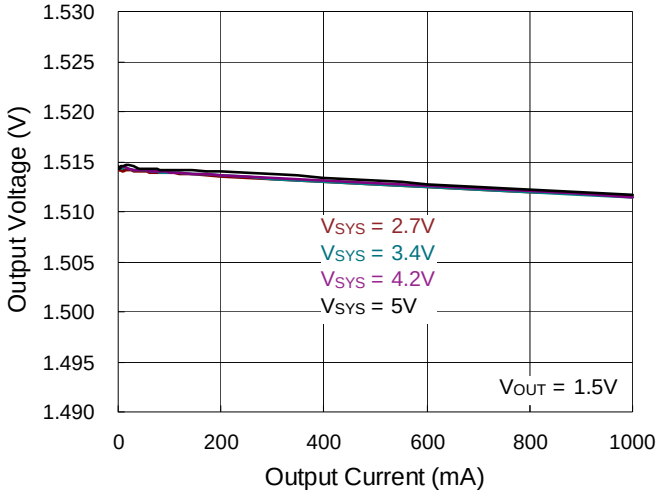
CH2 Step-Up/Down Output Voltage vs. Output Current



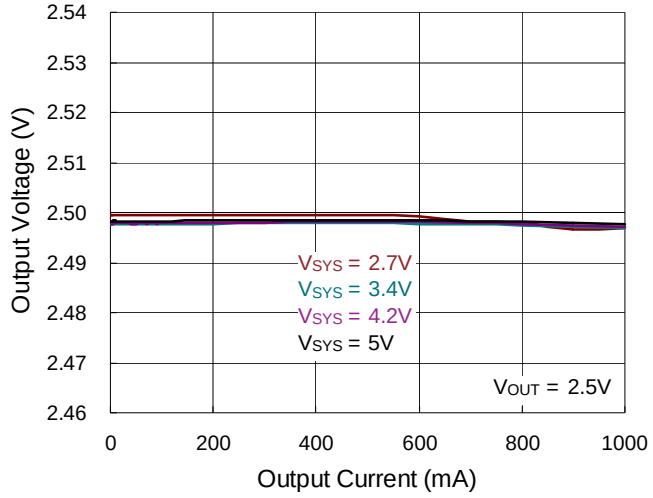
CH3 Step-Down Output Voltage vs. Output Current



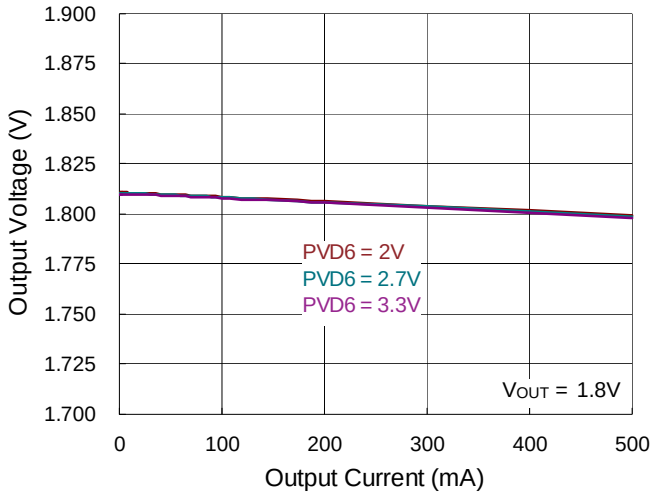
CH4 Step-Down Output Voltage vs. Output Current



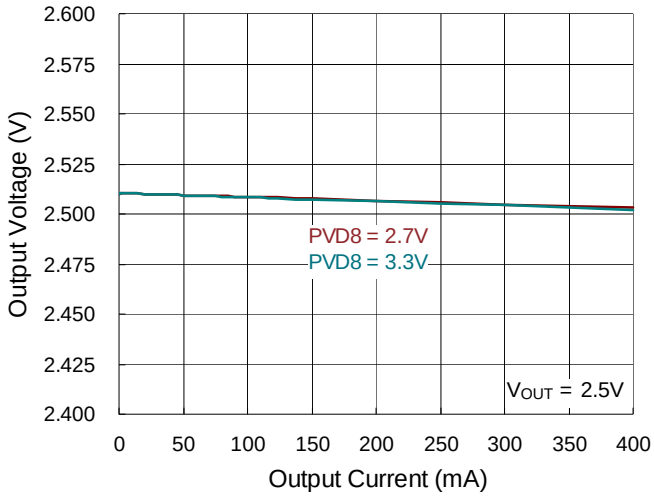
CH5 Step-Down Output Voltage vs. Output Current



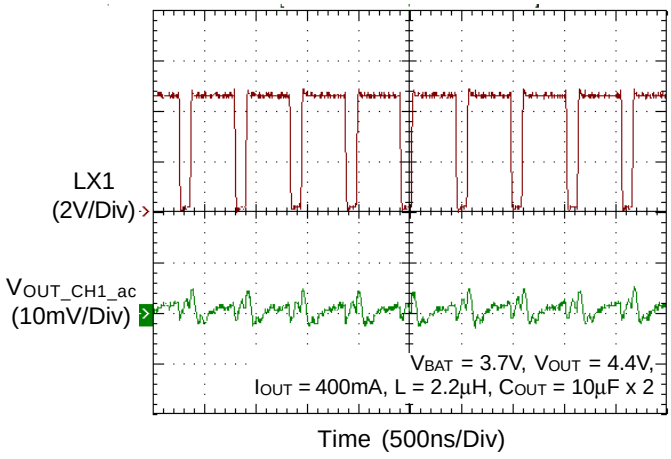
CH6 LDO Output Voltage vs. Output Current



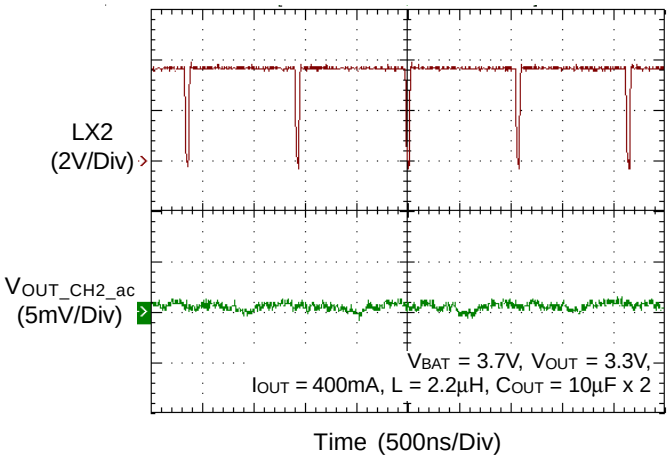
CH8 LDO Output Voltage vs. Output Current



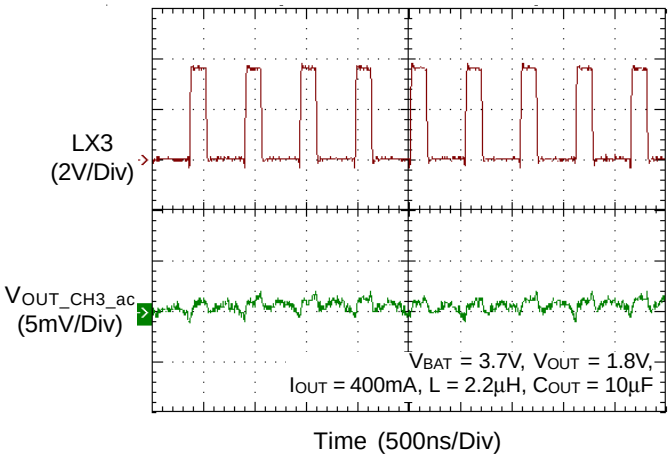
CH1 Output Voltage Ripple



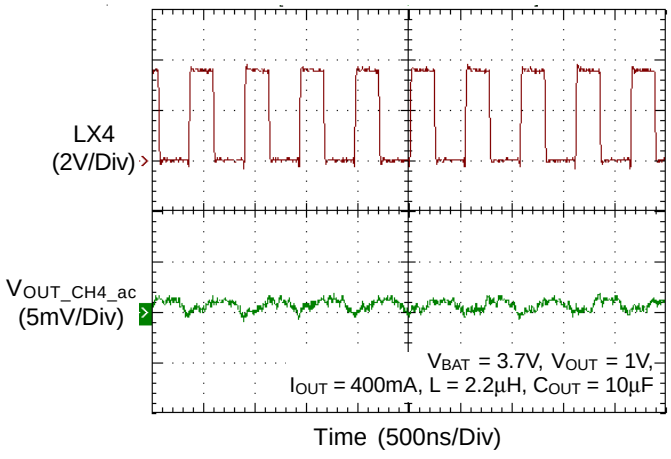
CH2 Output Voltage Ripple



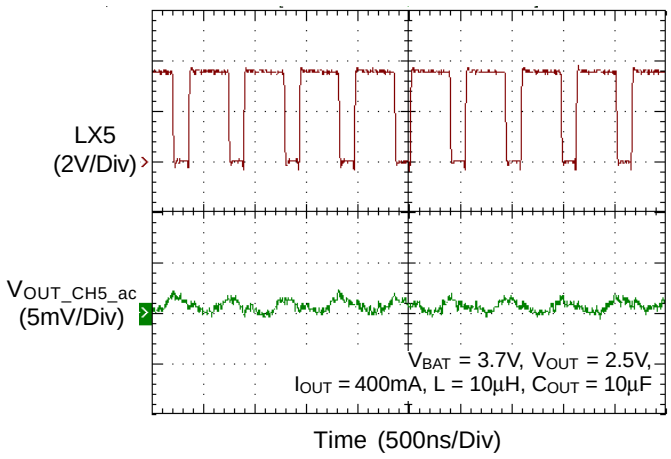
CH3 Output Voltage Ripple



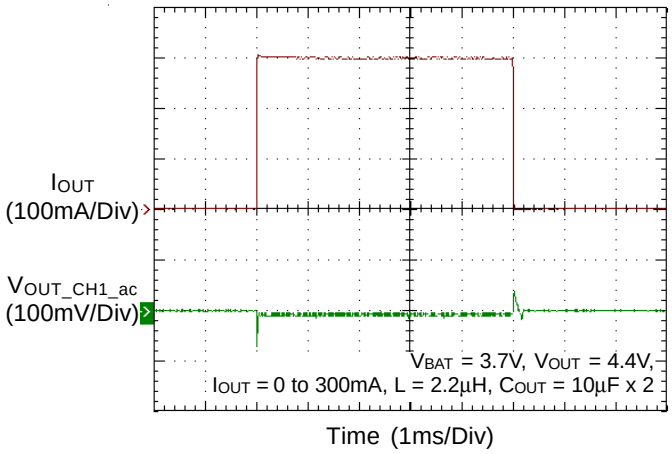
CH4 Output Voltage Ripple



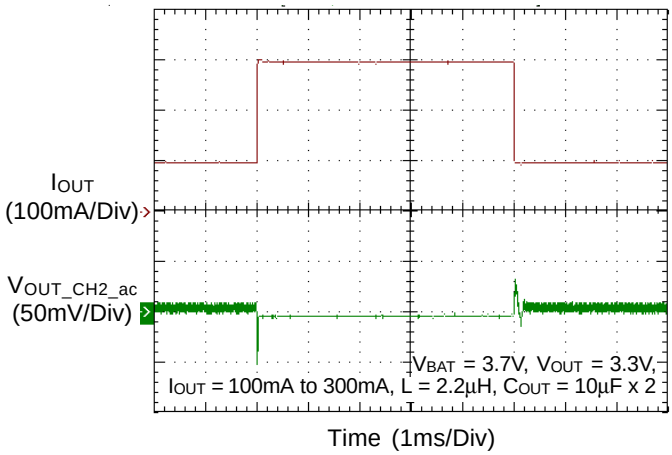
CH5 Output Voltage Ripple



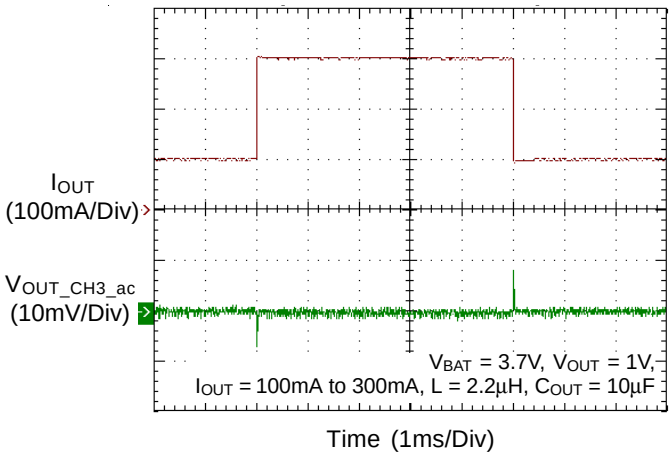
CH1 Load Transient Response



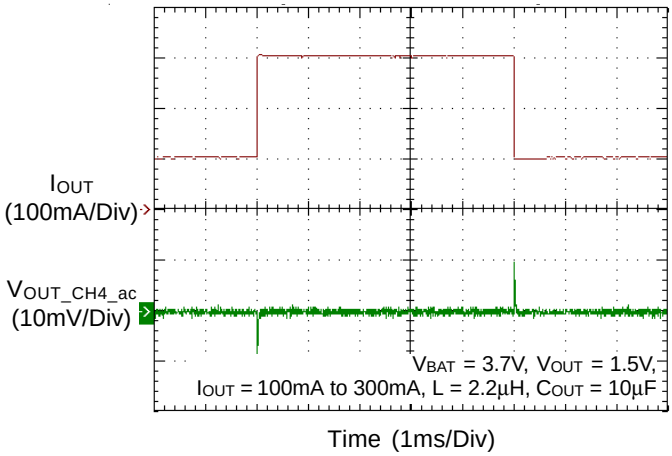
CH2 Load Transient Response



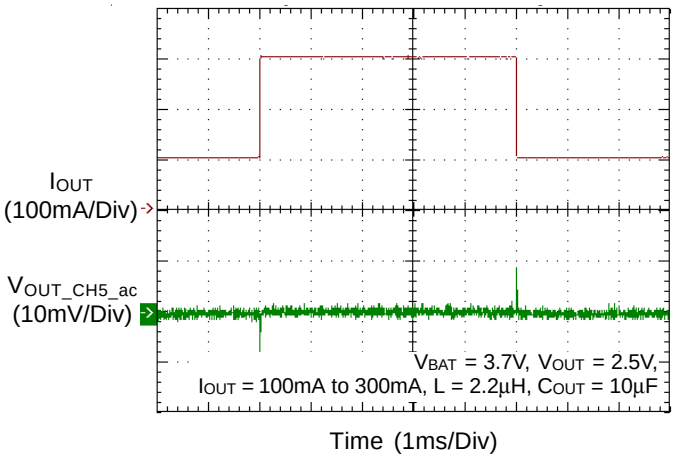
CH3 Load Transient Response



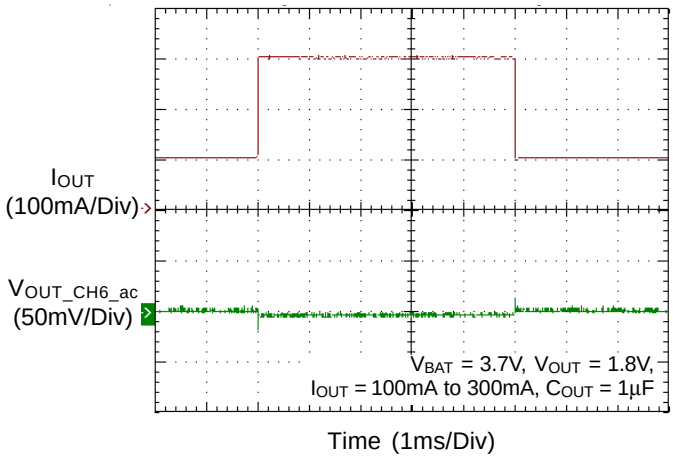
CH4 Load Transient Response



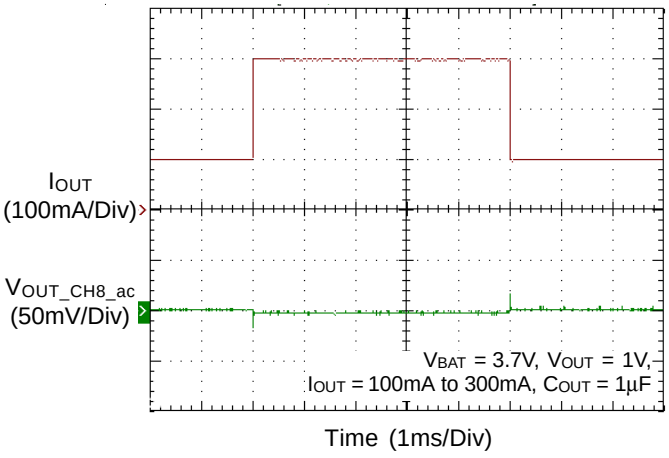
CH5 Load Transient Response



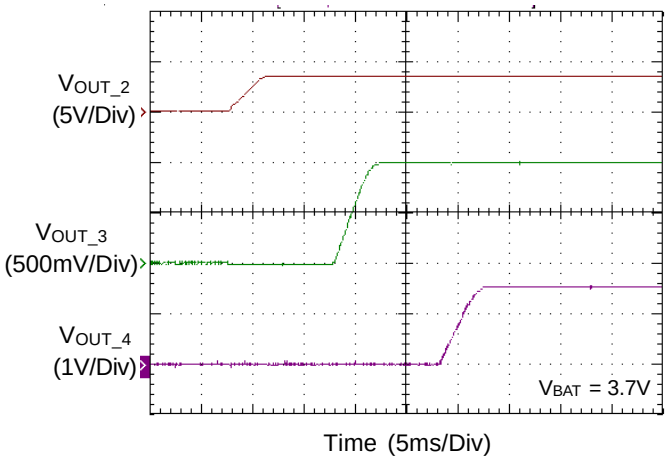
CH6 Load Transient Response



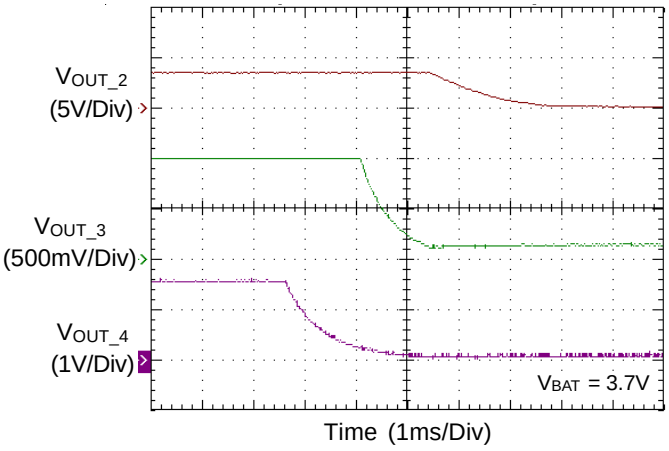
CH8 Load Transient Response



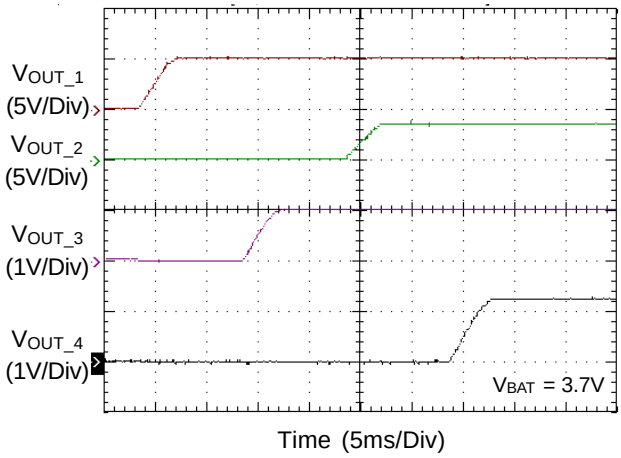
Power On Sequence 0



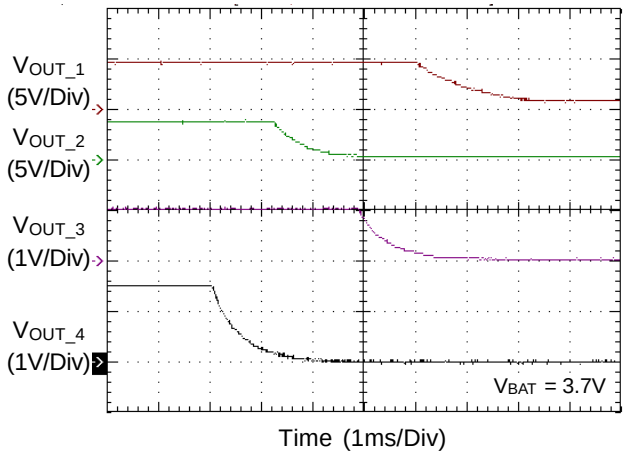
Power Off Sequence 0



Power On Sequence 1



Power Off Sequence 1



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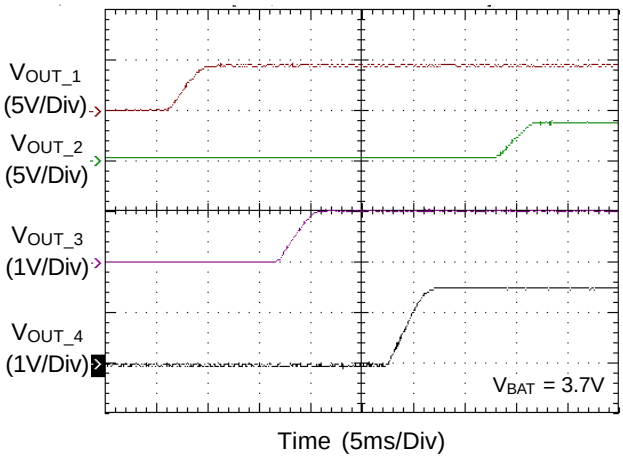

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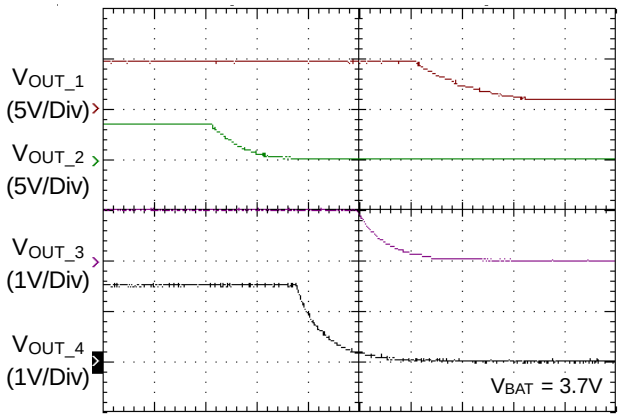

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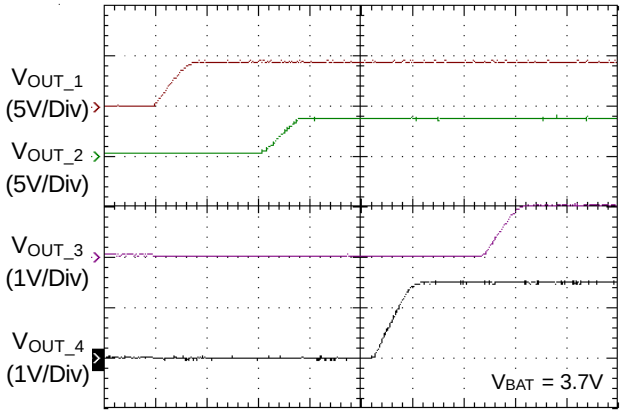
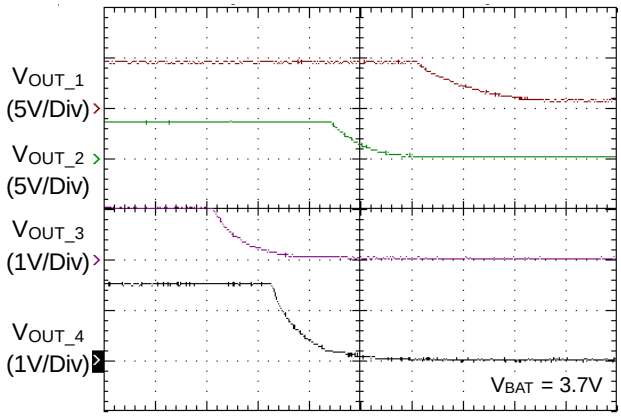


Power Off Sequence 3



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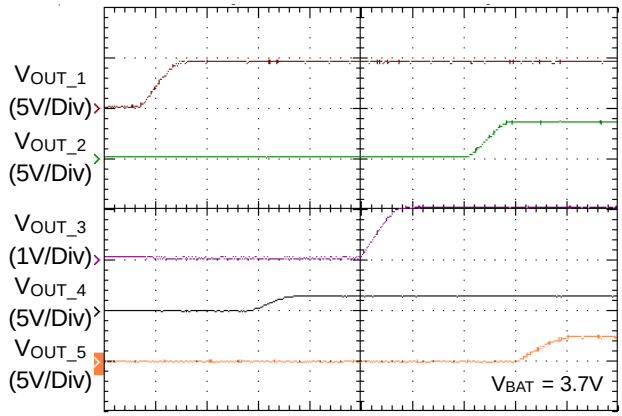
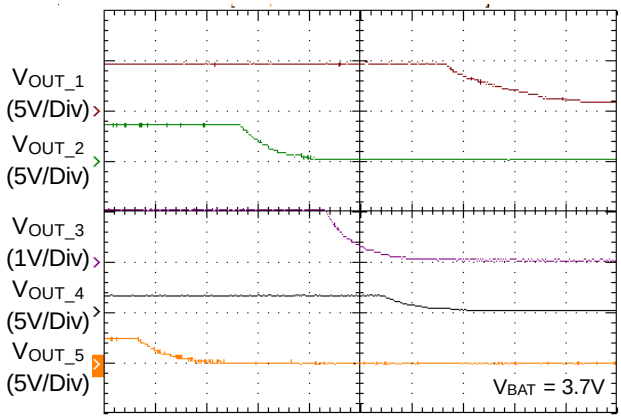


Power Off Sequence 4



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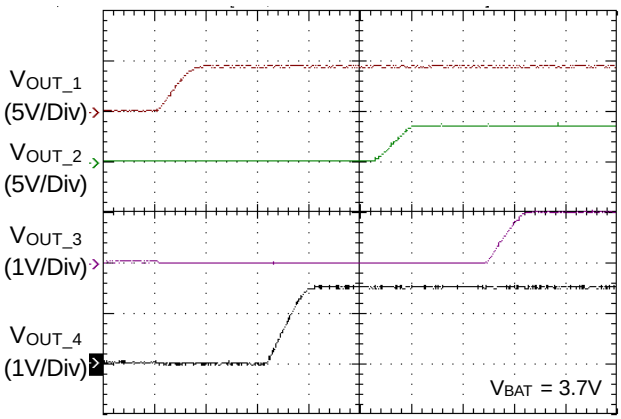
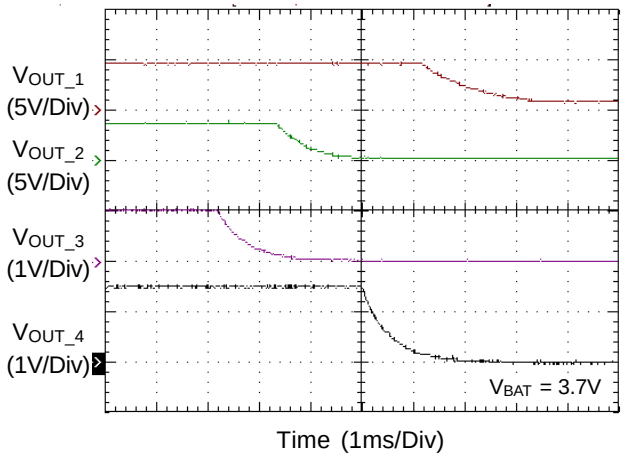
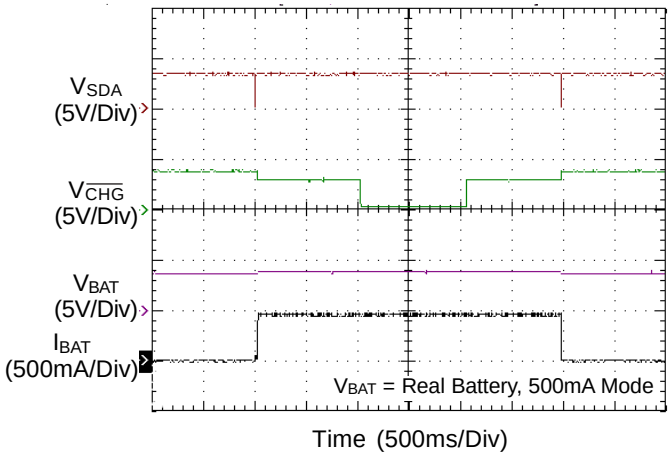


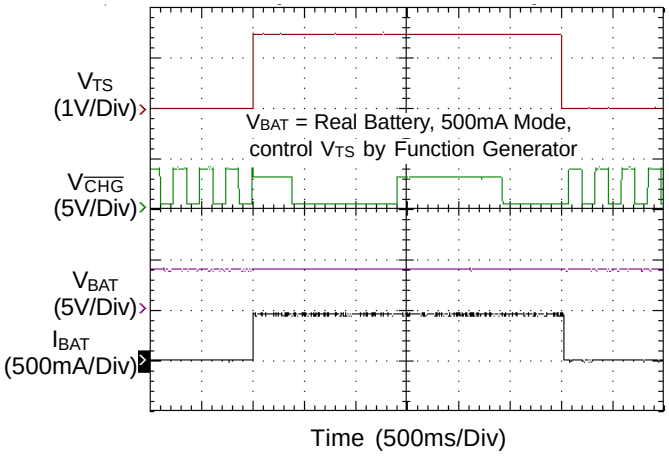
Power Off Sequence 5



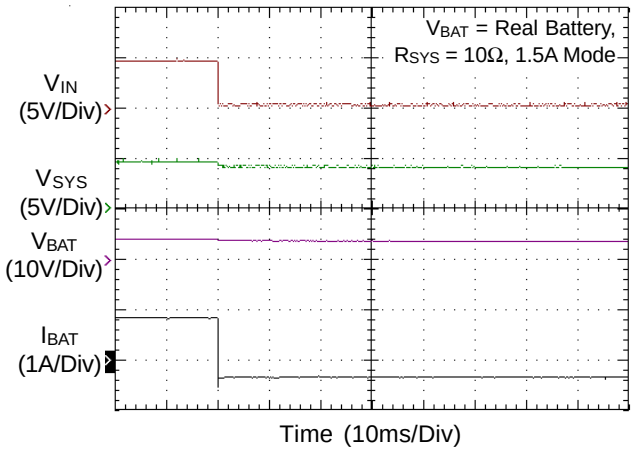
Charge On/Off Control by I²C



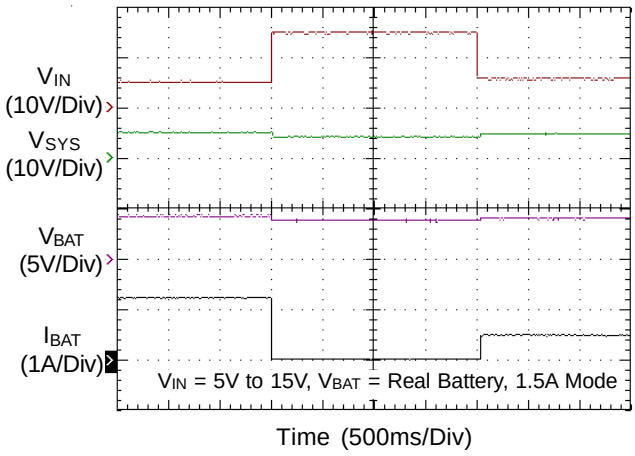
V_{TS} On/Off



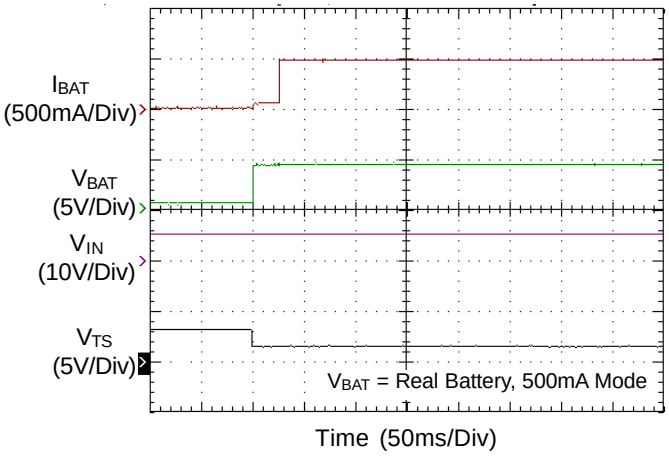
V_{IN} Removal



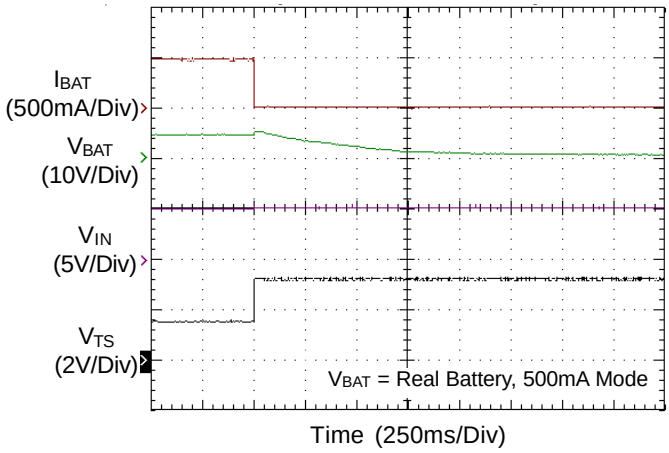
V_{IN} Over Voltage Protection



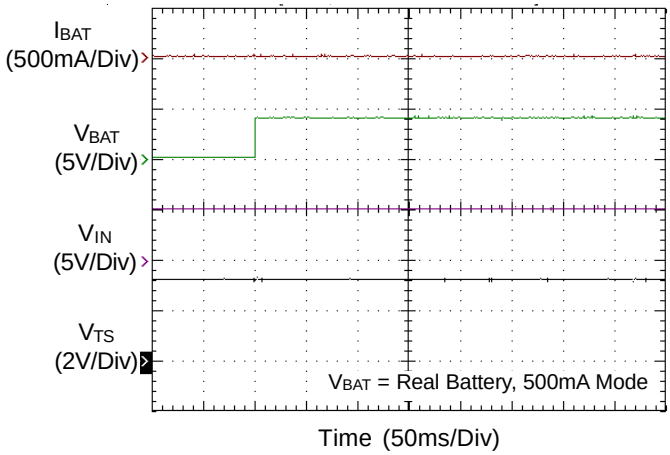
Battery with NTC Resistor Plug-In



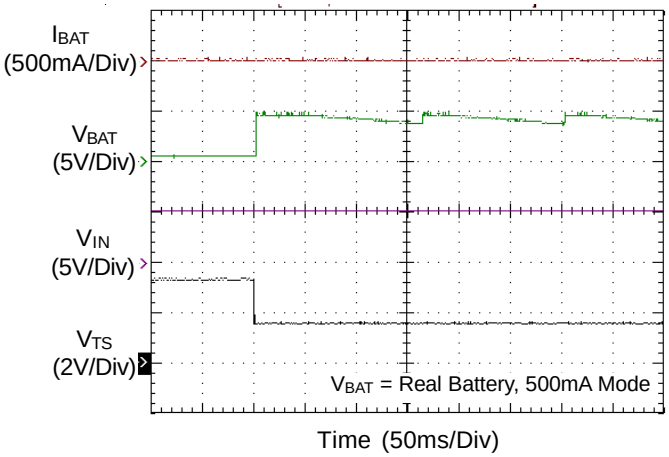
Battery with NTC Resistor Plug-Out



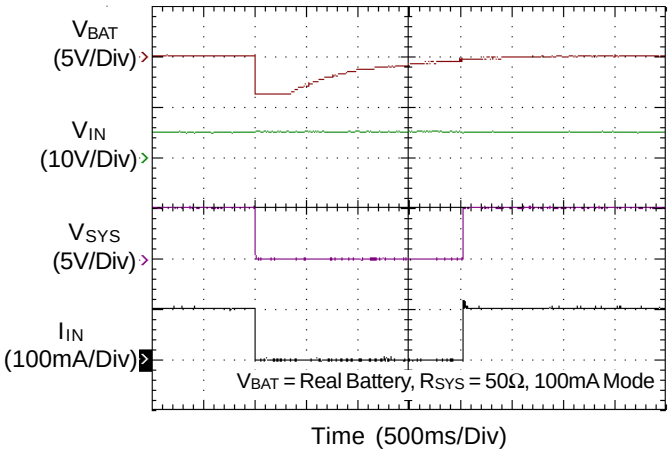
With Battery without NTC Resistor



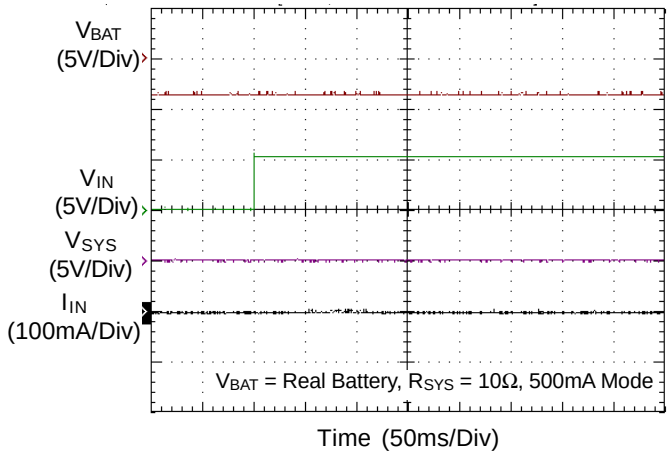
With NTC Resistor without Battery



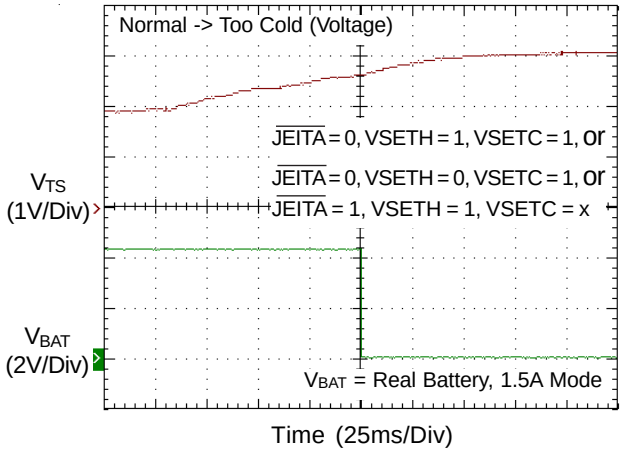
V_{IN} Exist then Negative Battery and Plug-out



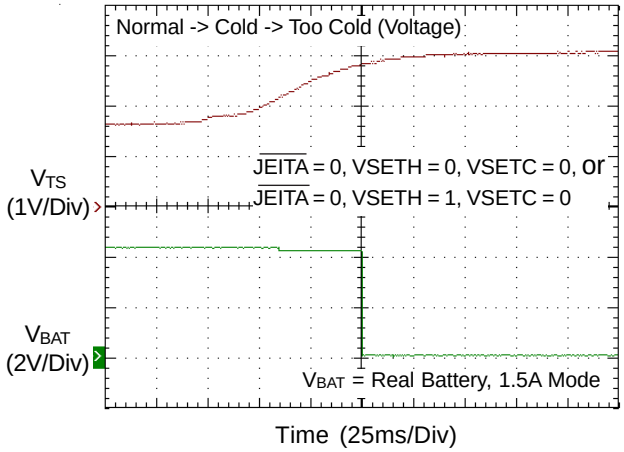
Negative Battery then V_{IN} Plug-In



The Temperature of Battery Status



The Temperature of Battery Status



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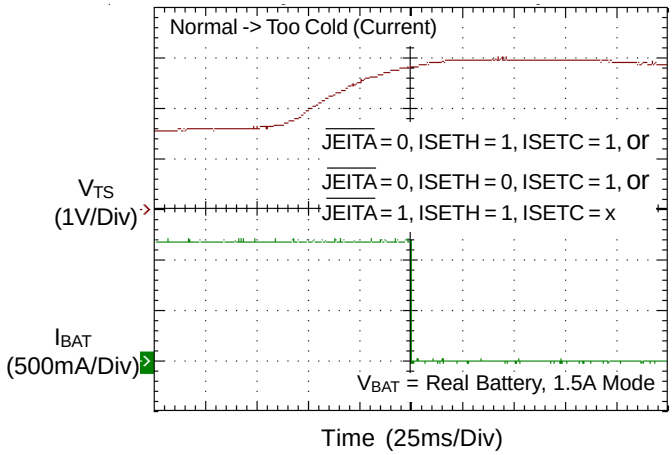
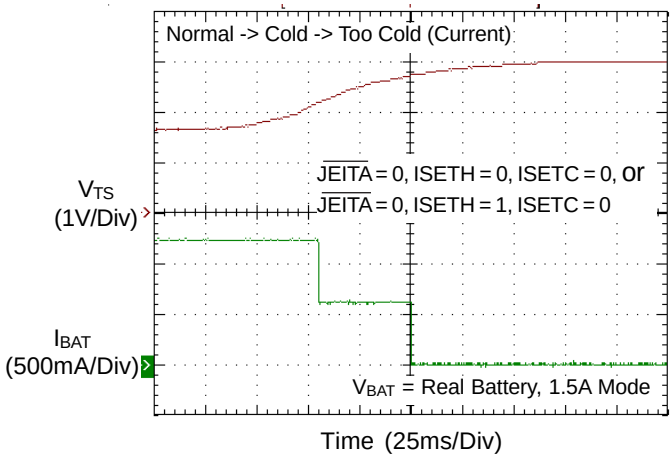


The Temperature of Battery Status



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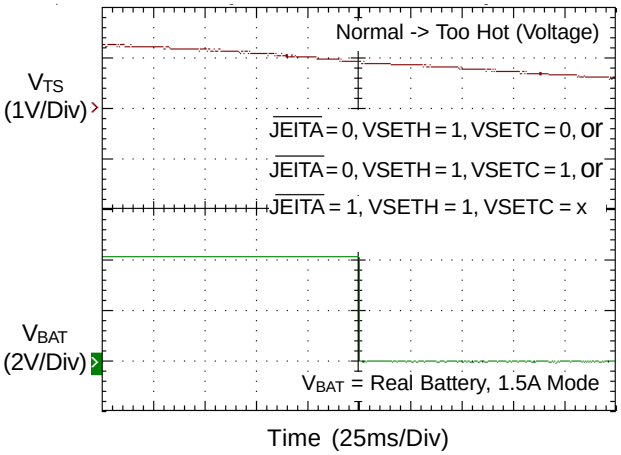

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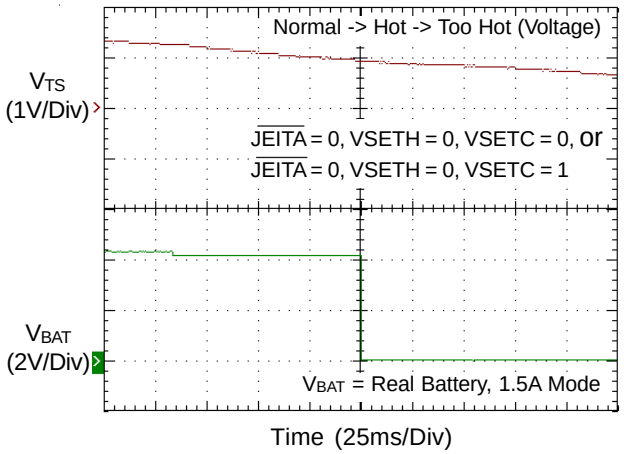
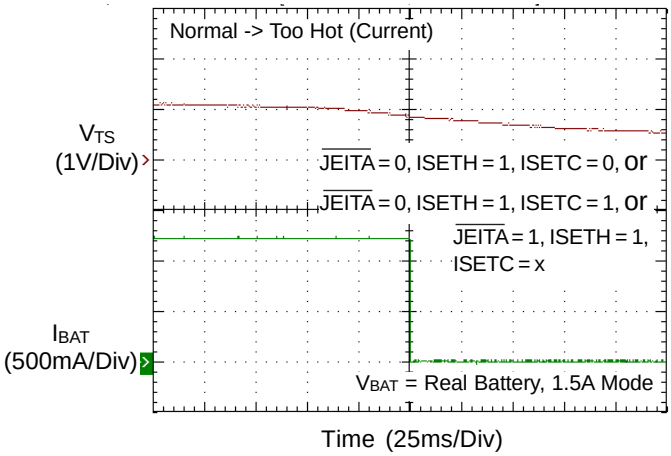
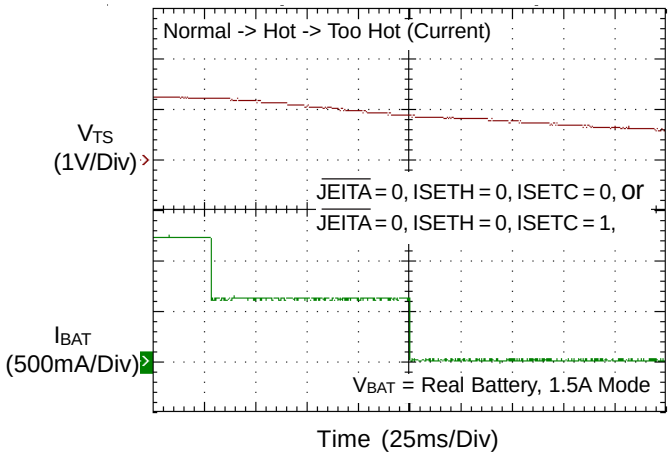


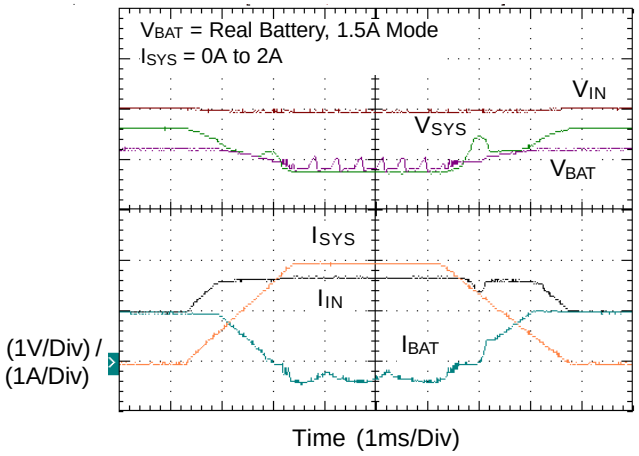
The Temperature of Battery Status



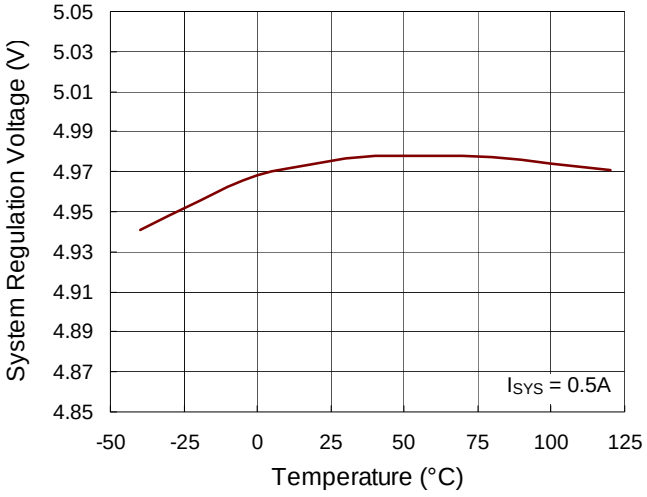
The Temperature of Battery Status



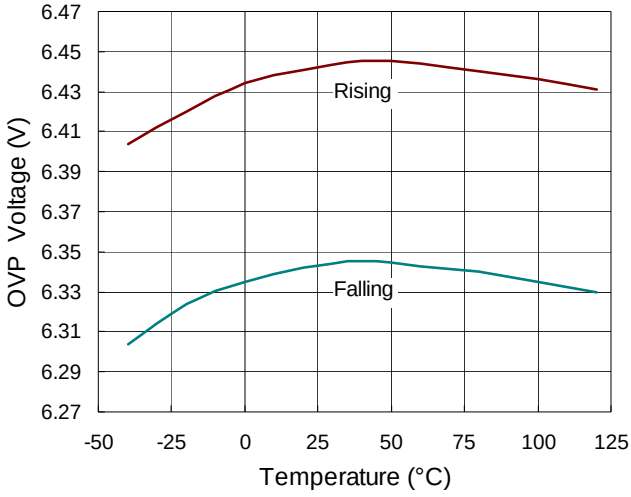
APPM



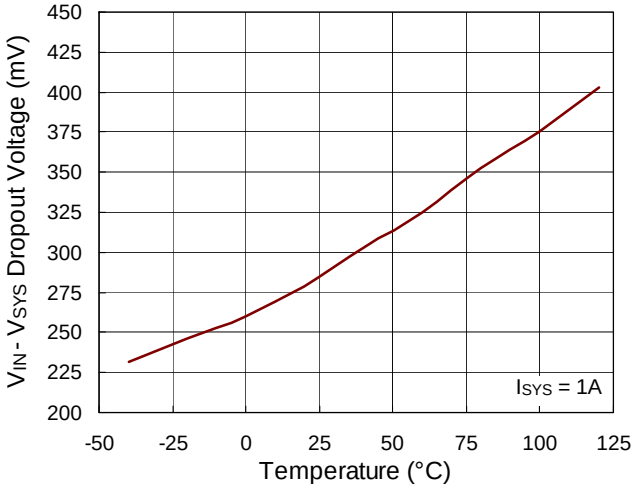
System Regulation Voltage vs. Temperature



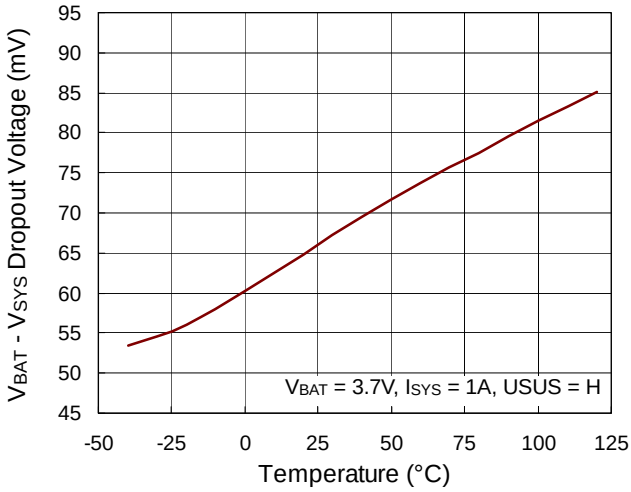
OVP Threshold Voltage vs. Temperature

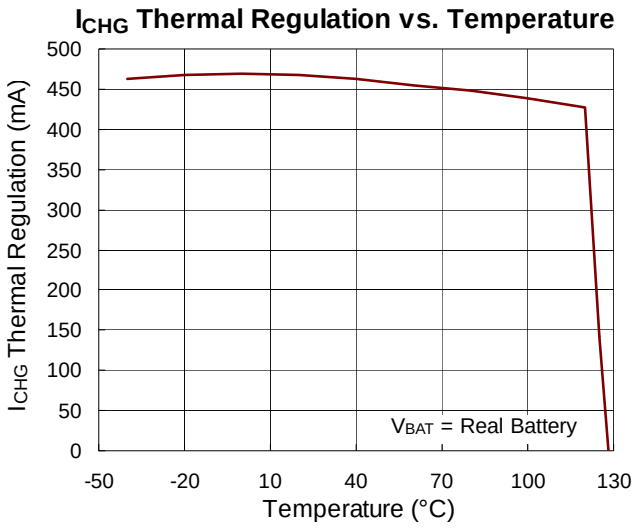


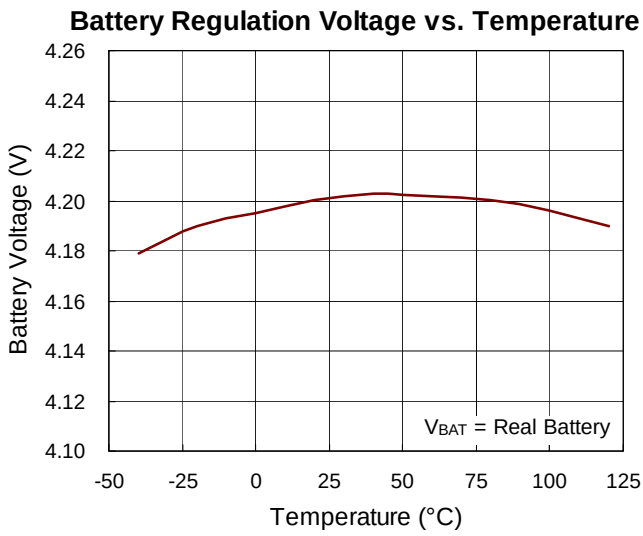
V_{IN} - V_{SYS} Dropout Voltage vs. Temperature

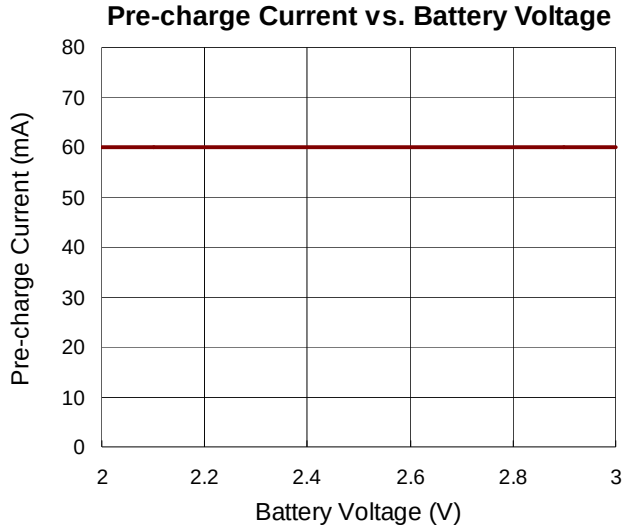


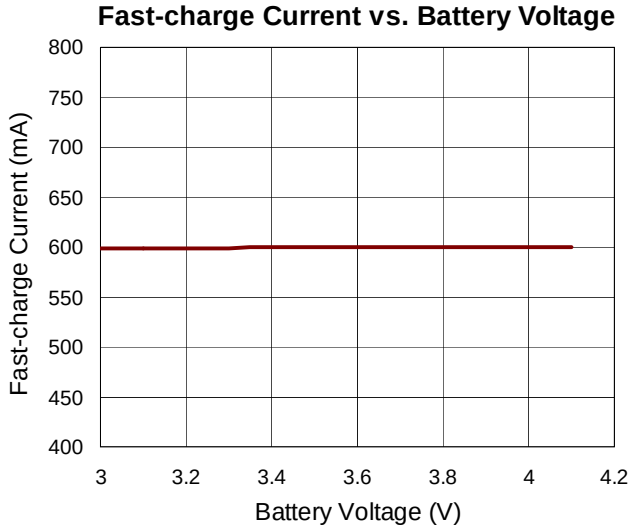
V_{BAT} - V_{SYS} Dropout Voltage vs. Temperature











Application Information

Power Converter Unit

The RT5024 is an integrated power solution for digital still cameras and other small handheld devices. It includes six DC-DC converters, a WLED driver, two low output LDO, a RTC LDO and a fully integrated single-cell Li-ion battery charger that is ideal for portable applications.

CH1 : Synchronous Step-Up DC-DC Converter

The synchronous step-up DC-DC converter can be operated in either PFM or Sync-PWM mode by setting I^2C. It includes internal power MOSFETs, compensation network and feedback resistors. The P-MOSFET can be controlled to disconnect output loading. It is suitable for providing power to the motor. The output voltage of CH1 can be adjusted by the I^2C interface in the range of 3.6V to 5.5V.

	CH1 regulation voltage can be selected by I^2C interface. The default voltage is 4.4V.							
VOUT1 [3:0]	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
	0000	3.6V	0001	3.7V	0010	3.8V	0011	3.9V
	0100	4V	0101	4.4V	0110	4.6V	0111	4.7V
	1000	4.8V	1001	4.9V	1010	5V	1011	5.1V
	1100	5.2V	1101	5.3V	1110	5.4V	1111	5.5V

CH2 : Synchronous Step-Up/Down (Buck-Boost) DC-DC Converter

The synchronous step-up/down (Buck-Boost) DC-DC converter can be operated in either PFM or Sync-PWM mode by setting I^2C. It includes internal power MOSFETs, compensation network and feedback resistors. This channel supplies the power for I/O. The FB voltage of CH2 can be adjusted by the I^2C interface in the range of 0.72V to 0.86V.

	FB2 regulation voltage can be selected by I^2C interface. The default voltage is 0.8V.				
FB2 [2:0]	**Code**	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

CH3 to CH4 : Step-Down Synchronous DC/ DC Converter

The step-down synchronous DC/ DC converters include internal power MOSFETs and compensation network. It support PFM or Sync-PWM mode by setting I^2C. These channels supply the power for core and DRAM. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The FB voltage of CH3 and CH4 can be adjusted by the I^2C interface in the range of 0.72V to 0.86V.

	FB3 regulation voltage can be selected by I^2C interface. The default voltage is 0.8V.				
	Code	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
FB3 [2:0]	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

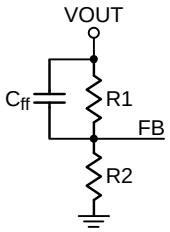
	FB4 regulation voltage can be selected by I^2C interface. The default voltage is 0.8V.				
	Code	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
FB4 [2:0]	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

If CH3/CH4 input voltage (PVD3/PVD4) is higher than 4.2V and the output voltage is lower than 1.5V, a feed forward capacitor can be added improve the transient response.

The capacitance can be estimated by the following equation.

$$C_{ff} = \frac{15.5 \times 10^{-6}}{R1}$$

For example, when R1 is 470kΩ, the available feed-forward capacitor is 33pF.



CH5 : Step-Down Synchronous DC/ DC Converter

The step-down synchronous DC/ DC converter includes internal power MOSFETs and compensation network. It supports PFM or Sync-PWM mode by setting I²C. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The output voltage can be selected as the following list or set by external feedback network.

VOUT5 [3:0]	CH5 regulation voltage can be selected by I²C interface. The default voltage is REF.							
	Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
	0000	REF	0001	1.1V	0010	1.2V	0011	1.3V
	0100	1.4V	0101	1.5V	0110	1.6V	0111	1.7V
	1000	1.8V	1001	2V	1010	2.2V	1011	2.3V
	1100	2.5V	1101	2.6V	1110	2.7V	1111	2.8V
	Note : VOUT5 [3:0] = 0000 (REF) means using external feedback network and FB5 regulation target is 0.8V ± 1.5%							

CH6 : Low Voltage LDO

CH6 is a low voltage LDO and its output voltage is controlled by I²C interface. This supplies the multiple purpose power. The output voltage of CH6 can be adjusted by the I²C interface in the range of 1.2V to 3.7V.

VOUT6 [3:0]	CH6 regulation voltage can be selected by I²C interface. The default voltage is 1.8V.							
	Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
	0000	1.2V	0001	1.3V	0010	1.5V	0011	1.6V
	0100	1.8V	0101	2V	0110	2.2V	0111	2.4V
	1000	2.7V	1001	3V	1010	3.1V	1011	3.2V
	1100	3.3V	1101	3.4V	1110	3.6V	1111	3.7V

CH7 : Current Source/Step-Up WLED Driver

The WLED drivers operating in either current source mode or synchronous step-up mode include internal power MOSFET and compensation network. The operation mode is determined by setting I²C. The P-MOSFET in step-up mode can be controlled to disconnect the output loading.

When CH7 works in current source mode, it likes a LDO and regulates the current by FB7 voltage. The LED current is defined by the FB7 voltage as well as the external resistor between FB7 and GND. The FB7 regulation voltage can be set in 31 steps from 8mV to 250mV. If CH7 works in synchronous step-up mode, it can support an output voltage up to 15V or 21V controlled by I²C interface. The LED current is also set via an external resistor and FB7 regulation voltage.

The WLED current can be set by the following equation :

ILED (mA) = [250mV / R (Ω)] x EN7_DIM7 [4:0] / 31

Where R is the current sense resistor from FB7 to GND and EN7_DIM7 [4:0] / 31 ratio refers to the I²C control register file.

CH8 : Low Voltage LDO

CH8 is a low voltage LDO and its output voltage is controlled by I^2C interface. It supplies for multiple purpose power. The output voltage of CH8 can be adjusted by the I^2C interface in the range of 1V to 2.8V.

	CH8 regulation voltage can be selected by I^2C interface. The default voltage is 2.5V.							
VOUT8 [3:0]	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
	0000	1V	0001	1.1V	0010	1.2V	0011	1.3V
	0100	1.4V	0101	1.5V	0110	1.6V	0111	1.7V
	1000	1.8V	1001	2V	1010	2.2V	1011	2.3V
	1100	2.5V	1101	2.6V	1110	2.7V	1111	2.8V

RTC_LDO : Accuracy 3.25V LDO Output.

The RT5024 provides a 3.25V output LDO for real-time clock. The LDO features low quiescent current (3μA), reverse leakage prevention from output node and high output voltage accuracy. This LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 0.1μF capacitor to the RTCPWR pin. The RTC LDO includes pass transistor body diode control to avoid the RTCPWR node from back-charging into the input node VDDI.

Switching Frequency

The converters of CH1, CH3, CH4 and CH5 operate in PWM mode with 2MHz switching frequency. The converters of CH2 and CH7 operates in PWM mode with 1MHz switching frequency.

Power On/Off Sequence and Deglitch Function for CH1 to CH4

SEQ pull down resistance Rseq Defines power on/off sequence.

SEQ#	**R_{SEQ} (kΩ) Range**		
	Min	**Typ**	**Max**
SEQ #0	Short to Power (> 0.2V)		
SEQ #1	25	40	64
SEQ #2	6.25	10	16
SEQ #3	1.56	2.5	4
SEQ #4	--	0.63	1
SEQ #5	100	160	--

SEQ # 0 : CH2 CH3 CH4
(CH1 is decided by register A4 bit3.)
SEQ # 1 : CH1 → CH3 → CH2 → CH4
SEQ # 2 : CH1 → CH3 → CH4 → CH2
SEQ # 3 : CH1 → CH2 → CH4 → CH3
SEQ # 4 : CH1 → CH4 → CH3 → CH2 → CH5
SEQ # 5 : CH1 → CH4 → CH2 → CH3
Floating = resistance greater than 160kΩ = SEQ#5

Please follow below setting if channel not used.	
CH1	PVD1 = GND, LX1 = Floating and select SEQ #0. If SEQ #0 is not meet requirement, please use external BOM.
CH2	PVD2 = GND, LX2A = GND, LX2B = GND, VO2 = GND and FB2 connect to previous CHx's FB. Can't operate in the SEQ #0 and SEQ #3.
CH3	PVD3 = VSYS, LX3 = GND and FB3 connect to previous CHx's FB. Can't operate in the SEQ #1 and SEQ #2.
CH4	PVD4 = VSYS, LX4 = GND and FB4 connect to previous CHx's FB. Can't operate in the SEQ #4 and SEQ #5.
CH5	If use SEQ #4, PVD5 = VSYS, LX5 = GND or Floating and FB5 connect to CH2's FB. Otherwise FB5 = GND, PVD5 = VSYS, LX5 = GND or Floating.
CH7	FB7 = GND, LX7 = GND and PVD7 = GND.

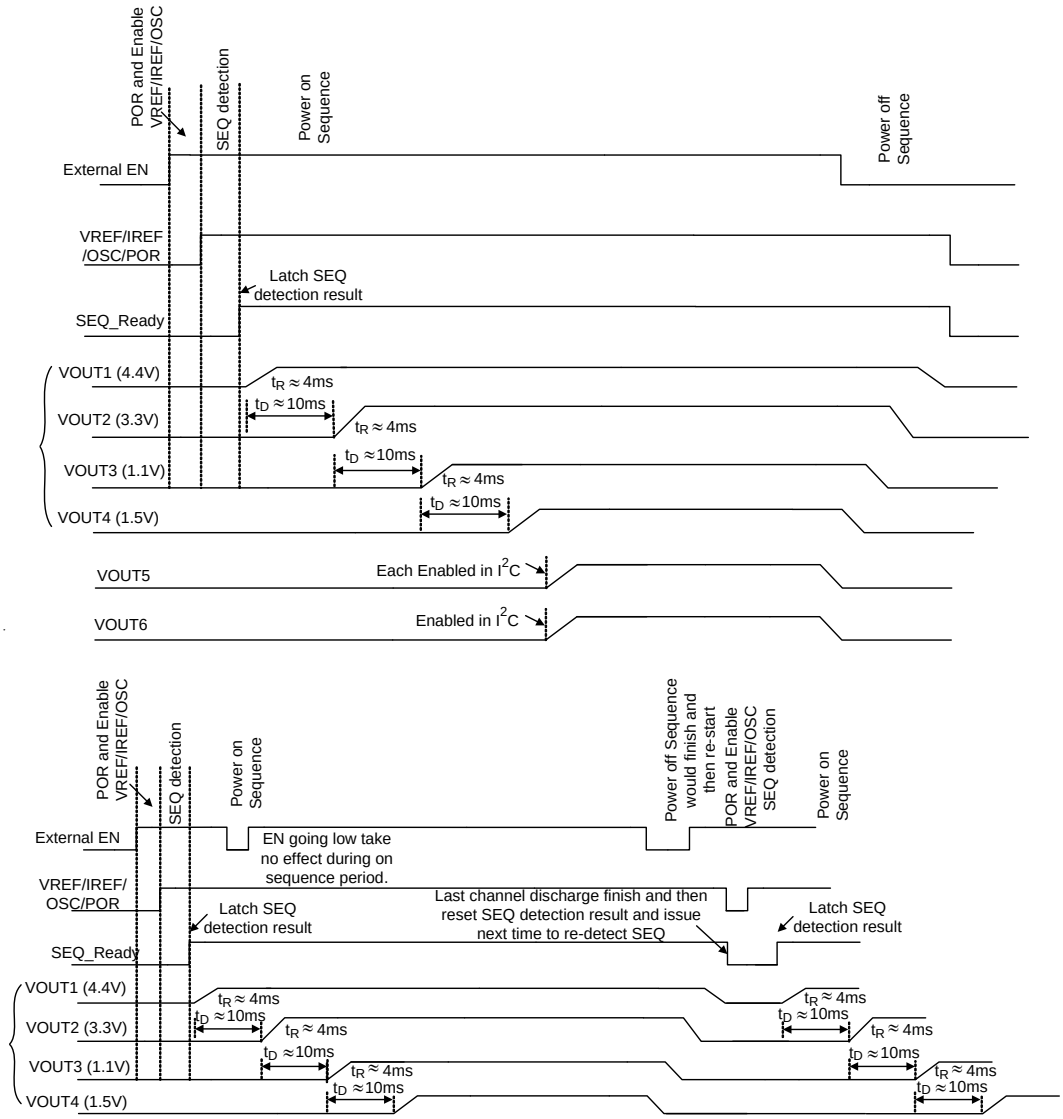
The power on sequence of CH1 to CH4 is shown below :

(Using SEQ #3 : CH1 → CH2 → CH4 → CH3 to explain)

When EN1234 goes high, CH1 will be turned on first then CH2 will be turned on after CH1 turn on for 10msec, likewise, CH4 will be turned on after CH2 turns on for 10msec. Finally, CH3 is turned on after CH4 turns on for 10msec. The soft-start time is 4msec for each channel.

The power off sequence of CH1 to CH4 is :

When EN1234 goes low, CH3 will turn off first and internally discharge output via LX3 pin. When FB3 < 0.1V, CH4 will turn off and also internally discharge output via the LX4 pin. When FB4 < 0.1V, CH2 will turn off and internally discharge output via the LX2 pin. Likewise, when FB2 < 0.1V, CH1 will turn off and discharge output. After FB1 < 0.1V, CH1 to CH4 shutdown sequence is completed.

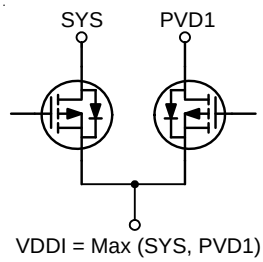


During On sequence period, EN going low would not take effect. After the sequence finish, EN state would be re-checked and decide to keep on or start off sequence.

During Off sequence period, EN going high would not take effect. After the sequence finish, EN state would be re-checked and decide to keep off or start on sequence.

VDDM Bootstrap

To support bootstrap function, the RT5024 provides a power selection circuit which selects the maximum voltage between SYS and PVD1 to support the power requirement at node VDDI. The RT5024 includes UVLO circuits to monitor VDDI and SYS voltage status.



Charger Unit

The RT5024 includes a Li-ion battery charger with Automatic Power Path Management. The charger is designed to operate in below modes :

- Pre-Charge Mode

  When the output voltage is lower than 2.8V, the charging current will be reduced to a ratio of the fast-charge current set by A8.ISETA [3:0] to protect the battery life-time. The timing diagram is showned in Figure 3.

- Fast-Charge Mode

  When the output voltage is higher than 3V, the charging current will be equal to the fast-charge current set by A8.ISETA [3:0] shown as Figure 3.

- Constant Voltage Mode

  When the output voltage is near 4.2V and the charging current falls below the termination current for a deglitch time of 25ms, the charger will be disabled and $\overline{CHG}$ will go high. The timing diagram is showed in Figure 3.

- Re-Charge Mode

  When the chip is in charge termination mode, the charging current gradually goes down to zero. Once the battery voltage drops to below 4.1V for a deglitch time of 100ms, the charger will resume charging shown as Figure 3.

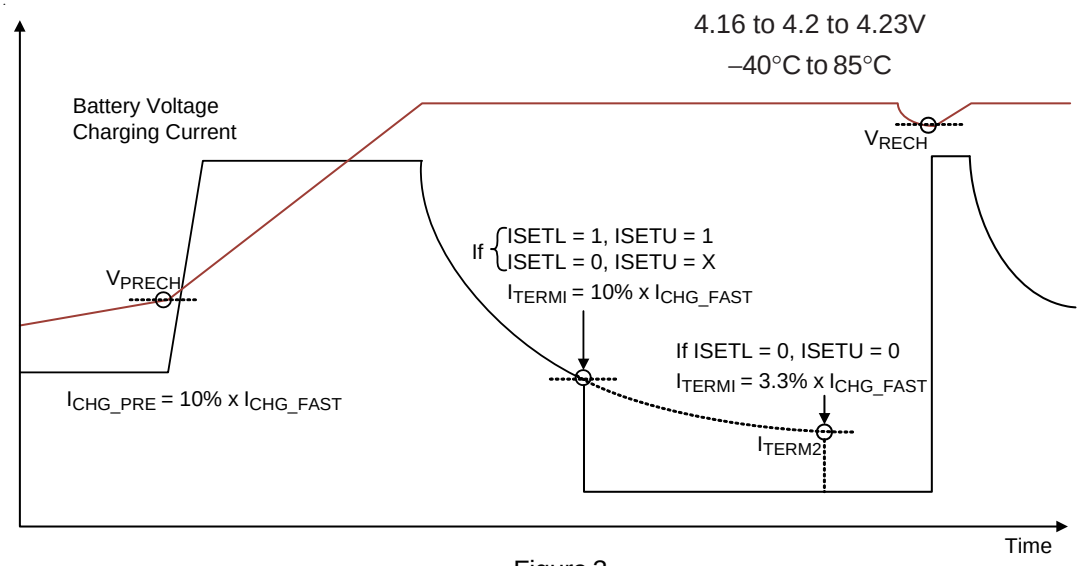


Figure 3

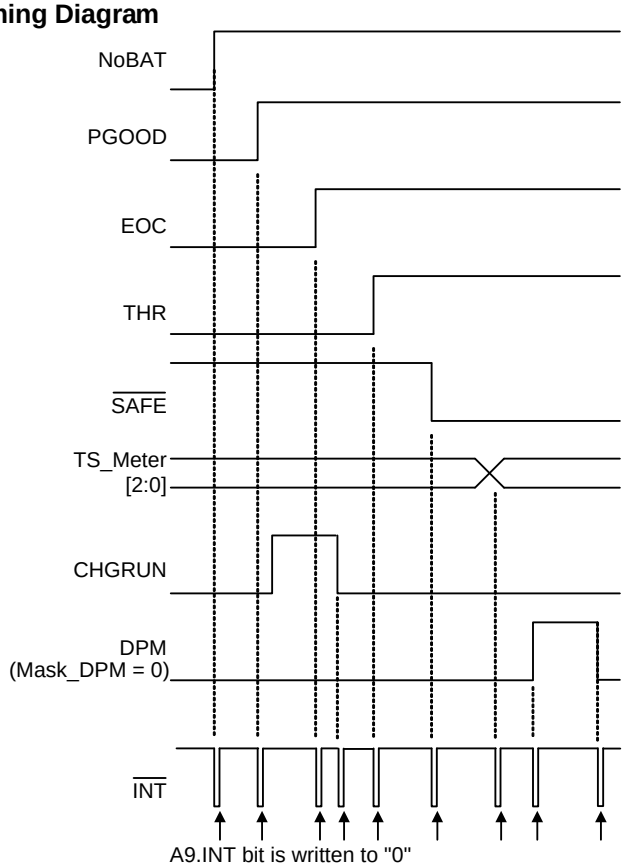
Interrupt Indicator

The RT5024 provides an interrupt indicator output pin ($\overline{INT}$). $\overline{INT}$ is an open drain output which is controlled by A9.INT bit. When the PGOOD, TS_Meter [2:0], EOC, THR, $\overline{SAFE}$, NoBAT, CHGRUN, DPM status bits toggle, the A9.INT bit will be set to high. In order to reset the interrupt status, a "0" must be written to the A9.INT bit or power on the PMU again. The timing diagram is shown below :

Interrupt vs. Events (I^2C Status Bits)

$\overline{INT}$ assert (Turn to low)	When PMU turns on with event condition		During PMU on	
	No Event (0)	Event has occurred (1)	Event appear (0 → 1)	Event disappear (1 → 0)
PGOOD	No	Yes	Yes	Yes
NoBAT	No	Yes	Yes	Yes
TS_METER [2:0] = 000 (Event may be cold or hot, VP UVLO, NoBAT)	No	Yes	Yes	Yes
EOC	No	Yes	Yes	Yes
THR	No	Yes	Yes	Yes
$\overline{SAFE}$	No	Yes	Yes	Yes
DPM	No	Yes	Yes	Yes
CHGRUN	No	No	No	Yes

$\overline{INT}$ vs. Fault/Status Timing Diagram



When the A9.INT bit is written to "0", the $\overline{INT}$ will be set to high.

When Mask_DPM = 1 and DPM event change, the $\overline{INT}$ would not be asserted.

Battery Installation Detection

RT5024 also detects TS voltage to monitor the battery status. If PMU is enabled but TS voltage > 90% of VP node voltage, RT5024 sets the bit

NoBAT = 1 an I²C register A10.NoBAT and sets A9.INT bit to "1".

NoBAT	1	No Battery Installed (TS > 90% of VP)
	0	BAT Installed

VIN Power Good Status

PGOOD	0	VIN < VUVLO
	0	VUVLO < VIN < VBAT + VOS_L
	1	VBAT + VOS_H < VIN < VOVP
	0	VIN > VOVP

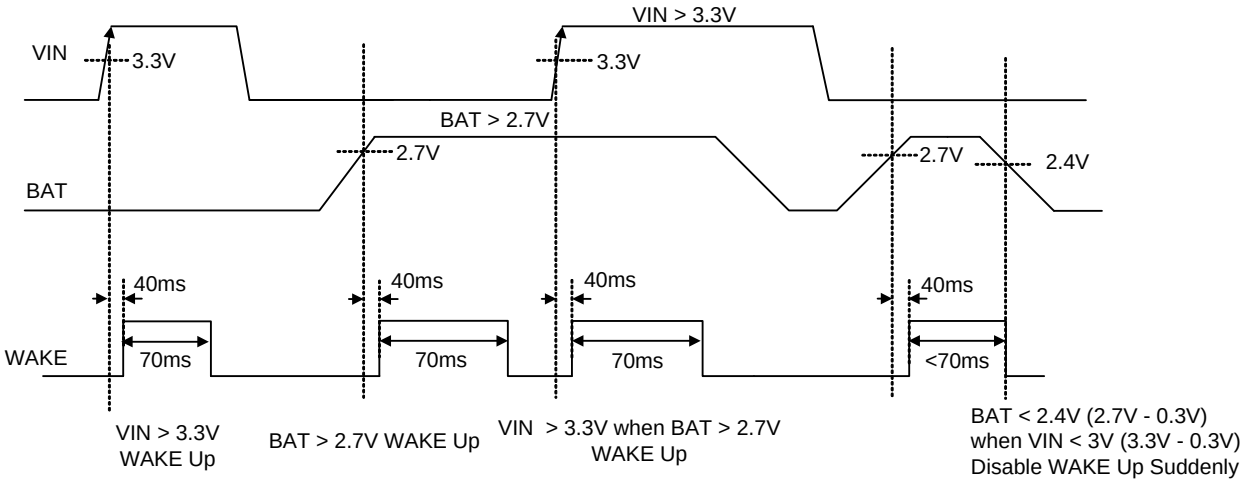
End_Of_Charge (EOC) Status

The bit EOC in I²C register A10.EOC can show the EOC status. If EOC = 1, the charger is in EOC state and A9.INT bit is set to "1"

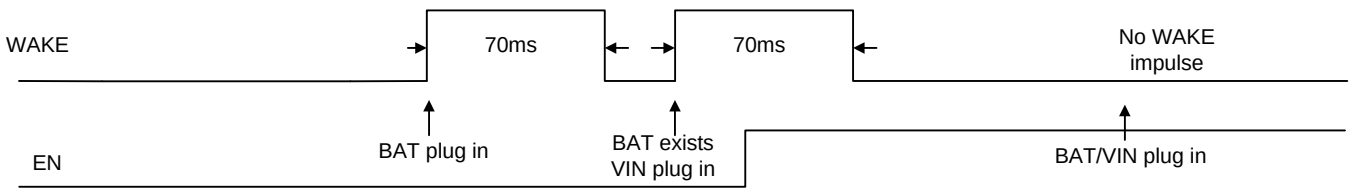
EOC	1	Charging Done or Recharging after Termination
	0	During Charging

Wake-Up Detector

Wake-Up Detector detects VIN or BAT plug-in events. Once BAT plugs in or VIN plugs in for a 40msec deglitch time, the WAKE pin will provide a 70ms width high pulse. The timing diagram shows as below.



When PMU is enabled, WAKE UP impulse would be masked off. WAKE impulse width 70ms can not be cut by EN = H



Suspend Mode

When USUS = 1, the charger will enter Suspend Mode. In Suspend Mode, $\overline{CHG}$ pin is high impedance and IUSUS(MAX) < 300μA.

Charging Current Decision

The charge current can be set according to the I^2C register A8.ISETA [3:0] setting :

	RT5024 allows user to set the battery charge current level and the list as below. The default value is 0.5A.							
ISETA [3:0]	**Code**	**BAT Charge Current**	**Code**	**BAT Charge Current**	**Code**	**BAT Charge Current**	**Code**	**BAT Charge Current**
	0000	0.1A	0001	0.2A	0010	0.3A	0011	0.4A
	0100	0.5A	0101	0.6A	0110	0.7A	0111	0.8A
	1000	0.9A	1001	1A	1010	1.1A	1011	1.2A
	1100	1.2A	1101	1.2A	1110	1.2A	1111	1.2A

Fault-Time

During the fast charge phase, several events may increase the charging time.

For example, the system load current may have activated the APPM loop which reduces the available charging current or the device has entered thermal regulation because the IC junction temperature has exceeded T_{REG}.

However, once the duration exceeds the fault-time, the $\overline{CHG}$ output pin will flash at approximately 4Hz to indicate a fault condition and the charge current will be reduced to about 1mA.

There are four methods to release the Fault-time :

- Re-plug power
- Toggle EN
- Enter/exit suspend mode
- Remove Battery
- OVP

The fault-time is inverse proportional to the charger current.

$$\text{Fault-Time} \propto \frac{1}{\text{Icharge}}$$

Example :

If the sensing battery temperature is hot or cold, the charge current will reduce to half charge current. So, the fault-time will increase to be double.

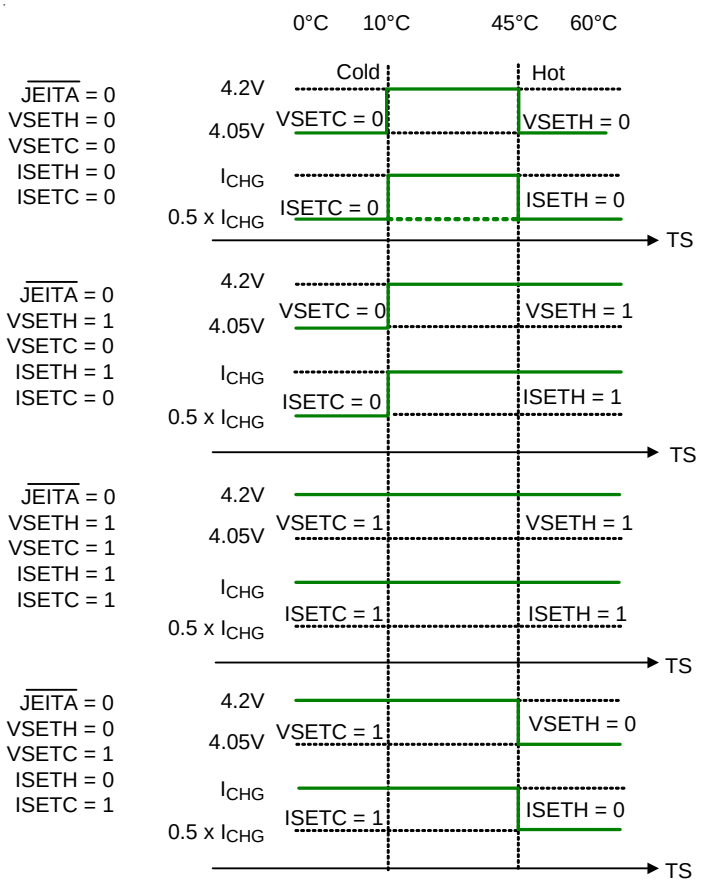
JEITA Battery Temperature Standard

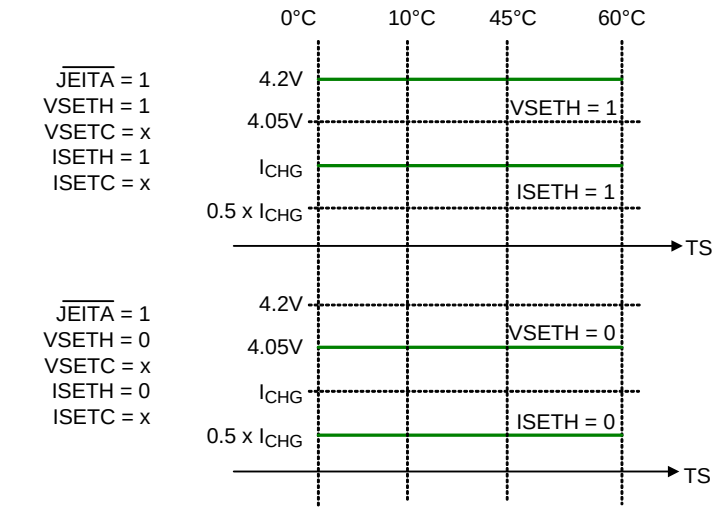
CV regulation voltage will be changed in the following battery temperature ranges : 0°C to 10°C and 45°C to 60°C.

This function can be disabled by A9.VSETH and A9.VSETC.

CC regulation current will be changed in the following battery temperature ranges : 0°C to 10°C and 45°C to 60°C.

This function can be disabled by A9.ISETH and A9.ISETC.





Battery Pack Temperature Monitoring

The battery pack temperature monitoring function can be realized by connecting the TS pin to an external Negative Temperature Coefficient (NTC) thermal resistor to prevent over temperature condition. Charging is suspended when the voltage at the TS pin is out of normal operating range. The internal timer is then paused, but the value is maintained.

When the TS pin voltage returns to normal operating range, charging will resume and the safe charge timer will continue to count down from the point where it was suspended. Note that although charging is suspended due to the battery pack temperature fault, the $\overline{CHG}$ pin will flash at 0.5Hz and indicate charging.

The 3.3V at VP pin is buffered by the RT5024 once it is in charging state or its PMU part is enabled. If a 100kΩ NTC thermal resistor is used, the A0.TSSEL bit should be set to "1". If a 10kΩ NTC thermal resistor is used, the A0.TSSEL bit should be set to "0". The TSSEL bit determines the TS threshold levels for 0°C and 60°C. It also defines the TS threshold levels used in JEITA operation. The choosing method of R1 and R2 to meet battery temperature monitoring shows as below.

Case 1 : TSSEL = H (For 100kΩ NTC) :

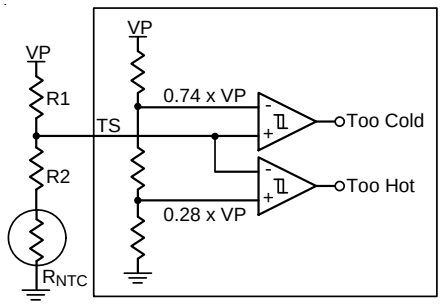


Figure 4

Too Cold Temperature

$R_{COLD} = R_{NTC}$

Too Hot Temperature

$R_{HOT} = R_{NTC}$

$$\frac{R2+R_{COLD}}{R_{COLD}+R1+R2} = 0.74 \quad \text{----------} \quad (1)$$

$$\frac{R2+R_{HOT}}{R_{HOT}+R1+R2} = 0.28 \quad \text{----------} \quad (2)$$

Form (1), (2)

$$R1 = \frac{R_{COLD}-R_{HOT}}{2.457}$$

$$R2 = 0.389 \times R1 - R_{HOT}$$

If R2 < 0

$$\frac{R_{COLD}}{R_{COLD}+R1} = 0.74 \quad \text{----------} \quad (3)$$

Form (3)

$$R1 = \frac{R_{COLD}}{0.74} - R_{COLD}$$

Case 2 : TSSEL = L (For 10kΩ NTC) :

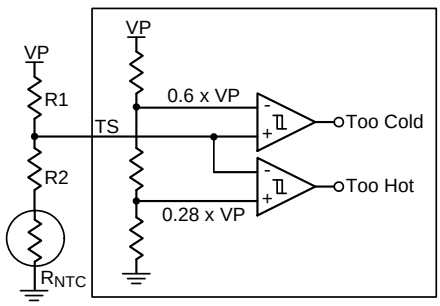


Figure 5

Too Cold Temperature

$R_{COLD} = R_{NTC}$

Too Hot Temperature

$R_{HOT} = R_{NTC}$

$$\frac{R2+R_{COLD}}{R_{COLD}+R1+R2} = 0.6 \quad \text{----------} \quad (1)$$

$$\frac{R2+R_{HOT}}{R_{HOT}+R1+R2} = 0.28 \quad \text{----------} \quad (2)$$

Form (1), (2)

$$R1 = 0.9 \times (R_{COLD} - R_{HOT})$$

$$R2 = 0.388 \times R1 - R_{HOT}$$

If R2 < 0

$$\frac{R_{COLD}}{R_{COLD}+R1} = 0.6 \quad \text{----------} \quad (3)$$

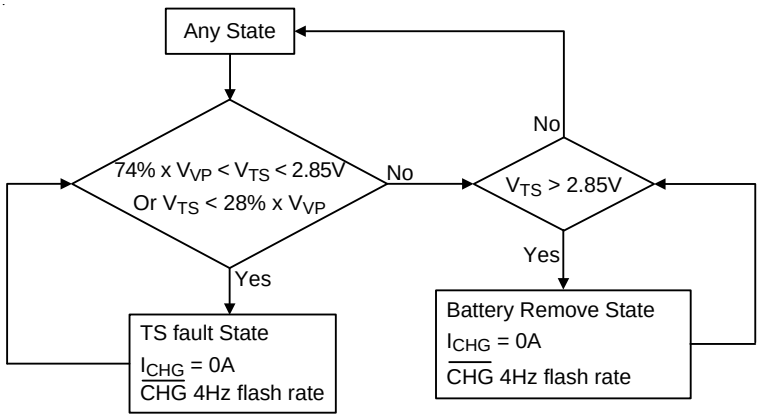
Form (3)

$$R1 = \frac{R_{COLD}}{0.6} - R_{COLD}$$

The Control Temperature Used in JEITA Operation

The above calculation gives R1 and R2. JEITA control thresholds for full charging current and 4.2V regulation voltage are at TS/VP ratio = 32% and 52% (for TSSEL = L), 35% and 64% (for TSSEL = H). With the ratio, the corresponding NTC thermistor resistances from the resistors in the voltage divider circuit can be obtained. According to the NTC resistances, the corresponding temperatures can be found. The two temperatures are the control temperatures used in JEITA operation.

Operation State Diagram for TS Pin (TSSEL = H)



Power Switch

For the charger, there are three power scenarios :

- When a battery and an external power supply (USB or adapter) are connected simultaneously

  If the system required load exceeds the input current limit, the battery will be used to supplement the current to the load. However, if the system load is less than the input current limit, the excess power from the external power supply will be used to charge the battery.

- When only the battery is connected to the system

  The battery provides the power to the system.

- When only an external power supply is connected to the system

  The external power supply provides the power to the system.

Input DPM Mode

For the charger, the input voltage is monitored when USB100 or USB500 is selected. If the input voltage is lower than VDPM, the input current limit will be reduced to stop the input voltage from dropping further. This can prevent the IC from damaging improperly configured or inadequately designed USB sources.

If VIN charger type is detected as SDP, the DPM function always is enabled.

For other types, the DPM function always is disabled but user can set A0.ENDPM to turn on the DPM function.

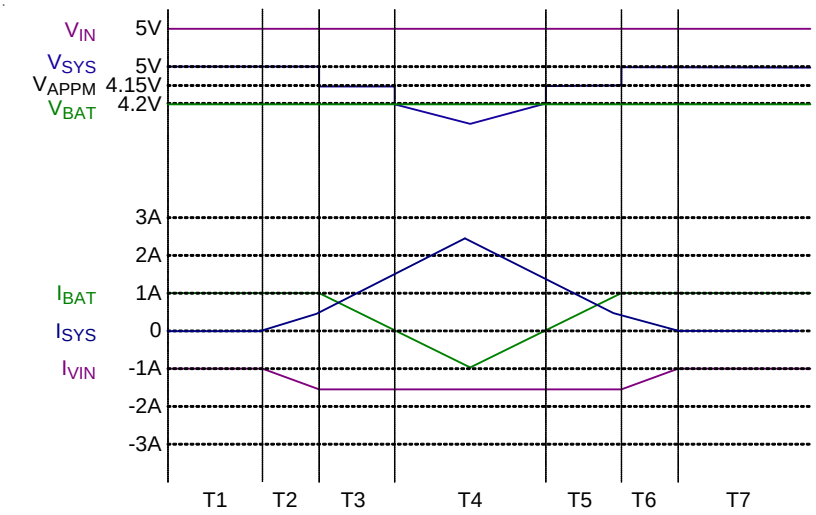
ENDPM	Enable the charger VIN DPM function. But if VIN charger type is detected as SDP (CHG_TYP [2:0] = 000), the DPM function always is enabled.
	0 : VIN DPM function disabled.
	1 : VIN DPM function enabled.

APPM Mode

Once the sum of the charging current and system load current is higher than the maximum input current limit, the SYS pin voltage will be reduced. When the SYS pin voltage is reduced to V_{APPM}, the RT5024 will automatically operate in APPM mode. In this mode, the charging current is reduced while the SYS current is increased to maintain system output. In APPM mode, the battery termination function is disabled.

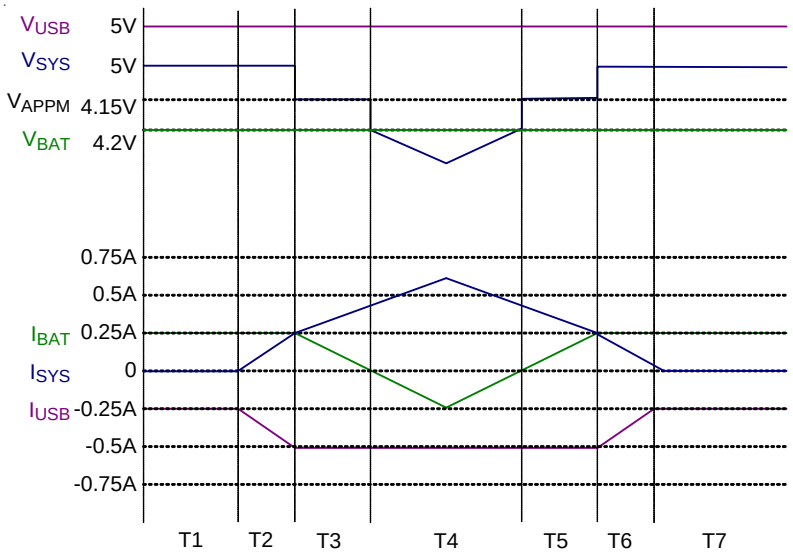
APPM Profile

1.5A Mode :



	I_{SYS}	V_{SYS}	I_{VIN}	I_{BAT}
T1, T7	0	SYS Regulation Voltage	CHG_MAX	CHG_MAX
T2, T6	< I_{VIN_OC} – CHG_MAX	SYS Regulation Voltage	I_{SYS} + CHG_MAX	CHG_MAX
T3, T5	> I_{VIN_OC} – CHG_MAX < I_{VIN_OC}	Auto Charge Voltage Threshold	V_{IN_OC}	V_{IN_OC} – I_{SYS}
T4	> I_{VIN_OC}	V_{BAT} – I_{BAT} x $R_{DS(ON)}$	V_{IN_OC}	I_{SYS} – I_{VIN_OC}

500mA Mode :



	I_{SYS}	V_{SYS}	I_{USB}	I_{BAT}
T1, T7	0	SYS Regulation Voltage	CHG_MAX	CHG_MAX
T2, T6	< I_{VIN_OC} (USB) – CHG_MAX	SYS Regulation Voltage	I_{SYS} + CHG_MAX	CHG_MAX
T3, T5	> I_{VIN_OC} (USB) – CHG_MAX < I_{VIN_OC} (USB)	Auto Charge Voltage Threshold	I_{VIN_OC} (USB)	I_{VIN_OC} (USB) – I_{SYS}
T4	> I_{VIN_OC} (USB)	V_{BAT} – I_{BAT} x $R_{DS(ON)}$	I_{VIN_OC} (USB)	I_{SYS} – I_{VIN_OC} (USB)

Battery Supplement Mode Short Circuit Protect

In APPM mode, the SYS voltage will continue to drop if the charge current is zero and the system load increases beyond the input current limit. When the SYS voltage decreases below the battery voltage, the battery will kick in to supplement the system load until the SYS voltage rises above the battery voltage.

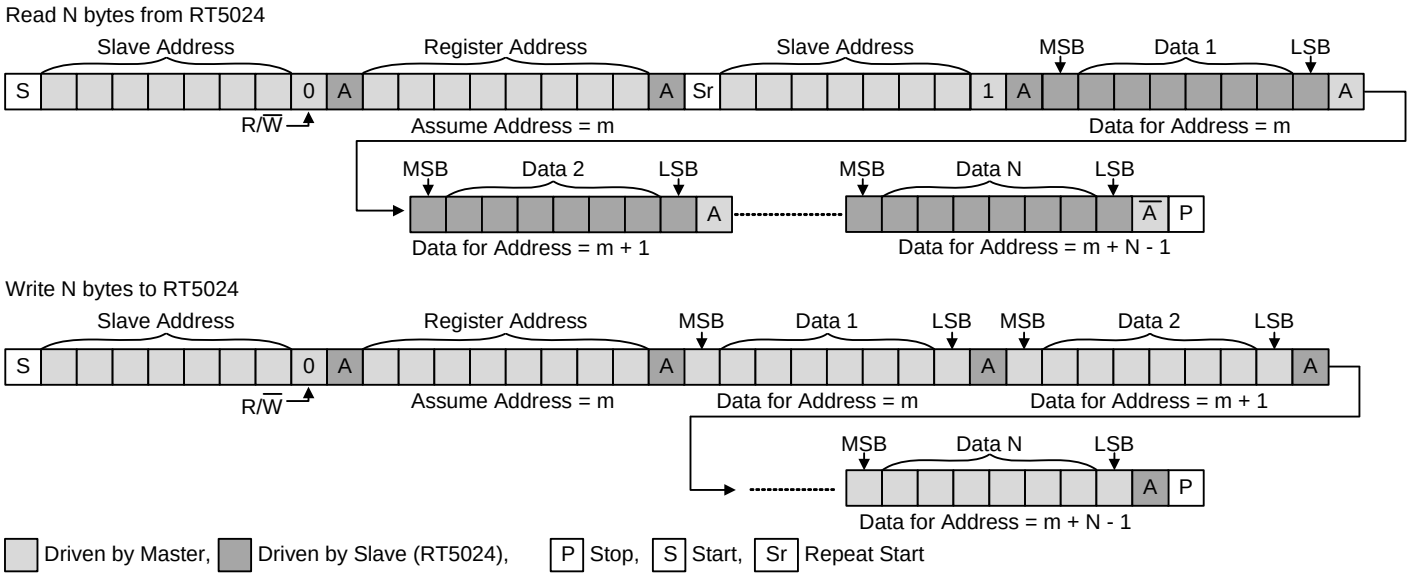
While in supplement mode, there is no battery supplement current regulation. However, a built-in short circuit protection feature is available to prevent any abnormal current situation. While the battery is supplementing the load, if the difference between the battery and SYS voltage exceeds the short circuit threshold voltage, SYS will be disabled. After a short circuit recovery time, t_{SHORT_R}, the counter will be restarted. In supplement mode, the battery termination function is disabled. Note that the battery supply mode exiting condition is $V_{BAT} – V_{SYS} < 0V$.

Thermal Regulation and Thermal Shutdown

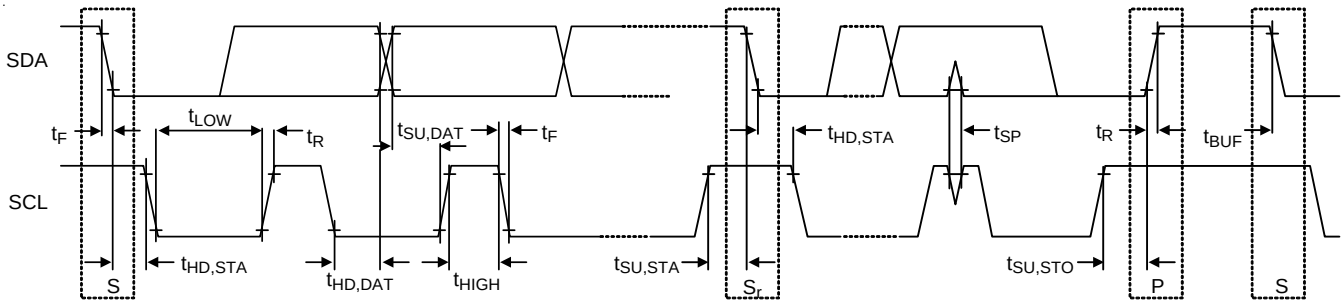
The charger provides a thermal regulation loop function to monitor the device temperature. If the die temperature rises above the regulation temperature, T_{REG}, the charge current will automatically be reduced to lower the die temperature. However, in certain circumstances (such as high VIN, heavy system load, etc.) even with the thermal loop in place, the die temperature may still continue to increase. In this case, if the temperature rises above the thermal shutdown threshold, T_{SD}, the internal switch between VIN and SYS will be turned off. The switch between the battery and SYS will remain on, however, to allow continuous battery power to the load. Once the die temperature decreases by ΔT_{SD}, the internal switch between VIN and SYS will be turned on again and the device returns to normal thermal regulation. The internal thermal feedback circuitry regulates the die temperature to optimize the charge rate for all ambient temperatures.

I²C Interface

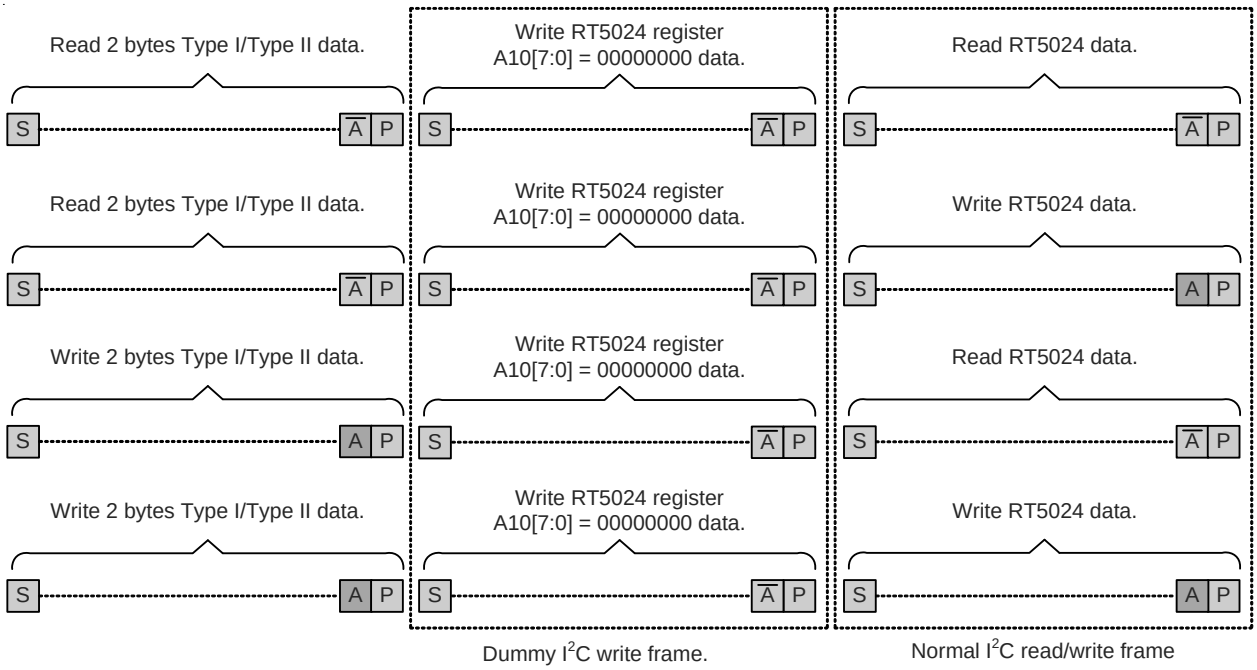
RT5024 I²C slave address = 0010010 (7 bits). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



I²C Waveform Information

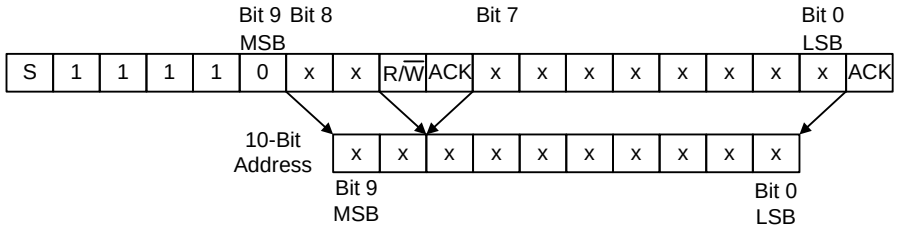


When RT5024 and other I²C devices with 10-bit slave addressing (type I) or two-byte register addressing (type II) coexist in one I²C bus, RT5024 need one dummy I²C write frame to reset the RT5024 internal I²C operation state. The below shows a dummy write frame example, that is to write RT5024 register A10 [7:0] = 00000000. Master should ignore the write operation (This operation is invalid). After the dummy frame, the master can read/write formal I²C frame for RT5024 to get right operation.



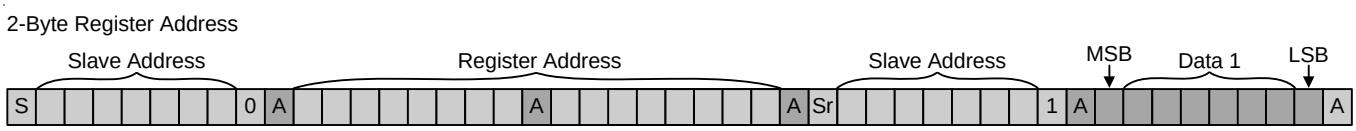
Type I : 10-bit slave address data format

In 10-bit addressing, the slave address is sent in the first two bytes. The first byte begins with the special reserved address of 11110XX which indicates that 10-bit addressing is being used.



Type II : 2-byte register address data format

The register address is combined with 2-byte as below.



Note : I²C start operate after power on sequence finish and success.

I²C Register File

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A0	0x00	Meaning	RST_P	RST_C	OVP7	CHGST	ENDPM	TSD	MOD7	TSSEL
		Default	1	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
RST_P			RT5024 would reset PMU-related registers under any one of two conditions as below : 1) VDDI < 1.3V 2) (EN pin = low and A0.RST_P = 1) In the 2nd condition, RT5024 uses the register bit A0.RST_P to decide whether the PMU-related registers are reset or not when EN pin goes low.							
			0: Don't reset register (0x3 to 0x6)							
			1: Reset register (0x3 to 0x6).							
RST_C			RT5024 would reset Charge-related register under any one of three conditions as below : 1) VIN < 4V 2) VDDI < 1.3V 3) (BAT < 3.1V) and (A0.RST_C = 1) In the 3rd condition, RT5024 uses the register bit A0.RST_C to decide whether the Charge-related registers are reset or not when BAT < 3.1V.							
			0: Don't reset register (0x7 to 0x9).							
			1: Reset register (0x7 to 0x9)							
OVP7			CH7 allow user to select the OVP level by I²C interface							
			0 : 16V OVP							
			1 : 25V OVP							
CHGST			Used to control how $\overline{CHG}$ open drain port shows the charging events.							
			0 : $\overline{CHG}$ port output low when charging.							
			1 : $\overline{CHG}$ port output a flicker signal with 0.5Hz.							
ENDPM			Enable the charger VIN DPM function. But if VIN charger type is detected as SDP (CHG_TYP [2:0] = 000), the DPM function always is enabled.							
			0 : VIN DPM function disabled							
			1 : VIN DPM function enabled.							
TSD			Report whether thermal shutdown of PMU ever occurs. Reset it by writing 0 into the bit or (VDDI < 1.3V).							
			0 : Thermal Shutdown has not occurred.							
			1 : Thermal Shutdown event ever occurs.							
MOD7			Report the result of CH7 mode detection.							
			0 : Current Source.							
			1 : Boost.							
TSSEL			TS/VP ratio setting for battery temperature.							
			0 : TS/VP = 60% (0°C). 28% (60°C)							
			1 : TS/VP = 74% (0°C). 28% (60°C)							

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A1	0x01	Meaning	ERR1	ERR2	ERR3	ERR4	ERR5	ERR6	ERR7	ERR8
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ERR1 to ERR8			Report whether the protection event of CH1 to CH8 ever occurs respectively. Reset it by writing 0 into the bit or (VRTC < 1.6V).							
			0 : No protection event occurs.							
			1 : Protection event ever occurs.							

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A2	0x02	Meaning	EN5	EN6	EN8	EN7_DIM7 [4:0]				
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EN5			Enable/disable CH5							
			0 : Disable							
			1 : Enable							
EN6			Enable/disable CH6							
			0 : Disable							
			1 : Enable							
EN8			Enable/disable CH8							
			0 : Disable							
			1 : Enable							
EN7_DIM7 [4:0]			Enable CH7 and defines FB7 regulation voltage							
			00000 : CH7 turn off							
			00001 to11111 : CH7 turns on and dimming ratio : VFB7 = EN7_DIM7 [4:0] / 31 x 0.25V							

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A3	0x03	Meaning	PSM1	PSM2	PSM3	PSM4	VOUT8 [3:0]			
		Default	1	1	1	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PSM1 to PSM4			Define the CH1/2/3/4 CCM or PWM/PSM switching operation.							
			0 : Force PWM							
			1 : Automatic PWM/PSM switch operation							
VOUT8 [3:0]			CH8 regulation voltage can be selected by I^2C interface. The default voltage is 2.5V.							
			Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
			0000	1V	0001	1.1V	0010	1.2V	0011	1.3V
			0100	1.4V	0101	1.5V	0110	1.6V	0111	1.7V
			1000	1.8V	1001	2V	1010	2.2V	1011	2.3V
			1100	2.5V	1101	2.6V	1110	2.7V	1111	2.8V

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit	Bit0 (LSB)
A4	0x04	Meaning	VOUT1 [3:0]				EN1	FB2 [2:0]		
		Default	0	1	0	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VOUT1 [3:0]	CH1 regulation voltage can be selected by I^{2}C interface. The default voltage is 4.4V.							
	Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
	0000	3.6V	0001	3.7V	0010	3.8V	0011	3.9V
	0100	4V	0101	4.4V	0110	4.6V	0111	4.7V
	1000	4.8V	1001	4.9V	1010	5V	1011	5.1V
	1100	5.2V	1101	5.3V	1110	5.4V	1111	5.5V
EN1	Enable/Disable CH1 when sequence ID is SEQ#0. In SEQ#0, CH1 is not in the power on/off sequence. In other sequence, CH1 is in sequence control and on/off by the pin EN, not by the register bit EN1.							
	0 : Disable							
	1 : Enable							

FB2 [2:0]	FB2 regulation voltage can be selected by I^{2}C interface. The default voltage is 0.8V.			
	Code	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A5	0x05	Meaning	Reserved	FB3 [2:0]			Reserved	FB4 [2:0]		
		Default	x	1	0	0	x	1	0	0
		Read/Write	--	R/W	R/W	R/W	--	R/W	R/W	R/W

FB3 [2:0]	FB3 regulation voltage can be selected by I^{2}C interface. The default voltage is 0.8V.				
	Code	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

FB4 [2:0]	FB4 regulation voltage can be selected by I^{2}C interface. The default voltage is 0.8V.				
	Code	**VREF**	**If Target = 1.8V**	**If Target = 1V**	**If Target = 3.3V**
	000	0.72V	1.62V	0.9V	2.97V
	001	0.74V	1.665V	0.925V	3.0525V
	010	0.76V	1.71V	0.95V	3.135V
	011	0.78V	1.755V	0.975V	3.2175V
	100	0.8V	1.8V	1V	3.3V
	101	0.82V	1.845V	1.025V	3.3825V
	110	0.84V	1.89V	1.05V	3.465V
	111	0.86V	1.935V	1.075V	3.5475V

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A6	0x06	Meaning	VOUT5 [3:0]				VOUT6 [3:0]			
		Default	0	0	0	0	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VOUT5 [3:0]							
CH5 regulation voltage can be selected by I^2C interface. The default voltage is REF.							
Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
0000	REF	0001	1.1V	0010	1.2V	0011	1.3V
0100	1.4V	0101	1.5V	0110	1.6V	0111	1.7V
1000	1.8V	1001	2V	1010	2.2V	1011	2.3V
1100	2.5V	1101	2.6V	1110	2.7V	1111	2.8V
Note : VOUT5 [3:0] = 0000 (REF) means using external feedback network and FB5 regulation target is 0.8V ± 1.5%							

VOUT6 [3:0]							
CH6 regulation voltage can be selected by I^2C interface. The default voltage is 1.8V.							
Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
0000	1.2V	0001	1.3V	0010	1.5V	0011	1.6V
0100	1.8V	0101	2V	0110	2.2V	0111	2.4V
1000	2.7V	1001	3V	1010	3.1V	1011	3.2V
1100	3.3V	1101	3.4V	1110	3.6V	1111	3.7V

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A7	0x07	Meaning	TIMER [3:0]				$\overline{\text{ENCH}}$	USUS	ISETU	ISETL
		Default	0	1	0	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TIMER [3:0]	Define fast charger safe charging time. Fast charging timeout time = (TIMER [3:0] + 1) hours. The default voltage is 5 hours. Note : pre-charge timeout time = fast charge time/8.
$\overline{\text{ENCH}}$	Enable charger
	0 : Enable charger
	1 : Disable charger
USUS	VIN Suspend control
	0 : No suspend
	1 : Suspend

ISETU and ISETL

VIN Current limit setting :

ISETL	ISETU	VIN Input Current Limit
0	0	95mA
0	1	475mA (default)
1	0	1A
1	1	1.5A

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A8	0x08	Meaning	TSHT[1:0]		Mask_DPM	Reserved	ISETA [3:0]			
		Default	0	0	0	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Mask_DPM	To determine whether interrupt event triggered by charger VIN DPM status toggling is masked off or not.
	0 : When DPM event change, $\overline{INT}$ would be asserted.
	1 : When DPM event change, $\overline{INT}$ would not be asserted.

TSHT [1:0]

Set TS/VP threshold to monitor battery temperature for HOT boundary.

Code	TS/VP ratio	Equivalent Battery Temperature	
		10k NTC	100k NTC
00	28%	60°C	60°C
01	28.5%	58°C	59°C
10	29%	56°C	57°C
11	29.5%	54°C	56°C

ISETA [3:0]

RT5024 allows user to set the battery charge current level and the list as below. The default value is 0.5A.

Code	BAT Charge Current	Code	BAT Charge Current	Code	BAT Charge Current	Code	BAT Charge Current
0000	0.1A	0001	0.2A	0010	0.3A	0011	0.4A
0100	0.5A	0101	0.6A	0110	0.7A	0111	0.8A
1000	0.9A	1001	1A	1010	1.1A	1011	1.2A
1100	1.2A	1101	1.2A	1110	1.2A	1111	1.2A

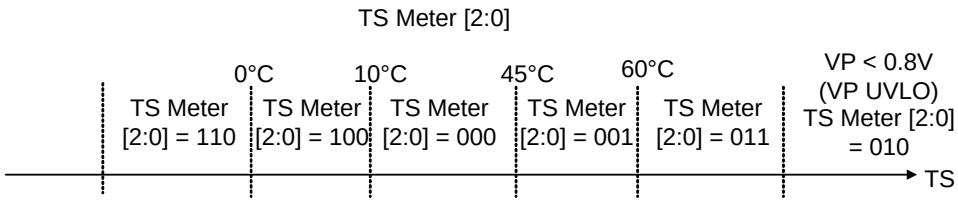
Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A9	0x09	Meaning	$\overline{JEITA}$	VSETH	VSETC	ISETH	ISETC	Reserved	INT	DPM
		Default	0	0	1	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

$\overline{JEITA}$, VSETH, VSETC, ISETH, ISETC	BAT charge current and regulation voltage control scheme.
	$\overline{JEITA}$ = 0, it means the charger operation is automatic (JEITA rule).
	$\overline{JEITA}$ = 1, User can set the VSETH/VSETC to decide the BAT regulate voltage and set ISETH/ISETC to decide the BAT charge current level. The control scheme is listed as below.
INT	Control the output of $\overline{INT}$ open drain port. The bit value is inverted of $\overline{INT}$ output. When interrupt events happen, INT port goes low and this bit A9. INT would be triggered to 1. Micro-processor must write this bit to be 0 for making INT go high.
	0 : $\overline{INT}$ = High
	1 : $\overline{INT}$ = Low
DPM	The DPM bit is the charger VIN DPM status bit. It means the charger DPM (VIN falls and regulates at 4.35V) is activated or not.
	0 : VIN DPM not activated.
	1 : VIN DPM activated (working).
	Note : when PMU turns on, it would check the bit DPM and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once DPM bit toggles, INT also asserts again.

Address Name	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A10	0x0A	Meaning	TS_METER [2:0]			NoBAT	EOC	PGOOD	THR	$\overline{SAFE}$
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R

TS_METER [2:0]

Reports the battery temperature and VP status by detecting the TS pin voltage.



Note : when PMU turns on, it would check TS_Meter [2:0] and compare to the value 000. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once any bits of TS_Meter [2:0] toggles, $\overline{INT}$ also asserts again.

NoBAT

Means the battery installed or not.

0 : BAT Installed

1 : No Battery Installed (TS > 90% of VP)

Note : when PMU turns on, it would check the bit NoBAT and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once NoBAT bit toggles, $\overline{INT}$ also asserts again.

EOC

End of charge (EOC) bit shows the charge status. If EOC = 1 means the charger is in EOC status.

0 : During Charging

1 : Charging Done or Recharging after Termination

Note : when PMU turns on, it would check the bit EOC and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once EOC bit toggles, $\overline{INT}$ also asserts again.

PGOOD

PGOOD bit means the VIN power status.

Input Status	PGOOD Bit Status
VIN < VUVLO	0
VUVLO < VIN < VBAT + VOS_L	0
VBAT + VOS_H < VIN < VOVP	1
VIN > VOVP	0

Note : when PMU turns on, it would check the bit PGOOD and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once PGOOD bit toggles, $\overline{INT}$ also asserts again.

THR	THR bit can let user monitor whether the thermal regulation function is working or not.
	0 : thermal Regulation is not working
	1 : thermal Regulation is working
	Note : when PMU turns on, it would check the bit THR and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once THR bit toggles, $\overline{INT}$ also asserts again.
$\overline{SAFE}$	Charger safety timer status.
	0 : charger in charging or suspended by thermal loop
	1 : safety timer expired
	Note : when PMU turns on, it would check the bit $\overline{SAFE}$ and compare to the value 0. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once $\overline{SAFE}$ bit toggles, $\overline{INT}$ also asserts again.

Address Names	Register Address		Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)
A11	0x0B	Meaning	CHG_TYP [2:0]			Reserved	Reserved	CHG_2DET	CHG_1DET	CHGRUN
		Default	0	0	0	x	x	0	1	0
		Read/Write	R	R	R	--	--	R/W	R/W	R

CHG_TYP [2:0]	The CHG_TYP [2:0] is used to recode the charger type.			
	Code	**Charger Type**	**Code**	**Charger Type**
	000	Standard USB CHARGER (SDP)	100	APPLE CHARGER (1A)
	001	Sony CHARGER -1	111	DEDICATED CHARGER (DCP)
	010	Sony CHARGER -2	110	Charging Downstream Port (CDP) (High current Host/Hub)
	011	APPLE CHARGER (0.5A)		
CHG_2DET	The CHG_2DET bit is used to enable the secondary charger detection (to distinguish CDP and DCP). Default value is 0. Set this bit value to 1 in order to enable charger detection.			
	0 : Secondary CHARGER DETECTION DISABLED			
	1 : Secondary CHARGER DETECTION ENABLE.			
CHG_1DET	The CHG_1DET bit is used to enable the primary charger detection. Default value is 1 (auto-detect charger type when VIN plug in). Toggle this bit value (set to 0 and then set 1) to re-enable charger detection.			
	0 : Primary CHARGER DETECTION DISABLED.			
	1 : Primary CHARGER DETECTION ENABLE.			
CHGRUN	The CHGRUN bit is the charger detector status bit. It means the charger detection is running or not.			
	0 : CHARGER DETECTION NOT RUNING.			
	1 : CHARGER DETECTION RUNNING.			
	Note : when PMU turns on, it would check the bit CHGRUN and compare to the value 1. If it is different, $\overline{INT}$ would be asserted. After PMU is on, once CHGRUN bit change from 1 to 0, $\overline{INT}$ also asserts again.			

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0	0x00	Meaning	RST_P	RST_C	OVP7	CHGST	ENDPM	TSD	MOD7	TSSEL
		Default	1	0	0	1	0	0	0	1
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
		Reset Condition	A	A	A	D	A	A	H	A
A1	0x01	Meaning	ERR1	ERR2	ERR3	ERR4	ERR5	ERR6	ERR7	ERR8
		Default	0	0	0	0	0	0	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	A	A	A	A	A	A	A	A
A2	0x02	Meaning	EN5	EN6	EN8	EN7_DIM7 [4:0]				
		Default	0	0	0	0	0	0	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	B	B	B	B	B	B	B	B
A3	0x03	Meaning	PSM1	PSM2	PSM3	PSM4	VOUT8 [3:0]			
		Default	1	1	1	1	1	1	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
A4	0x04	Meaning	VOUT1 [3:0]				EN1	FB2 [2:0]		
		Default	0	1	0	1	0	1	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	B	C	C	C
A5	0x05	Meaning	Reserved	FB3[2:0]			Reserved	FB4[2:0]		
		Default	x	1	0	0	x	1	0	0
		Read/ Write	--	R/W	R/W	R/W	--	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C
A6	0x06	Meaning	VOUT5 [3:0]				VOUT6 [3:0]			
		Default	0	0	0	0	0	1	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	C	C	C	C	C	C	C	C

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A7	0x07	Meaning	TIMER [3:0]				$\overline{\text{ENCH}}$	USUS	ISETU	ISETL
		Default	0	1	0	0	0	0	1	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	D	D	D	D	D	D	D	D
A8	0x08	Meaning	TSHT [1:0]		Mask_DPM	Reserved	ISETA [3:0]			
		Default	0	0	0	1	0	1	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Reset Condition	D	D	D	D	D	D	D	D
A9	0x09	Meaning	$\overline{\text{JEITA}}$	VSETH	VSETC	ISETH	ISETC	Reserved	INT	DPM
		Default	0	0	1	1	0	1	0	0
		Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
		Reset Condition	D	D	D	D	D	D	E	D
A10	0x0A	Meaning	TS_METER [2:0]			NoBAT	EOC	PGOOD	THR	$\overline{\text{SAFE}}$
		Default	0	0	0	0	0	0	0	0
		Read/ Write	R	R	R	R	R	R	R	R
		Reset Condition	I	I	I	I	J	J	J	J
A11	0x0B	Meaning	CHG_TYP [2:0]			Reserved	Reserved	CHG_ 2DET	CHG_ 1DET	CHGRUN
		Default	0	0	0	x	x	0	1	0
		Read/ Write	R	R	R	--	--	R/W	R/W	R
		Reset Condition	K	K	K	G	G	F	F	L

I^2C register reset condition :

A. In addition to A0.bit1 and A0.bit4, the bits of A0 and A1 (register 0x0, 0x1) reset only when (VRTC < 1.6V).

B. The bits of A2 (register 0x2) and A4.bit3 reset when (EN pin=low) or (VDDI < 2.4V) or (BAT < 1.3V) or (Temperature > 125°C).

C. In addition to A4.bit3, PMU settings (A3 to A6, register 0x3 to 0x6) reset when (EN pin = low and A0.RST_P = 1) or (VDDI < 1.3V)

VDDI < 1.3V	EN pin	A0.RST_P bit	==>	Reset PMU Setting
TRUE	x	x (don't care)		Reset
False (VDDI > 1.3V)	Low	1		Reset
	High	1		Not reset
	Low	0		Not reset
	High	0		Not reset

D. In addition to A9.bit1, Charger settings A7 to A9, registers (0x7 to 0x9) and A0.bit4 reset when ((VIN < 3.3V) and (EN pin = Low)) or ((BAT < 2.7V) and (A0.RST_C = 1))

EN Pin	VIN > 3.3V	A0.RST_C bit	(BAT < 2.7V)	==>	Reset Charger Setting
Low	False (VIN < 3.3V)	x	x		Reset
x	x	1	True		Reset
x	True	x	False (BAT > 2.7V)		Not reset
High	x	x	False (BAT > 2.7V)		Not reset
x	True	0	x		Not reset
High	x	0	x		Not reset

E. (EN pin = low) or (VDDI < 1.3V)

F. Charger type detection A11 (registers 0xB) reset when (VIN < 3.3V) or (VDDI < 1.3V)

G. Always reset.

H. A0.bit1 will be reset when (EN pin = low) or (VDDI < 2.4V) or (BAT < 1.3V) or (PMU protection occur) or (Temperature < 125°C).

I. A0.bit1 will be reset when (EN pin = low) or (VDDI < 2.4V) or (BAT < 1.3V) or (In addition to CH7 OVP, PMU protection occur) or (Temperature <125°C).

J. Reference A10 explanation.

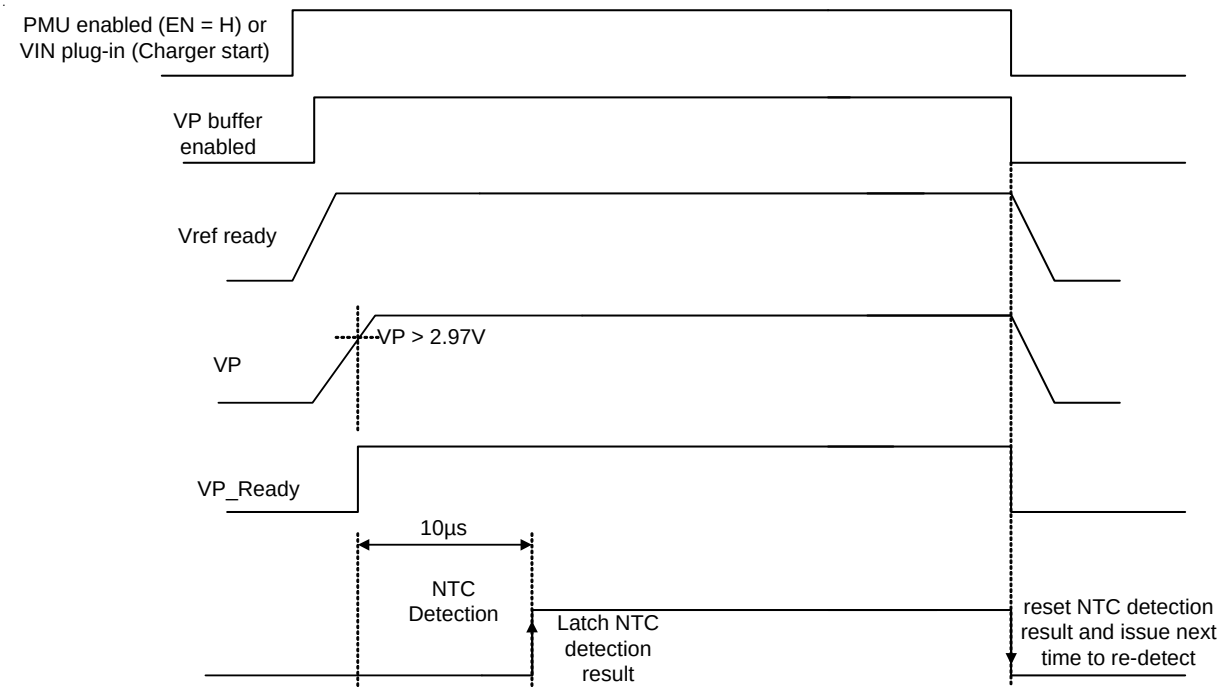
K. A11.bit7 to bit5 will be rewritten after charging type detects finish.

L. A11.bit0 keeps high during charging type detecting.

$\overline{\text{CHG}}$ Signal Status

Charging Status	CHGST = 0 ($\overline{\text{CHG}}$ Output H/L)	CHGST = 1 ($\overline{\text{CHG}}$ Output Flicker)
No Charging/ Charging Finish	in high impedance (no flashing)	in high impedance (no flashing)
Pre-Charge/Fast Charge	Low	0.5Hz (2s)
Abnormal (fault timer timeout, in thermal regulation, battery too cold or too hot)	4Hz (0.25s)	4Hz (0.25s)

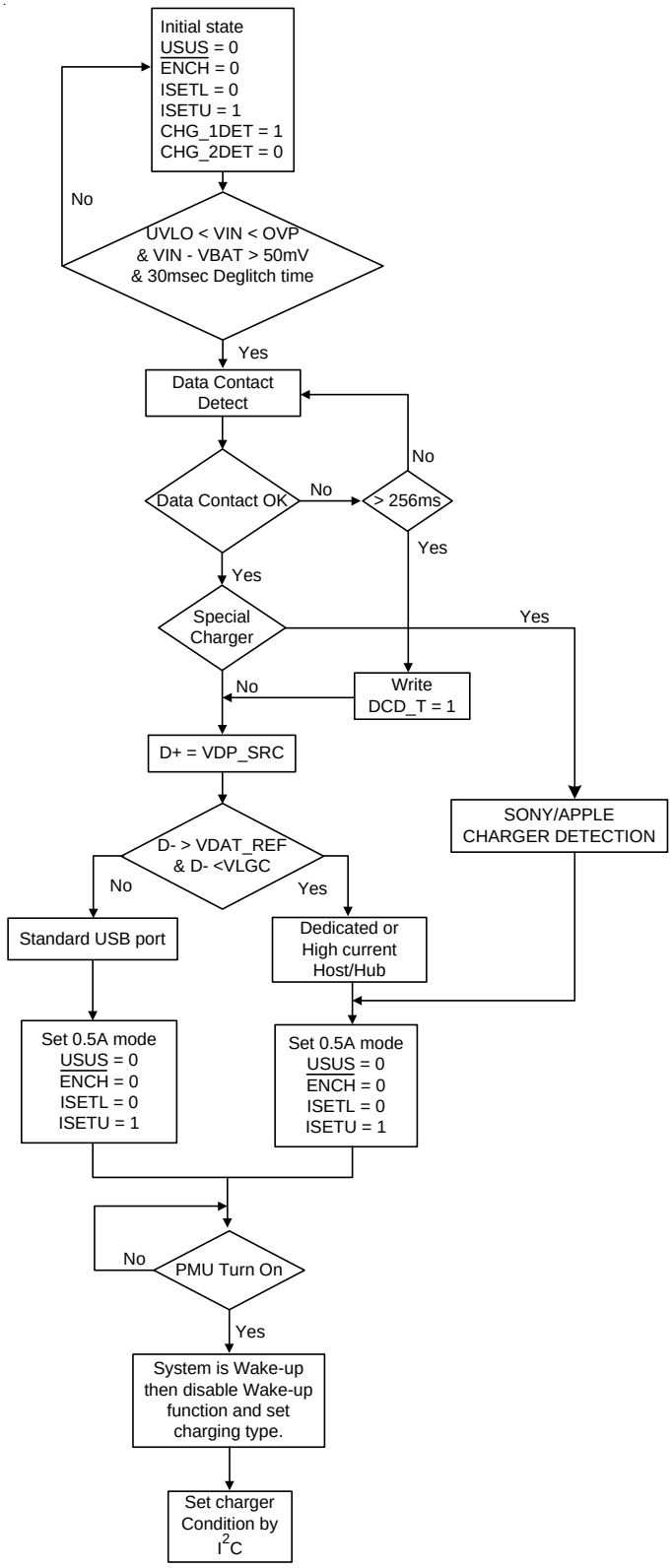
NTC Thermistor Order Detection



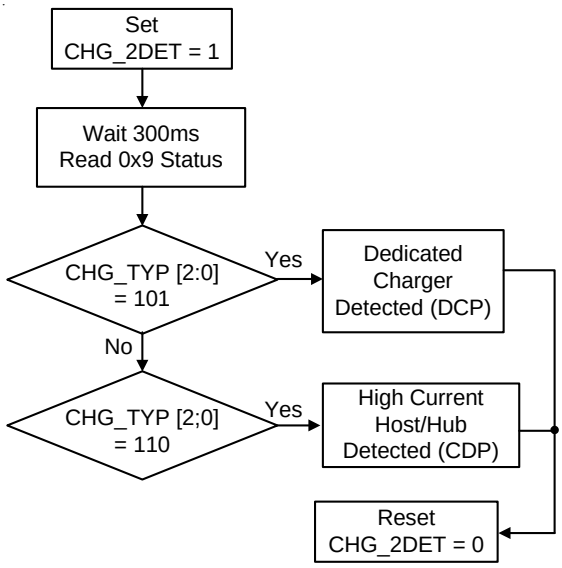
USB Charger Detection

Primary Charger Type Detection (CHG_1DET) : Detection Time ≤ 200ms

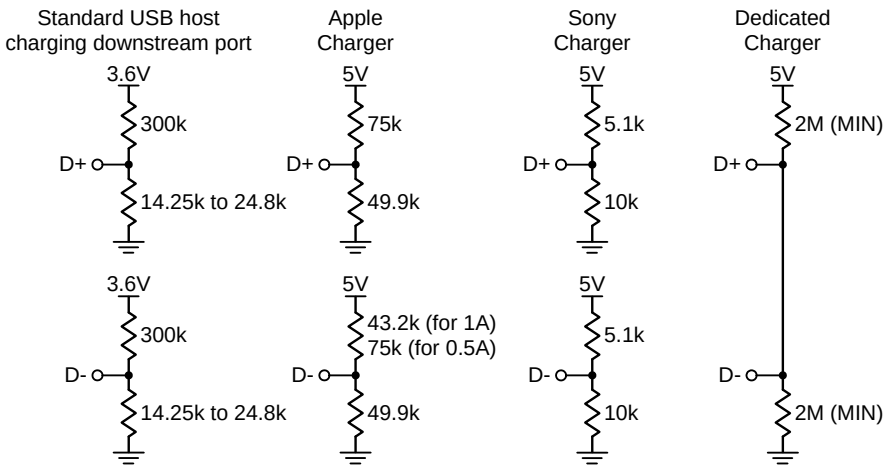
Note : VSYS loading must less than 90mA when w/o battery or VBAT voltage < 2.7V in the situation.



Secondary Charger Type Detection (CHG_2DET)



D+/D– impedance of Standard USB Host/Charging Downstream Port, Apple Charger, Sony Charger, and Dedicated Charger:



Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.64W for WQFN-40L 5x5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

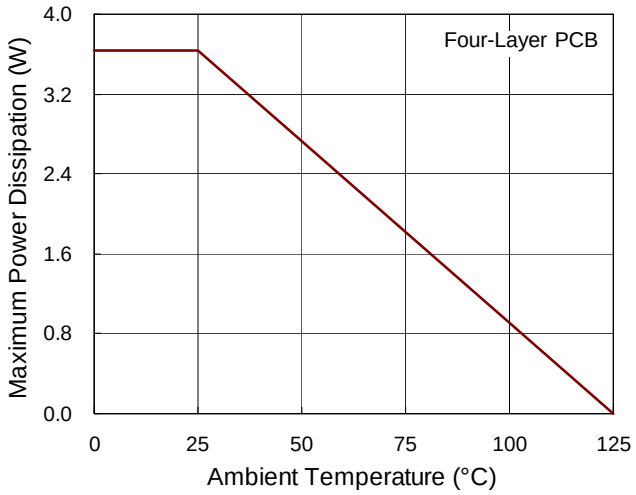


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT5024, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- To make CH1 and whole chip stable, the power path from the pin PVD1 to its output capacitors must be as short (≤ 1mm is better) and wide as possible.

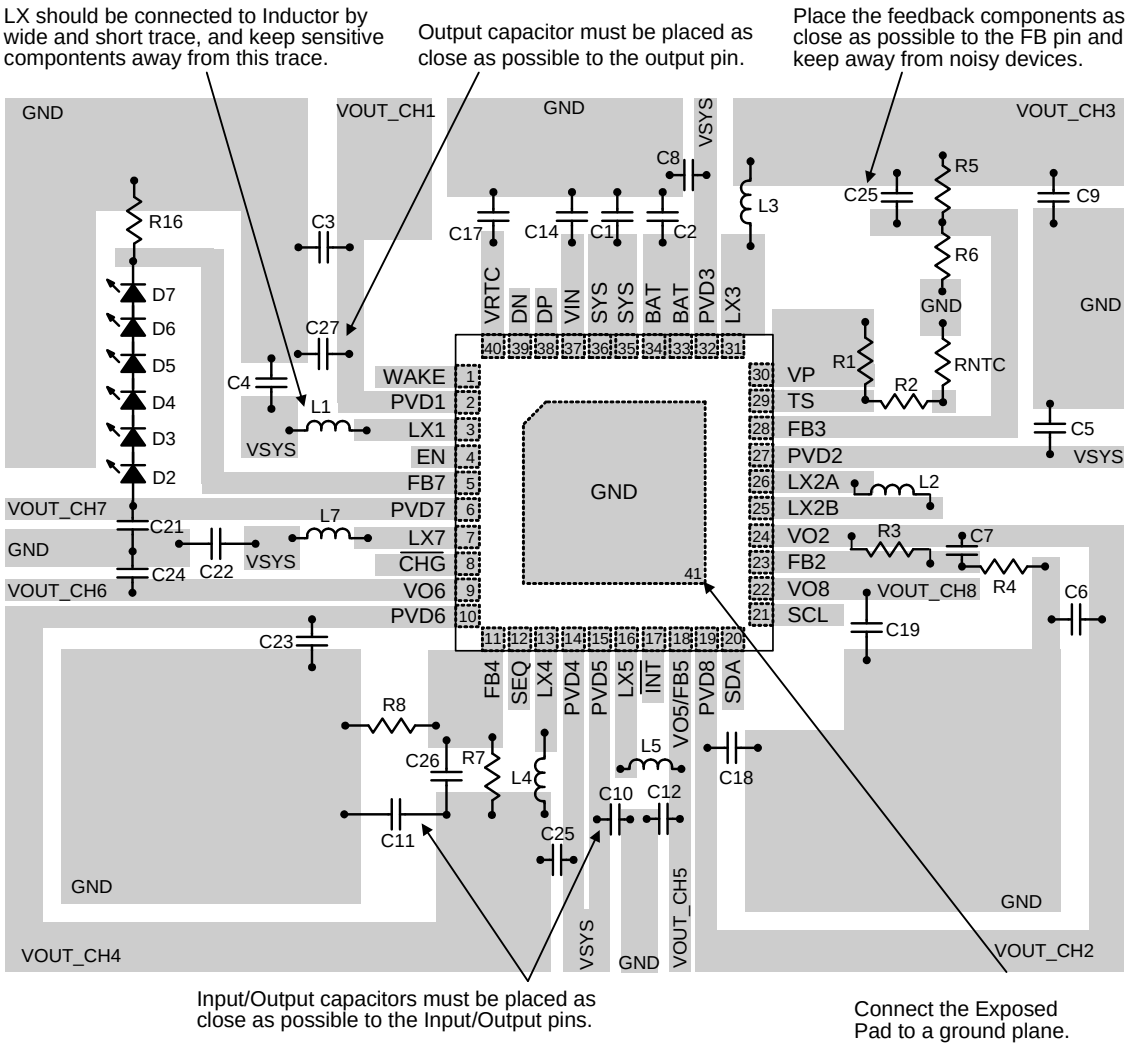
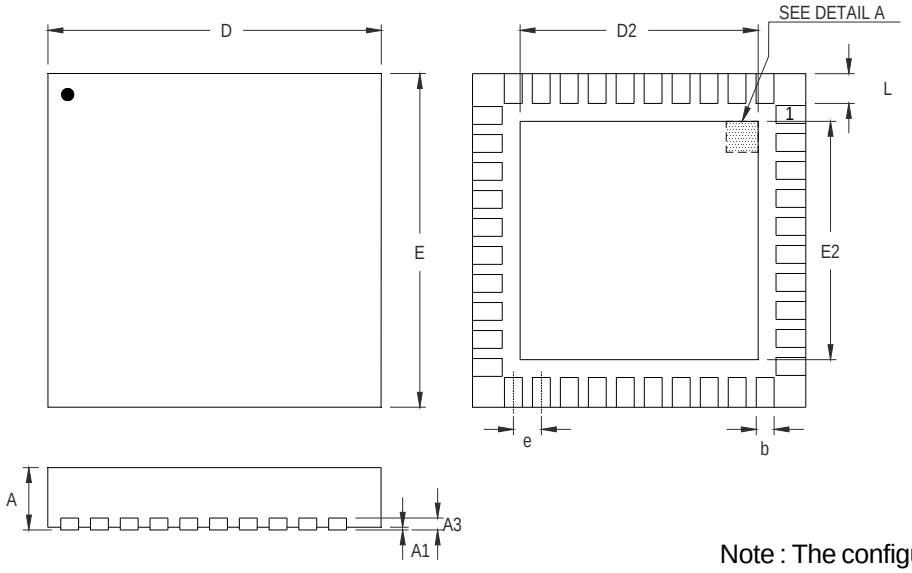


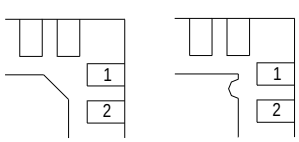
Figure 7. PCB Layout Guide

	Protection Type	Threshold (Typical) Refer to Electrical Spec.	Protection Methods	PMU Shutdown Delay Time	Reset Method
SYS	UVLO	SYS < 1.5V	PMU Shutdown.	No-delay	EN1234 pin set to low or SYS > 2.1V
VDDI	OVP	VDDM > 6V	Automatic reset at VDDM < 5.85V	100ms	VDDI power reset or EN1234 pin set to low
	UVLO	VDDM < 2.4V	PMU Shutdown.	No-delay	VDDI power reset or EN1234 pin set to low
CH1 Step-Up	Current Limit	N-MOSFET peak current > 3A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	PVD1 OVP	PVDD1 > 6V	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	PVD1 UVP --1	PVDD1 < (VSYS – 0.8V) or PVDD1 < 1.28V after soft-start end.	N-MOSFET off, P-MOSFET off.	100ms	VDDI power reset or EN1234 pin set to low
	PVD1 UVP --2	After pre-charge (PVD1 UVP-2 : FB1 < 0.4V after pre-charge)	N-MOSFET off, P-MOSFET off	No-delay	VDDI power reset or EN1234 pin set to low
	PVD1 Over Load (OL)	Target – 0.6V Target Voltage is defined in A4.VOUT1 [3:0]	PMU Shutdown when OL occur each cycle until 100ms.	100ms	VDDI power reset or EN1234 pin set to low
CH2 Step-Up/Down	Current limit	Both P-MOSFET (PVD2 – LX2A) and N-MOSFET (LX2B – GND) peak current > 2A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	VO2 OVP	PVDD1 > 6V	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	FB2 UVP	FB2 < 0.4V after soft-start end.	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	FB2 Over Load	Target – 0.1V (Target voltage is the chosen one in A4.FB2 [2:0])	PMU Shutdown when OL occur each cycle until 100ms.	100ms	VDDI power reset or EN1234 pin set to low
CH3 Step-Down	Current limit	P-MOSFET peak current > 1.8A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	FB3 UVP	FB3 < 0.4V after soft-start end.	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	FB3 Over Load	Target – 0.1V (Target voltage is the chosen one in A5.FB3 [2:0])	PMU Shutdown when OL occur each cycle until 100ms.	100ms	VDDI power reset or EN1234 pin set to low

	Protection Type	Threshold (Typical) Refer to Electrical Spec.	Protection Methods	PMU Shutdown Delay Time	Reset Method
CH4 Step-Down	Current limit	P-MOSFET peak current > 1.8A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	FB4 UVP	FB4 < 0.4V after soft-start end.	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	FB4 Over Load	Target – 0.1V (Target voltage is the chosen one in A5.FB4 [2:0])	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDI power reset or EN1234 pin set to low
CH5 Step-Down	Current limit	P-MOSFET peak current > 1.5A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	VO5 UVP	PVD5 UVP : FB5 < 0.4V after soft-start end	N-MOSFET off, P-MOSFET off.	No-delay	VDDI power reset or EN1234 pin set to low
	VO5 Over Load	Target voltage is the chosen one in A6.VOUT5 [3:0] = 0000 (FB5 = 0.8V)	PMU Shutdown when OL occur each cycle until 100mS.	100ms	VDDI power reset or EN1234 pin set to low
		Target voltage is the chosen one in A6.VOUT5 [3:0] = 0001 to 0111			
		Target voltage is the chosen one in A6.VOUT5 [3:0] = 0111 to 1111			
CH6 LDO	Max. output current (current limit)	P-MOSFET current > 0.55A (PVD6 = 1.5V, VO6 = 1.3V)	P-MOSFET off.	100ms	VDDI power reset or EN1234 pin set to low
CH7 WLED	Current limit (Step-Up mode)	N-MOSFET current > 0.8A	N-MOSFET off, P-MOSFET off. Automatic reset at next clock cycle.	100ms	VDDI power reset or EN1234 pin set to low
	PVDD7 OVP	PVDD7 > 16V (A0.OVP7 = 0)	N-MOSFET off, P-MOSFET off. Shutdown CH7 by self	No-delay	VDDI power reset and A2.EN7_DIM7 [4:0] reset or EN1234 pin set to low
		PVDD7 > 25V (A0.OVP7 = 1)			
CH8 LDO	Max. output current (current limit)	P-MOSFET current > 0.45A (PVD6 = 3V, VO6 = 2.5V)	P-MOSFET off.	100ms	VDDI power reset or EN1234 pin set to low
Thermal	Thermal shutdown	Temperature > 155°C	All channels stop switching	No-delay	Temperature < (155 – 20)°C
VIN	VIN UVLO	VIN < 3.3V	No-charge	No-delay	No latch
	VIN OVP	VIN > 6.5V	No-charge	No-delay	No latch

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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