LUX13HS

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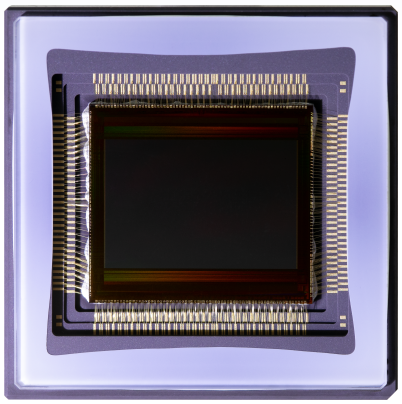

The LUXIMA™ LUX13HS image sensor is a 1.0 Megapixel 3,500+ Fps Global Shutter CMOS Digital Sensor developed for the high speed machine vision, 3D scanning, motion analysis, and industrial markets. LUX13HS features low noise pixel with CDS based on the patented Floating Storage Gate technology.

Optical format	4/3”
Active resolution	1280 x 864 pixels
Pixel	13.7 um pitch 7T shutter pixel with CDS
Full well/ Read Noise	20,000e-/ 14e-
Responsivity	25V/Lux-s @ 550nm
QE	>45% @ 550nm
Conversion gain	75 uV/e-
DSNU	4 mV r.m.s.
PRNU	<1.5% rms
Shutter efficiency	99.9%
Nominal Frame Rate	3500 Frames/s @ 1280 x 864 4,000 @720p 9,000 Frames/s @1184 x 384
Column Parallel ADC	10b
Data Output	80 LVDS ports @540MHz for 10-b output 64 LVDS ports for 8-b output
Multiplexed Output option	YES, 2:1 (40 LVDS ports @10b @ 2,500 Fps max)
Windowing	Y random access in quanta of 4 rows; X min = 1184 columns, smaller Xwin by data skip
Nominal clock rate	133 MHz
Power supply	3.3V Analog, 1.8V digital
Power consumption	2W @ 3500Fps full resolution
Package	352-pin uPGA, 36mm size 344-pin uPGA, 30mm size 236-pin uPGA 30mm; Multiplexed Output
Color Filter	RGB or Mono

REVISION HISTORY

Date	Revision	Comments
04.12.14	1.0	First draft; conversion from ICD V2.6
12.18.14	2.0.	The specs is updated based on the sensor Rev.2. measurements
		Typos found are fixed throughout the text
		Serialization table for Reduced mode is corrected (right pins) pg.38
01.14.15	2.1.	Sensor orientation is added to package description. Few typos fixed

INTRODUCTION.

LUX13HS is the 3rd generation 1 Mpix High Speed Digital CMOS image sensor.

Compared to the previous generation, LUX13HS has the following improvements:

- Low noise pixel
- Low noise LVDS drivers

The block diagram of the LUX13HS sensor is drawn in Fig.1.

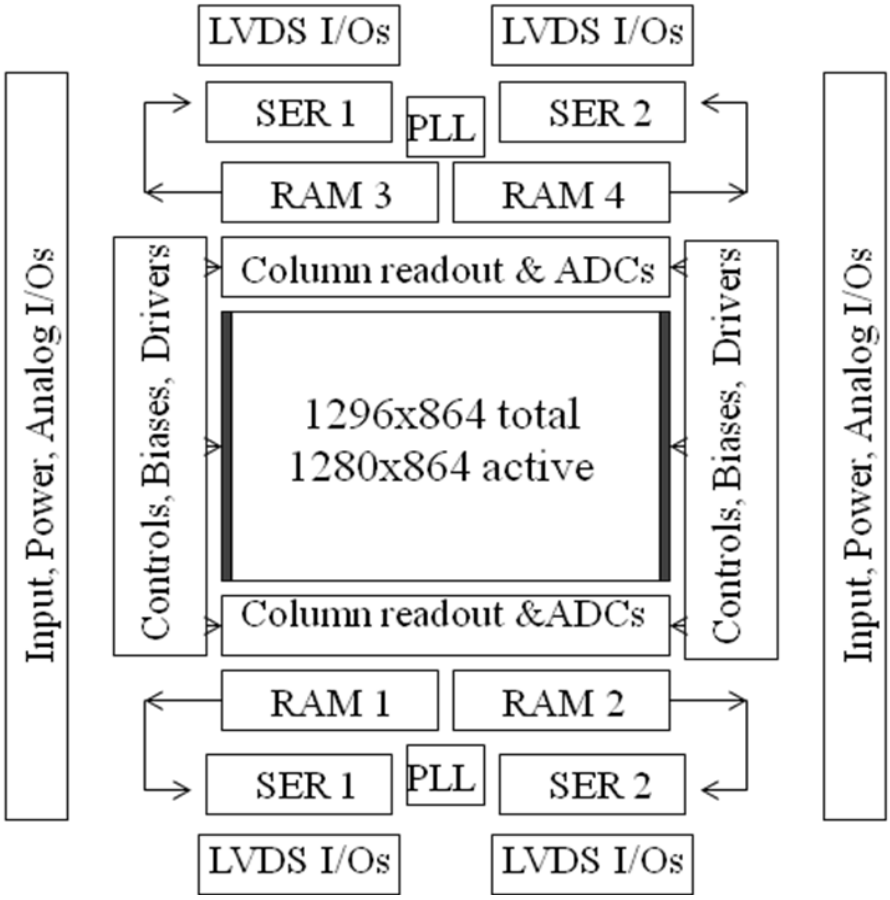

Fig.1.0. LUX13HS Sensor block diagram.

The sensor has two column readout blocks (on top and in the bottom) which include per-column sample circuits, amplifier circuits, and ADCs with readable SAR (successive-approximation) registers, where the ADC data is temporarily stored for readout. The readout from the SAR registers as well as the sensor controls are arranged as a 4 quadrant readout & control architecture, which allows local control over SAR ADCs and local data readout, both essential for high speed operation of the sensor. The sensor also has some biases and all current sources

generated internally. Although, many critical voltages to this chip are required to be generated externally.

2.0. PIXEL ARRAY.

There are total of 1296x864 pixels. The active resolution is 1280x864. Of 8 dark columns on each side, the first revision of the sensor has 7 true dark columns and 1 "grey" boundary columns which improve image iniformity in Active area.

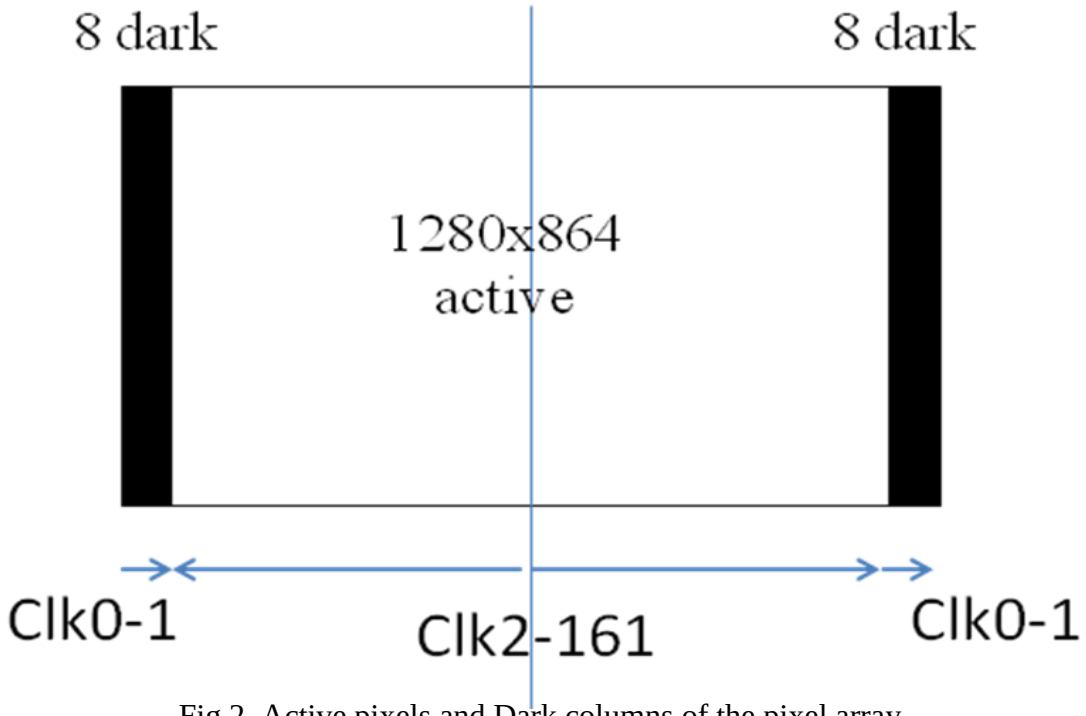

Fig.2. Active pixels and Dark columns of the pixel array.

The order of reading bi-lines: First go the dark columns on the left and the right, then the column decoder jumps to the middle of the pixel array and reads columns 647 to 8 on the left side, and 648 to 1287 on the right side.

3.0. PIXEL AND GLOBAL SHUTTER CONTROLS.

Pixel is a 7T (seven transistor) Storage Gate shutter pixel with diagram shown in Fig.3.
The diagram explains the need for four controls *PRST_n, TX_n, TX2_n, and PD_n* to operate the global shutter. The controls work as follows:

- *'PD_n'* (applied to AB gate). When low, erases the photo-charge in photodiode. When high, allows for exposure. Default state is High.
- *'TX_n'* (transfer pulse) *("low")* make the transfer of charge from the photodetector PD to the storage gate SG. Default state is High.
- *'TX2_n'* (second transfer control) *("low")* removes the charge from the storage gate SG. Default state is High.

- *'PRST_n' ("low")* resets the pixel memories SG. Unless specified differently, always stays Low.

So, if one needs to clear the entire pixel, such as in case of after a long pause, PD_n, TX_n, and TX2_n are made LOW, and the pixel cleared of the accumulated dark current charge.

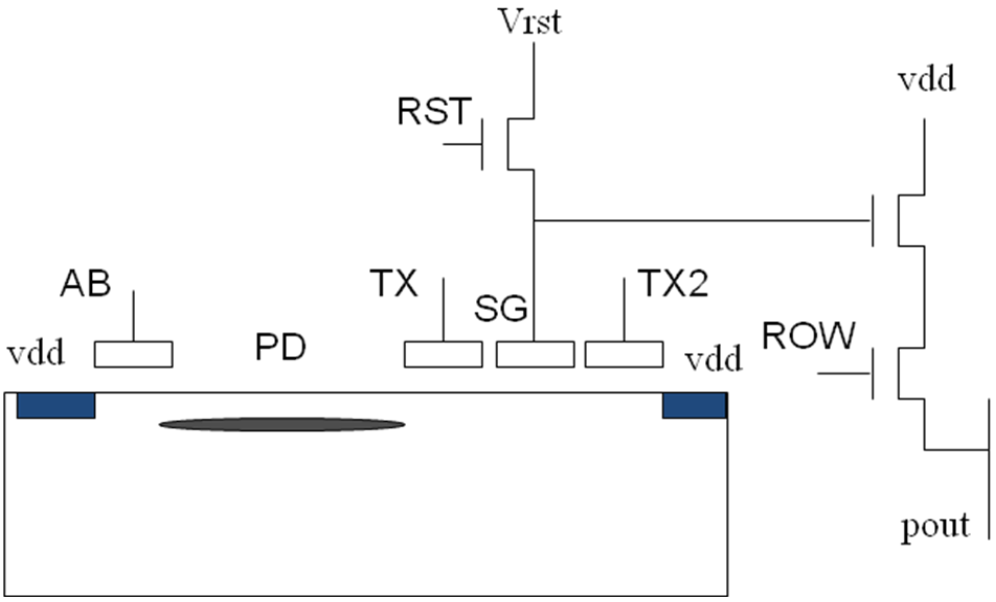

Fig.3. Simplified Diagram of the Shutter Pixel

During the signal readout from the pixel the sensor control block generate an internal sequence of pulses. These operations include the reset of the pixel, reading out the signal corresponding to the pixel reset, and reading out of the second signal stored at SG node. This operation is a true correlated double sampling, and it removes most of the pixel reset KTC noise.

4.0. TIMING IN CONTINUOUS MODE.

Sensor controls assume an external row addressing (row0- row8) using a simple binary encoding. The sensor uses a speed-up technique and reads two rows of the pixel data at a time. One bit increment of the Row address increments the row count by 2. The valid row addresses are 0 through 431.

To read from the selected bi- line of pixels and perform A-to-D over pixel signals, one needs to send a Start Row control "st_row_n". Reading out the pixel bi-line and the digitization take 150-152 clock cycles.

After the digitization of the pixel signals from the first bi-line, one may send the control Start Read ("st_read_n") to read the digital data out. Reading data out takes 160 clocks plus 2-4 clocks filling the horizontal blank time.

LUX13HS has the ability to read the same columns of the pixels through either top or bottom readout. While top readout samples signals from the selected two rows, the bottom readout may perform ADC conversion, and vice versa. This achieves the maximum data throughput from the sensor. So, there are two Start_row controls, one for the bottom sampling one for the top, and there are two Start_read controls, one for the top and one for the bottom. One bit increment of the Row dress increments the row count by 2. The valid row addresses are 0 through 431. The row address 0 reads physical rows 0 and 1, The row address 1 reads rows 2 and 3. In the diagram below, are real physical rows:

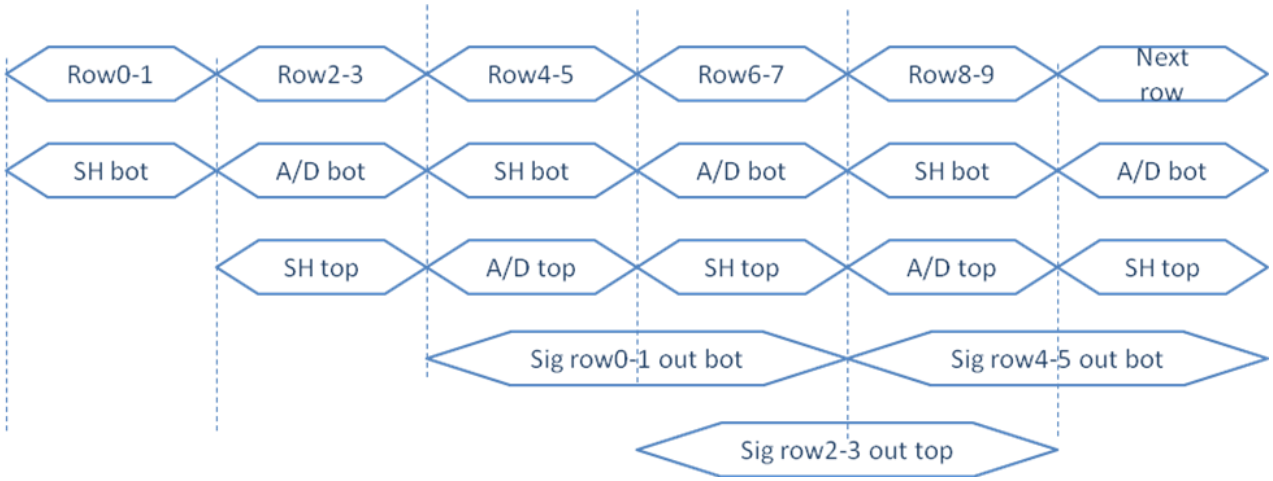

Fig.4. Pipelined readout top-bottom allowing 100% pixel sampling efficiency.

One SH operation lasts 78 clocks, one A/D operation lasts 72 clocks. One data readout lasts 162 clocks. A short 1 clock pause is then needed between two data reads from one sensor side (top/bot). The recommended minimum row time is 164 clocks. Because the row operations are shorter than the data read, the customer may crop the image (Bit 8 of the register) and reduce the row time to the minimum of 156 clock cycles. The cropped image resolution will be 1224x768.

The readout rolls row after row, and these two controls present in all rows except for the first one (when Start Read is not needed; no ADC data yet) and the last one (when another Start Row is no longer needed, but Start Read still needs to be applied to read out the ADC data from the last row).

An example of the frame timing with an exemplar global shutter controls is drawn in Fig.5. After selecting new double row for pixel read, we suggest to allocate 2 clocks for row address to settle (The Reduced interface mode may require 4 clock long pulse as the sensor core clock get divided by two), and then apply Start_row_bot_n pulse. This will read the pixels in the selected double row to the bottom ADCs. In the middle of the first line time, the address is changed, and while the bottom ADCs perform A-D conversion, another double line of the image is sampled

into the Top ADCs. The architecture does not have the preference if the odd or Even rows needs to be sampled particularly to the Top or the Bottom. Anyway, we allow for some difference in performance may occur, so this rule needs to be determined experimentally. Start_read_top/bot pulses followed after corresponding ADC conversion is completed. The window for Start_read is up to the middle of the next row, when the next ADC data start being written into ADC memory and the current data is erased. So, the delay of Start_read to the corresponding Start_row is ~160-244 clock cycles and could be optimized for the best performance.

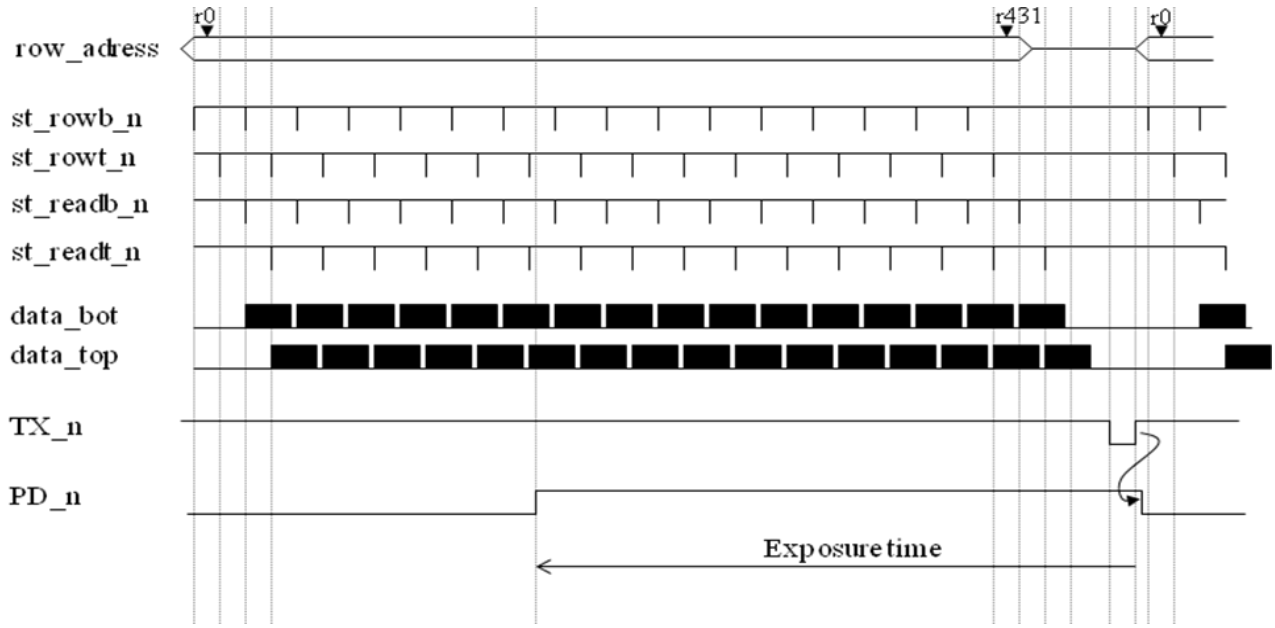

Fig.5. An example of one frame timing in continuous operation

The charge transfer is accomplished with *TX_n* low. Optional TX2_n pulse before TX_n can be tried to additionally clear the pixel memories before the readout. The abovementioned pixel memories are also cleared during the readout process. To start the exposure PD_n is brought High. The High state shall overlap the TX_n transfer pulse. If the shutter line associated with the line where PD_n is changed is visible, the position of PD_n inside the row need to be adjusted. If the shutter line is observed in the "change" frame, when exposure changes and the PD_edges moves, then we recommend to implement a "pulse-train" of PD_n going Low each line where PD_n is supposed to be Low.

This timing diagram is designed for continuous sensor operation when the exposure overlaps with the readout, and the exposures is less than the frame time.

The detailed example of the timing of one row (top readout) is shown in Fig.6. The minimum row width in terms of the clock number is defined by data read operation. All data is read out in 162 clocks. We leave 2 more clocks for row overhead time (Read state machine). So the minimum recommended row time is 164 clocks. Based on noise reduction requirement (if any) this time may be elongated.

We recommend to set up row address at least 3 clocks prior to sending Start_row_n command (a one-clock LOW pulse) and keep the row address at least for 76 clocks since the Start_row_n. During this time, signals from the pixels are read down into the column ADCs.

Keeping the row address until 3 clocks before the next Start_row_n eliminates static horizontal lines on the left and on the right. This timing is recommended for Global Shutter Operation.

Reading out the digital data of one row from the sensor is initiated with Start_read_n command (one-clock* LOW pulse). In the prototype chip (AM41) we recommended to send Start_read_n at 18th clock after Start_row_n. This shall be optimized for LUX13HS sensor.

There is a latency between Start_read and Data out from the first row. The latency is 3-4 clock internal readout delay.

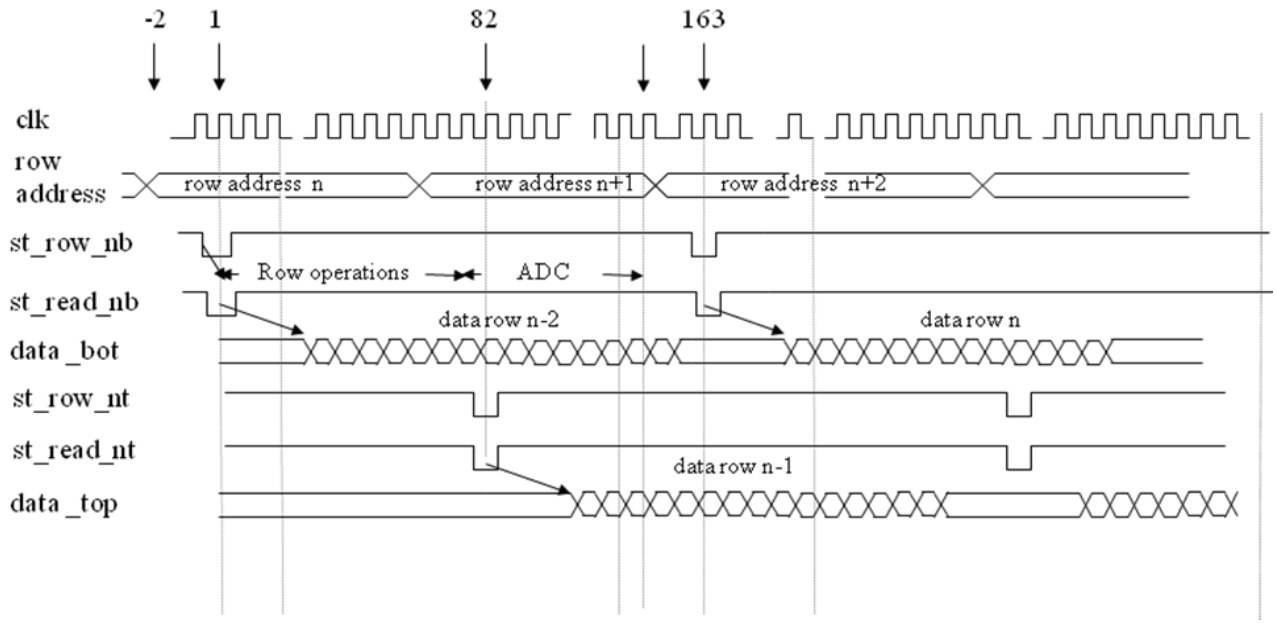

Fig.6. Example of the timing of one row (top readout).

Output data starts with 16 dark columns on the left and 16 dark column on the right. Then the column decoder jumps to the sensor center and the columns are read from the center to the left (left ports and to the right (right ports).

5.0. SENSOR CONTROLS.

5.1. Overview

There are four sensor control blocks in the four corners of the chip. The two upper control blocks serve the upper readout, the two bottom control blocks serve the bottom readout. The upper internal controls are somewhat autonomous from the bottom controls. Small timing misalignment between the top and the bottom internal control pulses shall not cause any conflict of drivers. But, there shall be good symmetry of operation between the left and the right

controllers. To facilitate this symmetry, the chip master clock is split into the *MCLKB* and *MCLKT* serving the top and the bottom of the chip, respectively. Also, the clock pads are placed in the middle of the pad ring to built a clock tree which is left-right symmetrical.

Row driver is placed on both lift and right sides of the chip, the global shutter controls are registered so they normally arrive at the same time to the row driver. However, if setup time is very short, it may happen that the left and the right control will be sampled by different clocks which **may cause the appearance of random broken lines in the image**.

Serial interface commands and the clock experience long internal delays. These controls use weak drivers over long distances. The clock frequency is recommended to be at least 1/10 of the master clock frequency.

Master Clock. ***MCLKT*** *and* ***MCLKB*** are 130 (with PLL) and 260 MHz (w/o PLL) for ~4000 Frames/s and 160 MHz/320 MHz for ~5000 Frames/s operation. Duration +-5% in the second case. **It is desirable that the clock to the bottom is synchronous to the top clock.**

5.2. Setup and hold time for essential controls

Definition of setup/hold time is in Fig.4

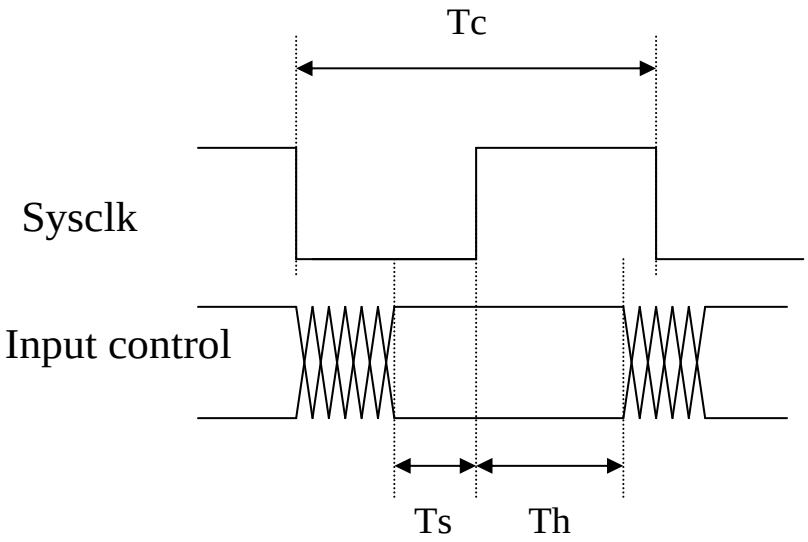

Fig.8.

For input controls st_row_n, st_read_n, use the following table

	Min	Typical	Max
Setup time Ts	5 ns		Tc- 0.5 ns
Hold time Th	0 ns	0.5 ns	

Since the recommended setup time is of the order of Tc/2, the standard choice of using the falling edge of the clock to start a control pulse may be problematic for these two controls. Rising edge plus some natural gate delay may work better.

The parameters of Lrst_n, Standby_n, are not critical.

The requirements to the timing of the serial interface are considered later.

6.0. DIGITAL I/O PADS ABSOLUTE RATINGS.

LUX13HS is **operated from 1.8V digital power supply and 3.3V analog power supply.**

The pads have the following ratings:

	Operating condition	Min	Typ	Max
VDDIO	I/O Power, operating ratings	1.7V	1.8V	2.5V
VDDIO	I/O Power, absolute maximum ratings	-0.3V		2.5V
	Input digital I/O pads, logic LOW level	-0.3V	0V	+0.5V
	Input digital I/O pads, logic HIGH level	1.6V	1.8V	+2.5V
	Input digital I/O pads, absolute maximum ratings	-0.3V		+3.3V
VDDK	Digital Core Power	1.7V	1.8V	2.2V
VDDLV	LVDS Power	1.7V	1.8V	2.0V
PLL_VDD	PLL POWER	1.7V	1.8V	2.0V
VCC_L	Quiet Digital Power for LVDS biases	1.7V	1.8V	2.2V
VAA	Analog Power	3.0V	3.3V	3.6V
VDD3V	Analog Driver Power	3.0V	3.3V	3.6V

The power supply requirements are summarized in the following tables:

Source/sink		Voltage	Current requirement (mA)	Noise requirement (mVp-p)
VDDIO/VSSIO	I/O Power, operating ratings	1.8V /0V	<100	200
VDDK/GNDK	Digital Core Power	1.8V /0V	<300	50
VDDLV/ VSSLV	Output LVDS Driver Power	1.8V /0V	<500	50
PLL_(VDD/GND)	PLL POWER	1.8V /0V	<20	50
VCC_L /VSS_L	Quiet Digital Power for LVDS biases	1.8V /0V	<10	10
VAA /AGND	Analog Power	3.3V	<400	10
VDD3V /GNDA	Analog Driver Power	3.3V	<100	25

7.0. PIN LIST FOR 1.27mm 361-pin uPGA (with 3x3 Index Pin).

Sensor pad	Package pin	Name	Comment
1	Y26	VSSLV	LVDS ground
2	X24	VDDLV	LVDS power 1.8V
3	X26	GNDK	Digital Core ground
4	X25	VDDK	Digital Core power
5	W25	VAD4	Second ADC voltage (=VADH/4)
6	W24	VOFF	ADC offset voltage 0-1.2V
7	W23	AGND	Analog ground
8	V23	VAA	Analog power 3.3V
9	W26	VADL	ADC Reference Low = connect to AGND
10	V24	VADH	ADC Reference High 0.8V (0.2V-1V)
11	V25	AGND	Analog ground
12	V26	VAA	Analog power 3.3V
13	U23	GNDA	Analog Driver ground, connect to AGND
14	U24	VDD3V	Analog Driver power 3.3V, connect to VAA
15	U26	VRSTH	Pixel Reset High voltage 3.4V (2.5V-4.0V)
16	U25	VPIX	Pixel Reset Voltage 1.2V (1.0V-3.6V)
17	T26	VTXH	Pixel Transfer High Voltage 3.3V (2.2V-3.6V)
18	Y24	VTX2L	Pixel Second transfer Low (-0.3 : +0.5V)
19	T25	VTXL	Transfer gate Low (-0.3 : +0.5V)
20	T24	VABL_TST	Pixel AntiBlooming Bias (0-0.4V operation, upto 2.5V testing)
21	X23	VLN	Pixel SF Current control bias 0.45V (0.4V-0.6V or floating)
22	Y25	St_read_tn	Start top SRAM read
23	R25	St_row_tn	Start top row read; 2clk minimum active LOW pulse
24	R24	PRST_n	Global Pixel Reset control
25	R26	rad7	Row address bit8
26	T23	rad5	Row address bit6
27	R23	rad3	Row address bit4
28	P23	rad1	Row address bit2
29	P25	lrst_n	Logic reset, asynchronous
30	P24	VDDIO	Digital I/O power 1.8V (1.8V-2.3V)
31	P26	VDDK	Digital Core power 1.8V
32	N23	GNDK	Digital Core ground
33	N25	VSSIO	Digital I/O ground
34	N24	rad0	Row address bit1
35	N26	rad2	Row address bit3

36	M23	rad4	Row address bit5
37	L23	rad6	Row address bit7
38	M24	rad8	Row address bit9
39	M25	TX_n	Global TX control
40	F25	St_row_bn	Start bottom row read; 2clk minimum active LOW pulse
41	F24	St_read_bn	Start bottom SRAM read
42	L25	VLN	Pixel SF Current control bias 0.45V (0.4V-0.6V) (=VLN)
43	M26	VABL_TST	Pixel AntiBlooming Bias
44	L24	VTXL	Transfer gate Low (-0.3 : +0.5V)
45	L26	VTX2L	Pixel Second transfer Low
46	K23	VTXH	Pixel Transfer High Voltage 3.3V
47	K26	VPIX	Pixel Reset Voltage
48	K24	VRSTH	Pixel Reset High voltage
49	K25	VDD3V	Analog Driver power 3.3V
50	J23	GNDA	Analog Driver ground 0V
51	J26	VAA	Analog Power 3.3V
52	J25	AGND	Analog ground
53	H23	VADH	ADC Reference High 0.8V (0.2V-1V)
54	J24	VADL	ADC Reference Low = connect to AGND
55	H26	VAA	Analog Power 3.3V
56	G23	AGND	Analog ground
57	H25	VOFF	ADC offset voltage 0-1.2V (=VOFF)
58	H24	VAD4	Second ADC voltage (=VADH/4)
59	G26	VDDK	Digital Core power 1.8V
60	G25	GNDK	Digital Core ground
61	F26	VDDLV	LVDS power 1.8V
62	G24	VSSLV	LVDS ground
63	E22	VSSLV	LVDS ground
64	F20	CHP0	LVDS out 0 positive
65	F21	CHN0	LVDS out 0 negative
66	F22	CHP1	LVDS out 1 positive
67	F23	CHN1	LVDS out 1 negative
68	D22	CHP2	LVDS out 2 positive
69	C22	CHN2	LVDS out 2 negative
70	E23	CHP3	LVDS out 3 positive
71	D23	CHN3	LVDS out 3 negative
72	E20	VDDLV	LVDS power 1.8V
73	E21	VSSLV	LVDS ground
74	D21	CHP4	LVDS out 4 positive
75	C21	CHN4	LVDS out 4 negative

76	A22	CHP5	LVDS out 5 positive
77	B22	CHN5	LVDS out 5 negative
78	D20	CHP6	LVDS out 6 positive
79	C20	CHN6	LVDS out 6 negative
80	A21	CHP7	LVDS out 7 positive
81	B21	CHN7	LVDS out 7 negative
82	E19	VDDLV	LVDS power 1.8V
83	F19	VSSLV	LVDS ground
84	D19	CHP8	LVDS out 8 positive
85	C19	CHN8	LVDS out 8 negative
86	A20	CHP9	LVDS out 9 positive
87	B20	CHN9	LVDS out 9 negative
88	C18	CHP10	LVDS out 10 positive
89	D18	CHN10	LVDS out 10 negative
90	A19	CHP11	LVDS out 11 positive
91	B19	CHN11	LVDS out 11 negative
92	E18	VDDLV	LVDS power 1.8V
93	E17	VSSLV	LVDS ground
94	C17	CHP12	LVDS out 12 positive
95	D17	CHN12	LVDS out 12 negative
96	A18	CHP13	LVDS out 13 positive
97	B18	CHN13	LVDS out 13 negative
98	C16	CHP14	LVDS out 14 positive
99	D16	CHN14	LVDS out 14 negative
100	A17	CHP15	LVDS out 15 positive
101	B17	CHN15	LVDS out 15 negative
102	F18	VDDLV	LVDS power 1.8V
103	E16	VSSLV	LVDS ground
104	C15	CHP16	LVDS out 16 positive
105	D15	CHN16	LVDS out 16 negative
106	A16	CHP17	LVDS out 17 positive
107	B16	CHN17	LVDS out 17 negative
108	E15	CHP18	LVDS out 18 positive
109	F15	CHN18	LVDS out 18 negative
110	A15	CHP19	LVDS out 19 positive
111	B15	CHN19	LVDS out 19 negative
112	F17	VDDLV	LVDS power 1.8V
113	A14	PCLKP	LVDS clock out positive for outputs 0-19
114	B14	PCLKN	LVDS clock out negative for outputs 0-19
115	F16	VSSLV	LVDS ground
116	D14	VSS_L	LVDS quiet bias ground

117	C14	VCC_L	LVDS quiet bias power 1.8V
118	F14	PLL_GND	PLL ground
119	E14	MCLKB	Master clock bottom
120	E13	SYNCB	Sync pulse bot for clock divide/2
121	F13	PLL_VDD	PLL power 1.8V
122	C13	VCC_L	LVDS quiet bias power 1.8V
123	D13	VSS_L	LVDS quiet bias ground
124	F11	VDDLV	LVDS power 1.8V
125	B13	DCLKP	LVDS clock out positive for outputs 20-39
126	A13	DCLKN	LVDS clock out negative for outputs 20-39
127	F10	VSSLV	LVDS ground
128	F12	CHP20	LVDS out 20 positive
129	E12	CHN20	LVDS out 20 negative
130	B12	CHP21	LVDS out 21 positive
131	A12	CHN21	LVDS out 21 negative
132	D12	CHP22	LVDS out 22 positive
133	C12	CHN22	LVDS out 22 negative
134	B11	CHP23	LVDS out 23 positive
135	A11	CHN23	LVDS out 23 negative
136	E11	VDDLV	LVDS power 1.8V
137	E10	VSSLV	LVDS ground
138	D11	CHP24	LVDS out 24 positive
139	C11	CHN24	LVDS out 24 negative
140	B10	CHP25	LVDS out 25 positive
141	A10	CHN25	LVDS out 25 negative
142	D10	CHP26	LVDS out 26 positive
143	C10	CHN26	LVDS out 26 negative
144	B9	CHP27	LVDS out 27 positive
145	A9	CHN27	LVDS out 27 negative
146	F9	VDDLV	LVDS power 1.8V
147	E9	VSSLV	LVDS ground
148	D9	CHP28	LVDS out 28 positive
149	C9	CHN28	LVDS out 28 negative
150	B8	CHP29	LVDS out 29 positive
151	A8	CHN29	LVDS out 29 negative
152	C8	CHP30	LVDS out 30 positive
153	D8	CHN30	LVDS out 30 negative
154	B7	CHP31	LVDS out 31 positive
155	A7	CHN31	LVDS out 31 negative
156	F8	VDDLV	LVDS power 1.8V
157	E8	VSSLV	LVDS ground

158	C7	CHP32	LVDS out 32 positive
159	D7	CHN32	LVDS out 32 negative
160	B6	CHP33	LVDS out 33 positive
161	A6	CHN33	LVDS out 33 negative
162	C6	CHP34	LVDS out 34 positive
163	D6	CHN34	LVDS out 34 negative
164	B5	CHP35	LVDS out 35 positive
165	A5	CHN35	LVDS out 35 negative
166	E7	VDDLV	LVDS power 1.8V
167	E6	VSSLV	LVDS ground
168	C5	CHP36	LVDS out 36 positive
169	D5	CHN36	LVDS out 36 negative
170	D4	CHP37	LVDS out 37 positive
171	E4	CHN37	LVDS out 37 negative
172	F6	CHP38	LVDS out 38 positive
173	F7	CHN38	LVDS out 38 negative
174	F4	CHP39	LVDS out 39 positive
175	F5	CHN39	LVDS out 39 negative
176	E5	VDDLV	LVDS power 1.8V
177	G3	VSSLV	LVDS ground
178	F1	VDDLV	LVDS power 1.8V
179	G2	GNDK	Digital Core ground
180	G1	VDDK	Digital Core power 1.8V
181	H3	VAD4	Second ADC voltage (=VADH/4)
182	H2	VOFF	ADC offset voltage 0-1.2V
183	G4	AGND	Analog ground
184	H1	VAA	Analog power 3.3V
185	J3	VADL	ADC Reference Low = connect to AGND
186	H4	VADH	ADC Reference High 0.8V (0.2V-1V)
187	J2	AGND	Analog ground
188	J1	VAA	Analog power 3.3V
189	J4	GNDA	Analog driver ground 0V
190	K2	VDD3V	Analog Driver power 3.3V
191	K3	VRSTH	Pixel Reset High voltage
192	K1	VPIX	Pixel Reset Voltage 2.6V
193	K4	VTXH	Pixel Transfer High Voltage
194	L1	VTX2L	Pixel Second transfer Low
195	L3	VTXL	Pixel Transfer Low Voltage
196	M1	VABL_TST	Pixel AntiBlooming Bias
197	L2	VMUX1	Multipurpose override voltage; default- floating
198	F3	VMUX2	Multipurpose override voltage; default- floating

199	F2	VLNC	ADC comparator current
200	M2	data_dis_bn	Data read disable bottom;
201	M3	TX2_n	Global TX2_n control
202	L4	sdata	Serial Interface Data
203	M4	sclk	Serial Interface Clock
204	N1	Tr_en	Serial Interface Write
205	N3	VSSIO	Digital I/O ground
206	N2	clpout	Clamp pixel out
207	N4	GNDK	Digital Core ground
208	P1	VDDK	Digital Core power 1.8V
209	P3	pll_en_n	PLL enable control, Active Low
210	P2	VDDIO	Digital I/O power 1.8V (1.8V-2.3V)
211	P4		Reserved
212	R4	Standby_n	Standby control
213	T4	reduced	"1" enables reduced version of sensor with 1/2 outputs
214	R1	AB_n	Global photodiode reset
215	R3	Data_dis_tn	Data read disable top
216	R2	VLNA	Amplifier current control bias 0.95V (0.9V-1V)
217	Y2	VCAS	Amplifier Cascode voltage (=VREF+0.15V) override
218	X4	VREF	Amplifier reference 1.3V (1.2-1.4V)
219	T3	VABL_TST	Pixel AntiBlooming Bias
220	T2	VTXL	Transfer gate Low
221	Y3	VTX2L	Pixel Second transfer Low
222	T1	VTXH	Pixel Transfer High Voltage
223	U2	VPIX	Pixel Reset Voltage 2.6V (2.4V-3.6V)
224	U1	VRSTH	Pixel Reset High voltage 3.4V (2.5V-4.0V)
225	U3	VDD3V	Analog Driver power 3.3V
226	U4	GNDA	Analog Driver Ground 0V
227	V1	VAA	Analog Power 3.3V
228	V2	AGND	Analog ground
229	V3	VADH	ADC Reference High
230	W1	VADL	ADC Reference Low = connect to AGND
231	V4	VAA	Analog Power 3.3V
232	W4	AGND	Analog ground
233	W3	VOFF	ADC offset voltage 0-1.2V
234	W2	VAD4	Second ADC voltage (=VADH/4)
235	X2	VDDK	Digital Core power 1.8V
236	X1	GNDK	Digital Core ground
237	X3	VDDLV	LVDS power 1.8V
238	Y1	VSSLV	LVDS ground
239	AA5	VDDLV	LVDS power 1.8V

240	Y5	CHN79	LVDS out 79 negative
241	Y4	CHP79	LVDS out 79 positive
242	Y7	CHN78	LVDS out 78 negative
243	Y6	CHP78	LVDS out 78 positive
244	AA4	CHN77	LVDS out 77 negative
245	AB4	CHP77	LVDS out 77 positive
246	AB5	CHN76	LVDS out 76 negative
247	AC5	CHP76	LVDS out 76 positive
248	AA6	VSSLV	LVDS ground
249	AA7	VDDLV	LVDS power 1.8V
250	AE5	CHN75	LVDS out 75 negative
251	AD5	CHP75	LVDS out 75 positive
252	AB6	CHN74	LVDS out 74 negative
253	AC6	CHP74	LVDS out 74 positive
254	AE6	CHN73	LVDS out 73 negative
255	AD6	CHP73	LVDS out 73 positive
256	AB7	CHN72	LVDS out 72 negative
257	AC7	CHP72	LVDS out 72 positive
258	AA8	VSSLV	LVDS ground
259	Y8	VDDLV	LVDS power 1.8V
260	AE7	CHN71	LVDS out 71 negative
261	AD7	CHP71	LVDS out 71 positive
262	AB8	CHN70	LVDS out 70 negative
263	AC8	CHP70	LVDS out 70 positive
264	AE8	CHN69	LVDS out 69 negative
265	AD8	CHP69	LVDS out 69 positive
266	AC9	CHN68	LVDS out 68 negative
267	AB9	CHP68	LVDS out 68 positive
268	AA9	VSSLV	LVDS ground
269	Y9	VDDLV	LVDS power 1.8V
270	AE9	CHN67	LVDS out 67 negative
271	AD9	CHP67	LVDS out 67 positive
272	AC10	CHN66	LVDS out 66 negative
273	AB10	CHP66	LVDS out 66 positive
274	AE10	CHN65	LVDS out 65 negative
275	AD10	CHP65	LVDS out 65 positive
276	AC11	CHN64	LVDS out 64 negative
277	AB11	CHP64	LVDS out 64 positive
278	AA10	VSSLV	LVDS ground
279	AA11	VDDLV	LVDS power 1.8V
280	AE11	CHN63	LVDS out 63 negative

281	AD11	CHP63	LVDS out 63 positive
282	AC12	CHN62	LVDS out 62 negative
283	AB12	CHP62	LVDS out 62 positive
284	AE12	CHN61	LVDS out 61 negative
285	AD12	CHP61	LVDS out 61 positive
286	AA12	CHN60	LVDS out 60 negative
287	Y12	CHP60	LVDS out 60 positive
288	Y10	VSSLV	LVDS ground
289	AE13	DCLKN	LVDS clock out negative for outputs 60-79
290	AD13	DCLKP	LVDS clock out positive for outputs 60-79
291	Y11	VDDLV	LVDS power 1.8V
292	AB13	VSS_L	LVDS quiet bias ground
293	AC13	VCC_L	LVDS quiet bias power 1.8V
294	Y13	PLL_VDD	PLL power 1.8V
295	AA13	SYNCT	Sync pulse top for clock divide/2
296	AA14	MCLKT	Master clock top
297	Y14	PLL_GND	PLL ground
298	AC14	VCC_L	LVDS quiet bias power 1.8V
299	AB14	VSS_L	LVDS quiet bias ground
300	Y16	VSSLV	LVDS ground
301	AD14	PCLKN	LVDS clock out negative for outputs 40-59
302	AE14	PCLKP	LVDS clock out positive for outputs 40-59
303	Y17	VDDLV	LVDS power 1.8V
304	AD15	CHN59	LVDS out 59 negative
305	AE15	CHP59	LVDS out 59 positive
306	Y15	CHN58	LVDS out 58 negative
307	AA15	CHP58	LVDS out 58 positive
308	AD16	CHN57	LVDS out 57 negative
309	AE16	CHP57	LVDS out 57 positive
310	AB15	CHN56	LVDS out 56 negative
311	AC15	CHP56	LVDS out 56 positive
312	AA16	VSSLV	LVDS ground
313	Y18	VDDLV	LVDS power 1.8V
314	AD17	CHN55	LVDS out 55 negative
315	AE17	CHP55	LVDS out 55 positive
316	AB16	CHN54	LVDS out 54 negative
317	AC16	CHP54	LVDS out 54 positive
318	AD18	CHN53	LVDS out 53 negative
319	AE18	CHP53	LVDS out 53 positive
320	AB17	CHN52	LVDS out 52 negative
321	AC17	CHP52	LVDS out 52 positive

322	AA17	VSSLV	LVDS ground
323	AA18	VDDLV	LVDS power 1.8V
324	AD19	CHN51	LVDS out 51 negative
325	AE19	CHP51	LVDS out 51 positive
326	AB18	CHN50	LVDS out 50 negative
327	AC18	CHP50	LVDS out 50 positive
328	AD20	CHN49	LVDS out 49 negative
329	AE20	CHP49	LVDS out 49 positive
330	AC19	CHN48	LVDS out 48 negative
331	AB19	CHP48	LVDS out 48 positive
332	Y19	VSSLV	LVDS ground
333	AA19	VDDLV	LVDS power 1.8V
334	AD21	CHN47	LVDS out 47 negative
335	AE21	CHP47	LVDS out 47 positive
336	AC20	CHN46	LVDS out 46 negative
337	AB20	CHP46	LVDS out 46 positive
338	AD22	CHN45	LVDS out 45 negative
339	AE22	CHP45	LVDS out 45 positive
340	AC21	CHN44	LVDS out 44 negative
341	AB21	CHP44	LVDS out 44 positive
342	AA21	VSSLV	LVDS ground
343	AA20	VDDLV	LVDS power 1.8V
344	AB23	CHN43	LVDS out 43 negative
345	AA23	CHP43	LVDS out 43 positive
346	AC22	CHN42	LVDS out 42 negative
347	AB22	CHP42	LVDS out 42 positive
348	Y23	CHN41	LVDS out 41 negative
349	Y22	CHP41	LVDS out 41 positive
350	Y21	CHN40	LVDS out 40 negative
351	Y20	CHP40	LVDS out 40 positive
352	AA22	VSSLV	LVDS ground

8.0. PIN LIST FOR A SMALLER SIZE 344-pin uPGA.

Sensor pad	Package pin	Name	Comment
1, 352	W22	VSSLV	LVDS ground
2	U21	VDDLV	LVDS power 1.8V
3	V22	GNDK	Digital Core ground
4	T21	VDDK	Digital Core power
5	U22	VAD4	Second ADC voltage (=VADH/4)
6	T20	VOFF	ADC offset voltage 0-1.2V
7	T22	AGND	Analog ground
8	R19	VAA	Analog power 3.3V
9	R22	VADL	ADC Reference Low = connect to AGND
10	R20	VADH	ADC Reference High 0.8V (0.2V-1V)
11	R21	AGND	Analog ground
12	P18	VAA	Analog power 3.3V
13	P22	GNDA	Analog Driver ground, connect to AGND
14	P20	VDD3V	Analog Driver power 3.3V, connect to VAA
15	P21	VRSTH	Pixel Reset High voltage 3.4V (2.5V-4.0V)
16	P19	VPIX	Pixel Reset Voltage 1.2V (1.0V-3.6V)
17	N21	VTXH	Pixel Transfer High Voltage 3.3V (2.2V-3.6V)
18	N20	VTX2L	Pixel Second transfer Low (-0.3 : +0.5V)
19	N22	VTXL	Transfer gate Low (-0.3 : +0.5V)
20	N19	VABL_TST	Pixel AntiBlooming Bias (0-0.4V operation, upto 2.5V testing)
21	N18	VLN	Pixel SF Current control bias 0.55V (0.4V-0.6V or floating)
22	M18	St_read_tn	Start top SRAM read
23	M21	St_row_tn	Start top row read; 2clk minimum active LOW pulse
24	M20	PRST_n	Global Pixel Reset control
25	M19	rad7	Row address bit8
26	L18	rad5	Row address bit6
27	L19	rad3	Row address bit4
28	L20	rad1	Row address bit2
29	M22	lrst_n	Logic reset, asynchronous
30	L21	VDDIO	Digital I/O power 1.8V (1.8V-2.3V)
31	L22	VDDK	Digital Core power 1.8V
32	K21	GNDK	Digital Core ground
33	K22	VSSIO	Digital I/O ground
34	K20	rad0	Row address bit1
35	K19	rad2	Row address bit3

36	K18	rad4	Row address bit5
37	J19	rad6	Row address bit7
38	J20	rad8	Row address bit9
39	J22	TX_n	Global TX control
40	J18	St_row_bn	Start bottom row read; 2clk minimum active LOW pulse
41	J21	St_read_bn	Start bottom SRAM read
42	H19	VLN	Pixel SF Current control bias 0.55V (0.4V-0.6V) (=VLN)
43	H21	VABL_TST	Pixel AntiBlooming Bias
44	H20	VTXL	Transfer gate Low (-0.3 : +0.5V)
45	H22	VTX2L	Pixel Second transfer Low
46	H18	VTXH	Pixel Transfer High Voltage 3.3V
47	G19	VPIX	Pixel Reset Voltage
48	G20	VRSTH	Pixel Reset High voltage
49	G21	VDD3V	Analog Driver power 3.3V
50	G18	GNDA	Analog Driver ground 0V
51	G22	VAA	Analog Power 3.3V
52	F20	AGND	Analog ground
53	F22	VADH	ADC Reference High 0.8V (0.2V-1V)
54	F19	VADL	ADC Reference Low = connect to AGND
55	F21	VAA	Analog Power 3.3V
56	E20	AGND	Analog ground
57	E22	VOFF	ADC offset voltage 0-1.2V (=VOFF)
58	E21	VAD4	Second ADC voltage (=VADH/4)
59	D22	VDDK	Digital Core power 1.8V
60	D21	GNDK	Digital Core ground
61	C22	VDDLV	LVDS power 1.8V
62,63	B22	VSSLV	LVDS ground
64	D19	CHP0	LVDS out 0 positive
65	C19	CHN0	LVDS out 0 negative
66	C21	CHP1	LVDS out 1 positive
67	C20	CHN1	LVDS out 1 negative
68	E18	CHP2	LVDS out 2 positive
69	D18	CHN2	LVDS out 2 negative
70	B21	CHP3	LVDS out 3 positive
71	B20	CHN3	LVDS out 3 negative
72	D20	VDDLV	LVDS power 1.8V
73	A22	VSSLV	LVDS ground
74	C18	CHP4	LVDS out 4 positive
75	C17	CHN4	LVDS out 4 negative
76	A21	CHP5	LVDS out 5 positive

77	A20	CHN5	LVDS out 5 negative
78	D17	CHP6	LVDS out 6 positive
79	D16	CHN6	LVDS out 6 negative
80	B19	CHP7	LVDS out 7 positive
81	A19	CHN7	LVDS out 7 negative
82	F18	VDDLV	LVDS power 1.8V
83	E19	VSSLV	LVDS ground
84	E17	CHP8	LVDS out 8 positive
85	E16	CHN8	LVDS out 8 negative
86	B18	CHP9	LVDS out 9 positive
87	A18	CHN9	LVDS out 9 negative
88	C16	CHP10	LVDS out 10 positive
89	C15	CHN10	LVDS out 10 negative
90	B17	CHP11	LVDS out 11 positive
91	A17	CHN11	LVDS out 11 negative
92	F17	VDDLV	LVDS power 1.8V
93	F16	VSSLV	LVDS ground
94	E15	CHP12	LVDS out 12 positive
95	D15	CHN12	LVDS out 12 negative
96	B16	CHP13	LVDS out 13 positive
97	A16	CHN13	LVDS out 13 negative
98	D14	CHP14	LVDS out 14 positive
99	C14	CHN14	LVDS out 14 negative
100	B15	CHP15	LVDS out 15 positive
101	A15	CHN15	LVDS out 15 negative
102	F13	VDDLV	LVDS power 1.8V
103	F14	VSSLV	LVDS ground
104	E14	CHP16	LVDS out 16 positive
105	E13	CHN16	LVDS out 16 negative
106	B14	CHP17	LVDS out 17 positive
107	A14	CHN17	LVDS out 17 negative
108	D13	CHP18	LVDS out 18 positive
109	C13	CHN18	LVDS out 18 negative
110	B13	CHP19	LVDS out 19 positive
111	A13	CHN19	LVDS out 19 negative
112	F15	VDDLV	LVDS power 1.8V
113	C12	PCLKP	LVDS clock out positive for outputs 0-19
114	B12	PCLKN	LVDS clock out negative for outputs 0-19
115	F12	VSSLV	LVDS ground
116, 123	A12	VSS_L	LVDS quiet bias ground
117, 122	A11	VCC_L	LVDS quiet bias power 1.8V

118	E12	PLL_GND	PLL ground
119	D12	MCLKB	Master clock bottom
120	D11	SYNCB	Sync pulse bot for clock divide/2
121	E11	PLL_VDD	PLL power 1.8V
122		VCC_L	LVDS quiet bias power 1.8V
123		VSS_L	LVDS quiet bias ground
124	F11	VDDLV	LVDS power 1.8V
125	B11	DCLKP	LVDS clock out positive for outputs 20-39
126	C11	DCLKN	LVDS clock out negative for outputs 20-39
127	F10	VSSLV	LVDS ground
128	D10	CHP20	LVDS out 20 positive
129	C10	CHN20	LVDS out 20 negative
130	B10	CHP21	LVDS out 21 positive
131	A10	CHN21	LVDS out 21 negative
132	E10	CHP22	LVDS out 22 positive
133	E9	CHN22	LVDS out 22 negative
134	B9	CHP23	LVDS out 23 positive
135	A9	CHN23	LVDS out 23 negative
136	F9	VDDLV	LVDS power 1.8V
137	F8	VSSLV	LVDS ground
138	D9	CHP24	LVDS out 24 positive
139	C9	CHN24	LVDS out 24 negative
140	B8	CHP25	LVDS out 25 positive
141	A8	CHN25	LVDS out 25 negative
142	E8	CHP26	LVDS out 26 positive
143	D8	CHN26	LVDS out 26 negative
144	B7	CHP27	LVDS out 27 positive
145	A7	CHN27	LVDS out 27 negative
146	F7	VDDLV	LVDS power 1.8V
147	F6	VSSLV	LVDS ground
148	C8	CHP28	LVDS out 28 positive
149	C7	CHN28	LVDS out 28 negative
150	B6	CHP29	LVDS out 29 positive
151	A6	CHN29	LVDS out 29 negative
152	E7	CHP30	LVDS out 30 positive
153	D7	CHN30	LVDS out 30 negative
154	B5	CHP31	LVDS out 31 positive
155	A5	CHN31	LVDS out 31 negative
156	D3	VDDLV	LVDS power 1.8V
157	E4	VSSLV	LVDS ground
158	E6	CHP32	LVDS out 32 positive

159	D6	CHN32	LVDS out 32 negative
160	B4	CHP33	LVDS out 33 positive
161	A4	CHN33	LVDS out 33 negative
162	C6	CHP34	LVDS out 34 positive
163	C5	CHN34	LVDS out 34 negative
164	A3	CHP35	LVDS out 35 positive
165	A2	CHN35	LVDS out 35 negative
166	F5	VDDLV	LVDS power 1.8V
167	A1	VSSLV	LVDS ground
168	E5	CHP36	LVDS out 36 positive
169	D5	CHN36	LVDS out 36 negative
170	B3	CHP37	LVDS out 37 positive
171	B2	CHN37	LVDS out 37 negative
172	D4	CHP38	LVDS out 38 positive
173	C4	CHN38	LVDS out 38 negative
174	C3	CHP39	LVDS out 39 positive
175	C2	CHN39	LVDS out 39 negative
176,178	B1	VDDLV	LVDS power 1.8V
177	D2	VSSLV	LVDS ground
178		VDDLV	LVDS power 1.8V
179	E2	GNDK	Digital Core ground
180	C1	VDDK	Digital Core power 1.8V
181	G5	VAD4	Second ADC voltage (=VADH/4)
182	D1	VOFF	ADC offset voltage 0-1.2V
183	E3	AGND	Analog ground
184	E1	VAA	Analog power 3.3V
185	F4	VADL	ADC Reference Low = connect to AGND
186	F1	VADH	ADC Reference High 0.8V (0.2V-1V)
187	F3	AGND	Analog ground
188	F2	VAA	Analog power 3.3V
189	G4	GNDA	Analog driver ground 0V
190	G2	VDD3V	Analog Driver power 3.3V
191	G3	VRSTH	Pixel Reset High voltage
192	G1	VPIX	Pixel Reset Voltage 2.6V
193	H5	VTXH	Pixel Transfer High Voltage
194	H1	VTX2L	Pixel Second transfer Low
195	H3	VTXL	Pixel Transfer Low Voltage
196	H2	VABL_TST	Pixel AntiBlooming Bias
197	H4	VMUX1	Multipurpose override voltage; default- floating
198	J2	VMUX2	Multipurpose override voltage; default- floating
199	J5	VLNC	ADC comparator current

200	J1	data_dis_bn	Data read disable bottom;
201	J3	TX2_n	Global TX2_n control
202	J4	sdata	Serial Interface Data
203	K4	sclk	Serial Interface Clock
204	K2	Tr_en	Serial Interface Write
205	K3	VSSIO	Digital I/O ground
206	K1	clpout	Clamp pixel out
207	K5	GNDK	Digital Core ground
208	L5	VDDK	Digital Core power 1.8V
209	L4	pll_en_n	PLL enable control, Active Low
210	L2	VDDIO	Digital I/O power 1.8V (1.8V-2.3V)
211	L3		Reserved
212	L1	Standby_n	Standby control
213	M5	reduced	"1" enables reduced version of sensor with 1/2 outputs
214	M4	AB_n	Global photodiode reset
215	M3	Data_dis_tn	Data read disable top
216	M2	VLNA	Amplifier current control bias 0.95V (0.9V-1V)
217	N5	VCAS	Amplifier Cascode voltage (=VREF+0.15V) override
218	M1	VREF	Amplifier reference 1.3V (1.2-1.4V)
219	N4	VABL_TST	Pixel AntiBlooming Bias
220	N1	VTXL	Transfer gate Low
221	N3	VTX2L	Pixel Second transfer Low
222	N2	VTXH	Pixel Transfer High Voltage
223	P5	VPIX	Pixel Reset Voltage 2.6V (2.4V-3.6V)
224	P2	VRSTH	Pixel Reset High voltage 3.4V (2.5V-4.0V)
225	P4	VDD3V	Analog Driver power 3.3V
226	P1	GNDA	Analog Driver Ground 0V
227	P3	VAA	Analog Power 3.3V
228	T2	AGND	Analog ground
229	R3	VADH	ADC Reference High
230	R1	VADL	ADC Reference Low = connect to AGND
231	R2	VAA	Analog Power 3.3V
232	U2	AGND	Analog ground
233	R4	VOFF	ADC offset voltage 0-1.2V
234	T1	VAD4	Second ADC voltage (=VADH/4)
235	T3	VDDK	Digital Core power 1.8V
236	U1	GNDK	Digital Core ground
237,239	W1	VDDLV	LVDS power 1.8V
238	V1	VSSLV	LVDS ground
239		VDDLV	LVDS power 1.8V
240	V2	CHN79	LVDS out 79 negative

241	V3	CHP79	LVDS out 79 positive
242	V4	CHN78	LVDS out 78 negative
243	U4	CHP78	LVDS out 78 positive
244	W2	CHN77	LVDS out 77 negative
245	W3	CHP77	LVDS out 77 positive
246	U5	CHN76	LVDS out 76 negative
247	T5	CHP76	LVDS out 76 positive
248	X1	VSSLV	LVDS ground
249	R5	VDDLV	LVDS power 1.8V
250	X2	CHN75	LVDS out 75 negative
251	X3	CHP75	LVDS out 75 positive
252	V5	CHN74	LVDS out 74 negative
253	V6	CHP74	LVDS out 74 positive
254	X4	CHN73	LVDS out 73 negative
255	W4	CHP73	LVDS out 73 positive
256	U6	CHN72	LVDS out 72 negative
257	T6	CHP72	LVDS out 72 positive
258	T4	VSSLV	LVDS ground
259	U3	VDDLV	LVDS power 1.8V
260	X5	CHN71	LVDS out 71 negative
261	W5	CHP71	LVDS out 71 positive
262	U7	CHN70	LVDS out 70 negative
263	T7	CHP70	LVDS out 70 positive
264	X6	CHN69	LVDS out 69 negative
265	W6	CHP69	LVDS out 69 positive
266	V7	CHN68	LVDS out 68 negative
267	V8	CHP68	LVDS out 68 positive
268	R6	VSSLV	LVDS ground
269	R7	VDDLV	LVDS power 1.8V
270	X7	CHN67	LVDS out 67 negative
271	W7	CHP67	LVDS out 67 positive
272	U8	CHN66	LVDS out 66 negative
273	T8	CHP66	LVDS out 66 positive
274	X8	CHN65	LVDS out 65 negative
275	W8	CHP65	LVDS out 65 positive
276	V9	CHN64	LVDS out 64 negative
277	U9	CHP64	LVDS out 64 positive
278	R8	VSSLV	LVDS ground
279	R9	VDDLV	LVDS power 1.8V
280	X9	CHN63	LVDS out 63 negative
281	W9	CHP63	LVDS out 63 positive

282	T9	CHN62	LVDS out 62 negative
283	T10	CHP62	LVDS out 62 positive
284	X10	CHN61	LVDS out 61 negative
285	W10	CHP61	LVDS out 61 positive
286	V10	CHN60	LVDS out 60 negative
287	U10	CHP60	LVDS out 60 positive
288	R10	VSSLV	LVDS ground
289	V11	DCLKN	LVDS clock out negative for outputs 60-79
290	W11	DCLKP	LVDS clock out positive for outputs 60-79
291	R11	VDDLV	LVDS power 1.8V
292,299	X12	VSS_L	LVDS quiet bias ground
293,298	X11	VCC_L	LVDS quiet bias power 1.8V
294	T11	PLL_VDD	PLL power 1.8V
295	U11	SYNCT	Sync pulse top for clock divide/2
296	U12	MCLKT	Master clock top
297	T12	PLL_GND	PLL ground
298		VCC_L	LVDS quiet bias power 1.8V
299		VSS_L	LVDS quiet bias ground
300	R12	VSSLV	LVDS ground
301	W12	PCLKN	LVDS clock out negative for outputs 40-59
302	V12	PCLKP	LVDS clock out positive for outputs 40-59
303	R15	VDDLV	LVDS power 1.8V
304	X13	CHN59	LVDS out 59 negative
305	W13	CHP59	LVDS out 59 positive
306	V13	CHN58	LVDS out 58 negative
307	U13	CHP58	LVDS out 58 positive
308	X14	CHN57	LVDS out 57 negative
309	W14	CHP57	LVDS out 57 positive
310	T13	CHN56	LVDS out 56 negative
311	T14	CHP56	LVDS out 56 positive
312	R14	VSSLV	LVDS ground
313	R13	VDDLV	LVDS power 1.8V
314	X15	CHN55	LVDS out 55 negative
315	W15	CHP55	LVDS out 55 positive
316	V14	CHN54	LVDS out 54 negative
317	U14	CHP54	LVDS out 54 positive
318	X16	CHN53	LVDS out 53 negative
319	W16	CHP53	LVDS out 53 positive
320	U15	CHN52	LVDS out 52 negative
321	T15	CHP52	LVDS out 52 positive
322	R16	VSSLV	LVDS ground

323	R17	VDDLV	LVDS power 1.8V
324	X17	CHN51	LVDS out 51 negative
325	W17	CHP51	LVDS out 51 positive
326	V15	CHN50	LVDS out 50 negative
327	V16	CHP50	LVDS out 50 positive
328	X18	CHN49	LVDS out 49 negative
329	W18	CHP49	LVDS out 49 positive
330	T16	CHN48	LVDS out 48 negative
331	T17	CHP48	LVDS out 48 positive
332	T19	VSSLV	LVDS ground
333	R18	VDDLV	LVDS power 1.8V
334	X19	CHN47	LVDS out 47 negative
335	W19	CHP47	LVDS out 47 positive
336	U16	CHN46	LVDS out 46 negative
337	U17	CHP46	LVDS out 46 positive
338	X20	CHN45	LVDS out 45 negative
339	X21	CHP45	LVDS out 45 positive
340	V17	CHN44	LVDS out 44 negative
341	V18	CHP44	LVDS out 44 positive
342	X22	VSSLV	LVDS ground
343	U20	VDDLV	LVDS power 1.8V
344	W20	CHN43	LVDS out 43 negative
345	W21	CHP43	LVDS out 43 positive
346	U18	CHN42	LVDS out 42 negative
347	T18	CHP42	LVDS out 42 positive
348	V20	CHN41	LVDS out 41 negative
349	V21	CHP41	LVDS out 41 positive
350	V19	CHN40	LVDS out 40 negative
351	U19	CHP40	LVDS out 40 positive
352		VSSLV	LVDS ground

9.0. DESCRIPTION OF BIASES AND CONTROLS.

Column AMP, ADC and Pixel Biases, Absolute ratings and loading requirements.

Name	Min	Typ	Max	Current (mA) or specific requirements
VADH	0.1V	1V	1.2V	Must charge a 6nF capacitor from 0V to 1V once in 1 us with 0.1% settling accuracy within 10 ns. Average consumption is ~6 mA. No Start_row pulses- no consumption.
VADL	0	0	0V	Connect to AGND
VOFF	0	0.7V	1.2V	Similar to VADH, with capacitor size 1/8 of 6nF
VAD4	0	¼ of VADH	0.3V	Similar to VADH, with capacitor size 1/16 of 6nF
VLN	0.4V	0.6V	0.8V	Either leave floating or apply an override assuming a diode-connected load with conductance about 100 Ohm
VLNA	0.7V	0.95V	1.2V	Either leave floating or apply an override assuming a diode-connected load with conductance about 100 Ohm. Lower VLNA helps to reduce the sensor heating but may result in image artifacts such as a horizontal striping
VLNC	0.8V	0.9V	1.1V	Either leave floating or apply an override assuming a diode-connected load with conductance about 1 kOhm
VREF	1.0V	1.2V	+1.5V	<10 mA, high precision <1mV p-p
VCAS	ii	VREF+0.2V	ii	<10 mA, medium precision <20mV p-p
VPIX	1.2V	1.4V	2.5V	DC current of <100 mA, noise <1mV p-p, AC current: Must charge a 5nF capacitor at delta-V of +-0.2V once in frame time with 0.1% settling accuracy within 30 ns.
VRSTH	2.0V	3.3V	3.6V	DC current of <10 mA, noise <10mV p-p, AC current: Must charge a 5nF capacitor at delta-V of +-3V once in frame time with 1% settling accuracy within 30 ns.
VTXH	2.0V	3.3V	3.6V	Similar to VRSTH
VABL_TST	0V	0.2V	2.5V	Requirements relaxed 10X times compared to VRSTH. High voltage is only needed for a testing/troubleshoot purpose.
VTXL	-0.4	0	1	Connect to AGND or to -0.3V, requirements relaxed 10X compared to VRSTH
VTX2L	0	0.4V	0.9V	Requirements relaxed 10X times compared to VRSTH. Powerful tool to fight Lag in the shutter node
VMUX1	0.8	0.9V	2.5V	Overrides one of VLNs, so the requirements
VMUX2	0.8	0.9V	2.5V	Overrides one of VLNs, so the requirements

10.0. NEW FUNCTIONALITY.

Clpout.

Some of our previous sensors showed increased black level when increasing the sensor clock rate. In LUX13HS, we implemented a “Clamp pixel output” feature which allows to interfere into the pixel readout and to control the pixel black level. Clamp_pout was implemented as the register setting and as an external I/O control.

Internally generated Clpout is enabled by High at Bit14 of the register. The default for Bit14 is LOW and thus No clpout pulse. We did not found this control to be any useful as the pixel bus is already clamped during the horizontal blank.

The external "Clpout" is enabled by HIGH at the I/O pad 206 (pin N2). We found Clpout may indeed increase the Dark offset in the image if applied HIGH at the clock 46 through 58 after every "Start_row" pulse. The longer the clpout the darker the image.

SH_VLN

Sample and hold VLN is a switched capacitor filter which provides a more stable VLN bias to the pixel source followers across the array.

It is enabled by Register Bit13. When HIGH it enables the filter. When LOW (default), it provides regular VLN generation like in predecessor devices.

Data Disable

Data disable restores the feature we had in early sensors allowing to freeze the data read and restart it. LUX13HS has two external controls, one for the top readout and one for the bottom readout. Data_dis_bn and Data_dis_tn. These are pull-up pins which are High by default which means the data read is always enabled. Low at one of the pins stops the corresponding column counter in synchronous fashion, i.e. on the next rising edge of the clock. Bringing Data disable control Up restores the count.

Making the break in the readout allows freeze the noisy readout operation in the sensitive moments of the pixel readout and thus allows to minimize electronic noise introduced into the signal from the pixel.

11.0. DATA ENCODING.

The block-diagram of the Data Output (bottom only, top is symmetrical) is presented in Fig.9. The left and the right halves of the image are serialized separately through LVDS ports 0:19 and 20:39, respectively. The top channels of the sensor are 40:59 on the left and 60:79 on the right.

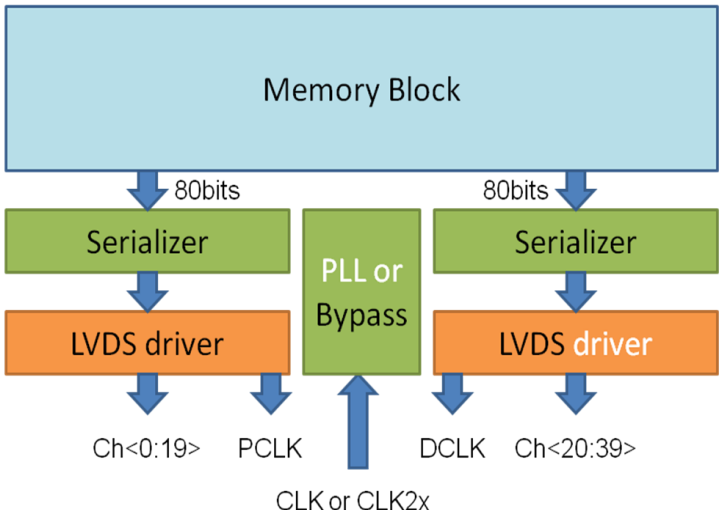

Fig.9. Block diagram for the digital output.

From the ADC registers (Memory Block) the data come as 8 ports left and 8 ports right of 10b LVCMOS data. Each serializer packs 4 data into one LVDS differential output. At the default rate of the input data of 133 MHz, the LVDS data rate is 532 MHz. The data is serialized w/o overhead for the synchs, so it should be recovered with the help of the frame timing generated by the user. The timing for the serializer and the LVDS out clocks is presented below:

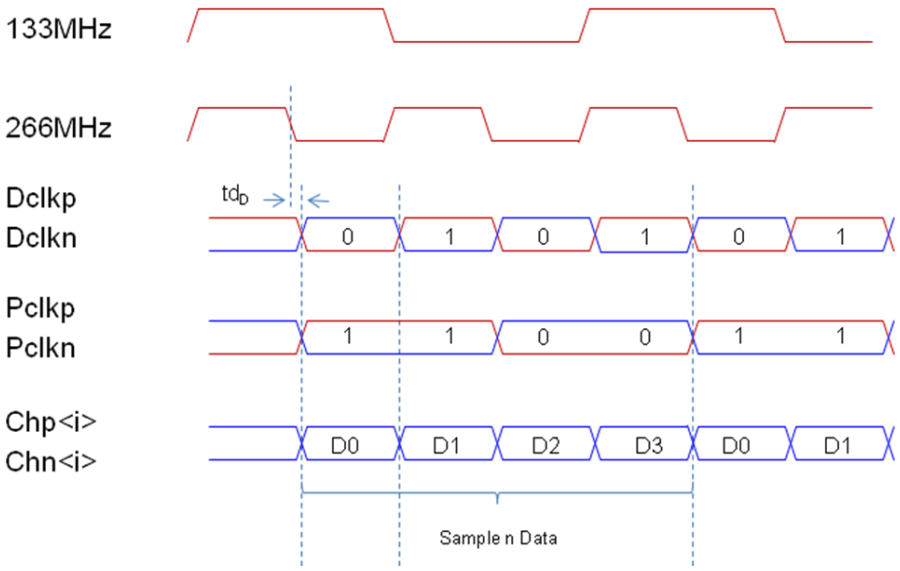

Fig.10. Block diagram for the digital output

The serialization Table is defined as follows:

LVDS channel	D0	D1	D2	D3	Next clk D0
CHP(N)0& 40	C0R0_Bit6	C0R0_Bit7	C0R0_Bit8	C0R0_Bit9	C4R0_Bit6
CHP(N)1, 41	C0R0_Bit2	C0R0_Bit3	C0R0_Bit4	C0R0_Bit5	C4R0_Bit2
CHP(N)2, 42	C0R1_Bit6	C0R1_Bit7	C0R1_Bit8	C0R1_Bit9	C4R1_Bit6
CHP(N)3, 43	C0R1_Bit2	C0R1_Bit3	C0R1_Bit4	C0R1_Bit5	C4R1_Bit2
CHP(N)4, 44	C1R0_Bit6	C1R0_Bit7	C1R0_Bit8	C1R0_Bit9	C5R00_Bit6
CHP(N)5, 45	C1R0_Bit2	C1R0_Bit3	C1R0_Bit4	C1R0_Bit5	C5R00_Bit2
CHP(N)6, 46	C1R1_Bit6	C1R1_Bit7	C1R1_Bit8	C1R1_Bit9	C5R1_Bit6
CHP(N)7, 47	C1R1_Bit2	C1R1_Bit3	C1R1_Bit4	C1R1_Bit5	C5R1_Bit2
CHP(N)8, 48	C2R0_Bit6	C2R0_Bit7	C2R0_Bit8	C2R0_Bit9	C6R0_Bit6
CHP(N)9, 49	C2R0_Bit2	C2R0_Bit3	C2R0_Bit4	C2R0_Bit5	C6R0_Bit2
CHP(N)10, 50	C2R1_Bit6	C2R1_Bit7	C2R1_Bit8	C2R1_Bit9	C6R1_Bit6
CHP(N)11, 51	C2R1_Bit2	C2R1_Bit3	C2R1_Bit4	C2R1_Bit5	C6R1_Bit2
CHP(N)12, 52	C3R0_Bit6	C3R0_Bit7	C3R0_Bit8	C3R0_Bit9	C7R0_Bit6
CHP(N)13, 53	C3R0_Bit2	C3R0_Bit3	C3R0_Bit4	C3R0_Bit5	C7R0_Bit2
CHP(N)14, 54	C3R1_Bit6	C3R1_Bit7	C3R1_Bit8	C3R1_Bit9	C7R1_Bit6
CHP(N)15, 55	C3R1_Bit2	C3R1_Bit3	C3R1_Bit4	C3R1_Bit5	C7R1_Bit2
CHP(N)16, 56	C1R0_Bit0	C1R0_Bit1	C0R0_Bit0	C0R0_Bit1	C5R0_Bit0
CHP(N)17, 57	C3R0_Bit0	C3R0_Bit1	C2R0_Bit0	C2R0_Bit1	C7R0_Bit0
CHP(N)18, 58	C1R1_Bit0	C1R1_Bit1	C0R1_Bit0	C0R1_Bit1	C5R1_Bit0
CHP(N)19, 59	C3R1_Bit0	C3R1_Bit1	C2R1_Bit0	C2R1_Bit1	C7R1_Bit0
CHP(N)20, 60	C1291r1_Bit0	C1291r1_Bit1	C1290r1_Bit0	C1290r1_Bit1	C1295r1_Bit0
CHP(N)21, 61	C1289r1_Bit0	C1289r1_Bit1	C1288r1_Bit0	C1288r1_Bit1	C1293r1_Bit0
CHP(N)22, 62	C1291r0_Bit0	C1291r0_Bit1	C1290r0_Bit0	C1290r0_Bit1	C1295r0_Bit0
CHP(N)23, 63	C1289r0_Bit0	C1289r0_Bit1	C1288r0_Bit0	C1288r0_Bit1	C1293r0_Bit0
CHP(N)24, 64	C1291r1_Bit2	C1291r1_Bit3	C1291r1_Bit4	C1291r1_Bit5	C1295r1_Bit2
CHP(N)25, 65	C1291r1_Bit6	C1291r1_Bit7	C1291r1_Bit8	C1291r1_Bit9	C1295r1_Bit6
CHP(N)26, 66	C1291r0_Bit2	C1291r0_Bit3	C1291r0_Bit4	C1291r0_Bit5	C1295r0_Bit2
CHP(N)27, 67	C1291r0_Bit6	C1291r0_Bit7	C1291r0_Bit8	C1291r0_Bit9	C1295r0_Bit6
CHP(N)28, 68	C1290r1_Bit2	C1290r1_Bit3	C1290r1_Bit4	C1290r1_Bit5	C1294r1_Bit2
CHP(N)29, 69	C1290r1_Bit6	C1290r1_Bit7	C1290r1_Bit8	C1290r1_Bit9	C1294r1_Bit6
CHP(N)30, 70	C1290r0_Bit2	C1290r0_Bit3	C1290r0_Bit4	C1290r0_Bit5	C1294r0_Bit2
CHP(N)31, 71	C1290r0_Bit6	C1290r0_Bit7	C1290r0_Bit8	C1290r0_Bit9	C1294r0_Bit6
CHP(N)32, 72	C1289r1_Bit2	C1289r1_Bit3	C1289r1_Bit4	C1289r1_Bit5	C1293r1_Bit2
CHP(N)33, 73	C1289r1_Bit6	C1289r1_Bit7	C1289r1_Bit8	C1289r1_Bit9	C1293r1_Bit6
CHP(N)34, 74	C1289r0_Bit2	C1289r0_Bit3	C1289r0_Bit4	C1289r0_Bit5	C1293r0_Bit2
CHP(N)35, 75	C1289r0_Bit6	C1289r0_Bit7	C1289r0_Bit8	C1289r0_Bit9	C1293r0_Bit6
CHP(N)36, 76	C1288r1_Bit2	C1288r1_Bit3	C1288r1_Bit4	C1288r1_Bit5	C1292r0_Bit2
CHP(N)37, 77	C1288r1_Bit6	C1288r1_Bit7	C1288r1_Bit8	C1288r1_Bit9	C1292r1_Bit6
CHP(N)38, 78	C1288r0_Bit2	C1288r0_Bit3	C1288r0_Bit4	C1288r0_Bit5	C1292r0_Bit2
CHP(N)39, 79	C1288r0_Bit6	C1288r0_Bit7	C1288r0_Bit8	C1288r0_Bit9	C1292r0_Bit6

Here, C0r0_Bit6 means the digital data Bit 6 (0 to 9) of the row 0 and Column 0.

For the convenience to design 8b only cameras, the top 8b of the data are signaled through 16 LVDS outputs on each sensor corner while the remaining 2b data are grouped together and output through remaining 4 LVDS ports.

The data packing table can be extended using the following rules:

For the outputs CHP(N) 0 through 19 and 40 through 59 the order of the column/row read is as follows:

Clk1	Clk2	Clk3	Clk4		Clk161	Clk162
C0- C3 R0& R1	C4- C7 R0& R1	C644- 647 R0& R1	C640- 643 R0& R1	…	C12- C15 R0& R1	C8- C11 R0& R1

For the outputs CHP(N) 39 down to 20 and 79 down to 60, the order of the column/row read is as follows:

Clk1	Clk2	Clk3	Clk4		Clk161	Clk162
C1288-1291 R0& R1	C1292-1295 R0& R1	C648-651 R0& R1	C652- 655 R0& R1	…	C1280-1283 R0& R1	C1284-1287 R0& R1

The register bit MSB_first changes the order of the bits within each group of 4 (D0- D3) from lower-to-higher (such as Bit6 to Bit9) into the higher-to-lower (such as Bit9 to Bit6).

***Serializer Delay*. Compared to the predecessor AM41, the data after serializer is further delayed by approximately 1 ¼ clock.**

12.0. PLL.

Sensor has internal PLL (one in top and one in bottom) which locks to the external Master Clock of 100…133…166 MHz. The PLL generates 2X-4X clocks for Serializer. PLL is enabled via package control pin 211 *pll_en_n* active LOW.

The internal PLL can be disabled, and then the clock applied to the sensor needs to be 2X of frequency e.g. 266 MHz, and should have 50%/50% duty cycle. In this mode, the sensor generates internal 133 MHz clock for its sensor core. **Please make sure all controls coming to the sensor are at least 2 (266Mhz) clock long to be correctly sampled.**

The internal divide by 2 block which generates 133Mhz needs a sync pulse to define the phase of 133MHz clock with respect to external commands. This is done with a short Sync pulse applied to pins 120 and 295 SYNCB and SYNCT.

When PLL is ON these syncs are not needed.

To initiate PLL, a certain power-up or control sequence is required (see p. 13.0)

13.0. SERIAL INTERFACE DESCRIPTION.

Serial interface in AM41-AM63 serves one function: to write the 16 sensor settings into the sensor controllers. The sensor settings are written in using the following pins: sdata, sclk, Tr_en. Serial interface allows to enable/disable 16 sensor setting controls:

Reg #	Name	Description
Bit0	Col_test_en	"1" disables pixel read and enables Column test with (VTST-AGND) as an input signal; Defailt is "0"
Bit1	Offset_sign	"1" makes the offset negative, "0:- positive. The offset value is controlled with VOFF voltage.
Bit2	Gain_X2_en	"1" enables gain X2
Bit3	Gain_bit1_en	"1" enables another gain X2 through reducing amp feedback capacitor
Bit4	Gain_bit2_en	With Bit3 ON, this enables another gain x2 through reducing amp feedback capacitance further
Bit5	Unipolar_ADC	"1" disconnects dummy differential circuit
Bit6	Long_latch	"1" Increases time for comparator decision, decreases for signal settling
Bit7	Row_cut_dis_b	"1" enables change in row select signal; may affect fpn
Bit8	Short_X_window	Enables 149 column read versus 162 column default
Bit9	VLN_cas_en_b	VLN cascode enable; "1" disables the cascoding
Bit10-11	VMUX1	Overrides internal biases VCASNA (00), VCASVLN (01) , VCASN2 (10), VCASN3 (11)
Bit12	VMUX2	Overrides internal biases VLN3 (0) and VLNT (1)
Bit13	SH_VLN*	Enables internal filter for VLN bias
Bit14	Cl_pout*	Enables the clamp for pixel driver
Bit15	Extended _tx	1 extends in-row TX pulse
Bit16	Pwren_lvds_b	"0" is power enable for LVDS drivers
Bit17	Pwren_bias_b	"0" enables current DACs for LVDS
Bit18	MSB_first	"0" enables "LSB first"
Bit21-19	LVDS current	2.5mA(001), 3.5mA (000), 4.5mA(010), 6mA(110)
Bit22	Term_off_b	"0" disables on chip termination

12.1. Timing of the interface

The serial interface is a D-flop shift register clocked by Sclk. Every rising edge of Sclk samples new Sdata into the register and moves the data written before by 1 bit. 24 Sclks update the entire register. **The bit written first is the bit #23 (the last bit).** For new register data to take effect on the image sensor, one needs to apply a Transfer enable (Tr_en) HIGH pulse, and on the first Low-to-Hign transition of the Clk_top (Clk_bot), the new register data is overwritten into the Digital Block registers.

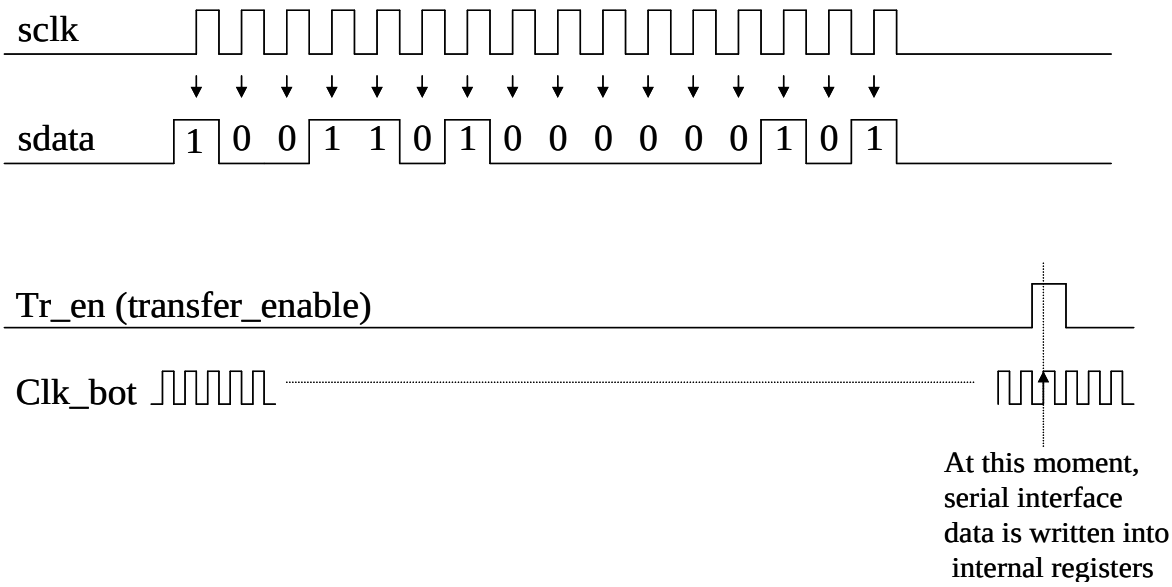

Fig.12. Operation of the serial register in the sensor setting mode.

14.0. Sensor Start-up Troubleshooting.

PLL Startup.

PLL is initiated with PLL_VDD going up from zero. However, if VDDLV is powered up at the same time, the PLL does not get enough supply current, so it may not initiate.

To resolve this, either PLL_VDD is delayed by >2us with respect to VDDLV/VDDK or the following reset sequence is enabled after power-up:

1) All powers up. 2) Apply logic reset lrst_n 3) Disable and enable again pll_en_n.

When PLL initiates, one may observe PCLK and DCLK signals from the sensor clock outputs. Yet, even with working PLL, the clock signals may be missing of there is no LVDS termination as foloows:

LVDS termination. By default, internal 100 Ohm termination in the sensor LVDS drivers is disabled. It is expected that the user has 100 Ohm termination on the receiving end. If the termination resistors are missing, the user may enable internal termination. This leads to higher power dissipation by the sensor and hence, heating.

Data is coming out, but Sensor is not sensitive to light.
When initially debugging the sensor, please use simplified Global pixel controls, as follows:
PRST_n = LOW
AB_n =HIGH
TX2_n = HIGH

TX_n is a pulse as in Fig.5

Make sure VPIX~ 1.5V is not too high.

Difficulty to unscramble the serializer data.

Please use the fact that PCLK which is the Word Sync for the serialized data is ALIGNED with the data. Generate the sampling clock in your FPGA, divide it by 2 (double edge data sampling) or by 4 (rising only edge sampling) and lock it to PCLK. You should now have no difficulty to sort within the group of bits 6-9 and bits 2-5. The remaining total data delay to Start_read now can be found within 2-3 trials.

15.0. Reduced (2:1 Multiplexed) Mode.

By enabling "1" at the Reduced pin, user switched the sensor into the Reduced/Multiplexed Data Output mode. Number of the output ports is reduced in half, and the internal Divide by 2 reduces the sensor core clock in half.

Of the output LVDS channels 0-80, every second pair of LVDS drivers is disabled and the data from the four nearby pads is consolidated into the first two outputs.

Reduced mode might be beneficial to the users who want to limit the width of the output sensor interface and who do not need the maximize frame rate from the sensor.

LUX13HS "reduced" will also be offered in a new, lower pin count and smaller size package (see 16.0-18.0) to enable a cost-effective solution to the users not pursuing the maximum data rate.

As the core of the sensor runs with ½ clock, the bottlenecks associated with the sensor core operation are removed, and the sensor in the reduced/Multiplexed mode may perform at the frame rate higher than ½ of the frame rate in the Full interface mode.

The serialization table for "reduced" mode:

LVDS channel	D0	D1	D2	D3	Next D0	Next D1	Next D2	Next D3
CH 0, 40	C0r0b6	C0r0b7	C0r0b8	C0r0b9	C0r1b6	C0r1b7	C0r1b8	C0r1b9
CH 1, 41	C0r0b2	C0r0b3	C0r0b4	C0r0b5	C0r1b2	C0r1b3	C0r1b4	C0r1b5
CH 2, 42	no data	no data	no data	no data	no data	no data	no data	no data
CH 3, 43	no data	no data	no data	no data	no data	no data	no data	no data
CH 4, 44	C1r0b6	C1r0b7	C1r0b8	C1r0b9	C1r1b6	C1r1b7	C1r1b8	C1r1b9
CH 5, 45	C1r0b2	C1r0b3	C1r0b4	C1r0b5	C1r1b2	C1r1b3	C1r1b4	C1r1b5
CH 6, 46	no data	no data	no data	no data	no data	no data	no data	no data
CH 7, 47	no data	no data	no data	no data	no data	no data	no data	no data
CH 8, 48	C2r0b6	C2r0b7	C2r0b8	C2r0b9	C2r1b6	C2r1b7	C2r1b8	C2r1b9
CH 9, 49	C2r0b2	C2r0b3	C2r0b4	C2r0b5	C2r1b2	C2r1b3	C2r1b4	C2r1b5
CH 10, 50	no data	no data	no data	no data	no data	no data	no data	no data

CH 11, 51	no data	no data	no data	no data	no data	no data	no data	no data
CH 12, 52	C3r0b6	C3r0b7	C3r0b8	C3r0b9	C3r1b6	C3r1b7	C3r1b8	C3r1b9
CH 13, 53	C3r0b2	C3r0b3	C3r0b4	C3r0b5	C3r1b2	C3r1b3	C3r1b4	C3r1b5
CH 14, 54	no data	no data	no data	no data	no data	no data	no data	no data
CH 15, 55	no data	no data	no data	no data	no data	no data	no data	no data
CH 16, 56	C1r0b0	C1r0b1	C0r0b0	C0r0b1	C1r1b0	C1r1b1	C0r1b0	C0r1b1
CH 17, 57	C3r0b0	C3r0b1	C2r0b0	C2r0b1	C3r1b0	C3r1b1	C2r1b0	C2r1b1
CH 18, 58	no data	no data	no data	no data	no data	no data	no data	no data
CH 19, 59	no data	no data	no data	no data	no data	no data	no data	no data
CH 20, 60	no data	no data	no data	no data	no data	no data	no data	no data
CH 21, 61	no data	no data	no data	no data	no data	no data	no data	no data
CH 22, 62	C1291r1b0	C1291r1b1	C1290r1b0	C1290r1b1	C1291r0b0	C1291r0b1	C1290r0b0	C1290r0b1
CH 23, 63	C1289r1b0	C1289r1b1	C1288r1b0	C1288r1b1	C1289r0b0	C1289r0b1	C1288r0b0	C1288r0b1
CH 24, 64	no data	no data	no data	no data	no data	no data	no data	no data
CH 25, 65	no data	no data	no data	no data	no data	no data	no data	no data
CH 26, 66	C1291r1b2	C1291r1b3	C1291r1b4	C1291r1b5	C1291r0b2	C1291r0b3	C1291r0b4	C1291r0b5
CH 27, 67	C1291r1b6	C1291r1b7	C1291r1b8	C1291r1b9	C1291r0b6	C1291r0b7	C1291r0b8	C1291r0b9
CH 28, 68	no data	no data	no data	no data	no data	no data	no data	no data
CH 29, 69	no data	no data	no data	no data	no data	no data	no data	no data
CH 30, 70	C1290r1b2	C1290r1b3	C1290r1b4	C1290r1b5	C1290r0b2	C1290r0b3	C1290r0b4	C1290r0b5
CH 31, 71	C1290r1b6	C1290r1b7	C1290r1b8	C1290r1b9	C1290r0b6	C1290r0b7	C1290r0b8	C1290r0b9
CH 32, 72	no data	no data	no data	no data	no data	no data	no data	no data
CH 33, 73	no data	no data	no data	no data	no data	no data	no data	no data
CH 34, 74	C1289r1b2	C1289r1b3	C1289r1b4	C1289r1b5	C1289r0b2	C1289r0b3	C1289r0b4	C1289r0b5
CH 35, 75	C1289r1b6	C1289r1b7	C1289r1b8	C1289r1b9	C1289r0b6	C1289r0b7	C1289r0b8	C1289r0b9
CH 36, 76	no data	no data	no data	no data	no data	no data	no data	no data
CH 37, 77	no data	no data	no data	no data	no data	no data	no data	no data
CH 38, 78	C1288r1b2	C1288r1b3	C1288r1b4	C1288r1b5	C1288r0b2	C1288r0b3	C1288r0b4	C1288r0b5
CH 39, 79	C1288r1b6	C1288r1b7	C1288r1b8	C1288r1b9	C1288r0b6	C1288r0b7	C1288r0b8	C1288r0b9

Here, C0r0b6 is column 0 row 0 bit 6 etc.,

16.0. PACKAGE 1.

Option 1 is a 1.27mm pitch 352 micro-PGA of ~36mm size.

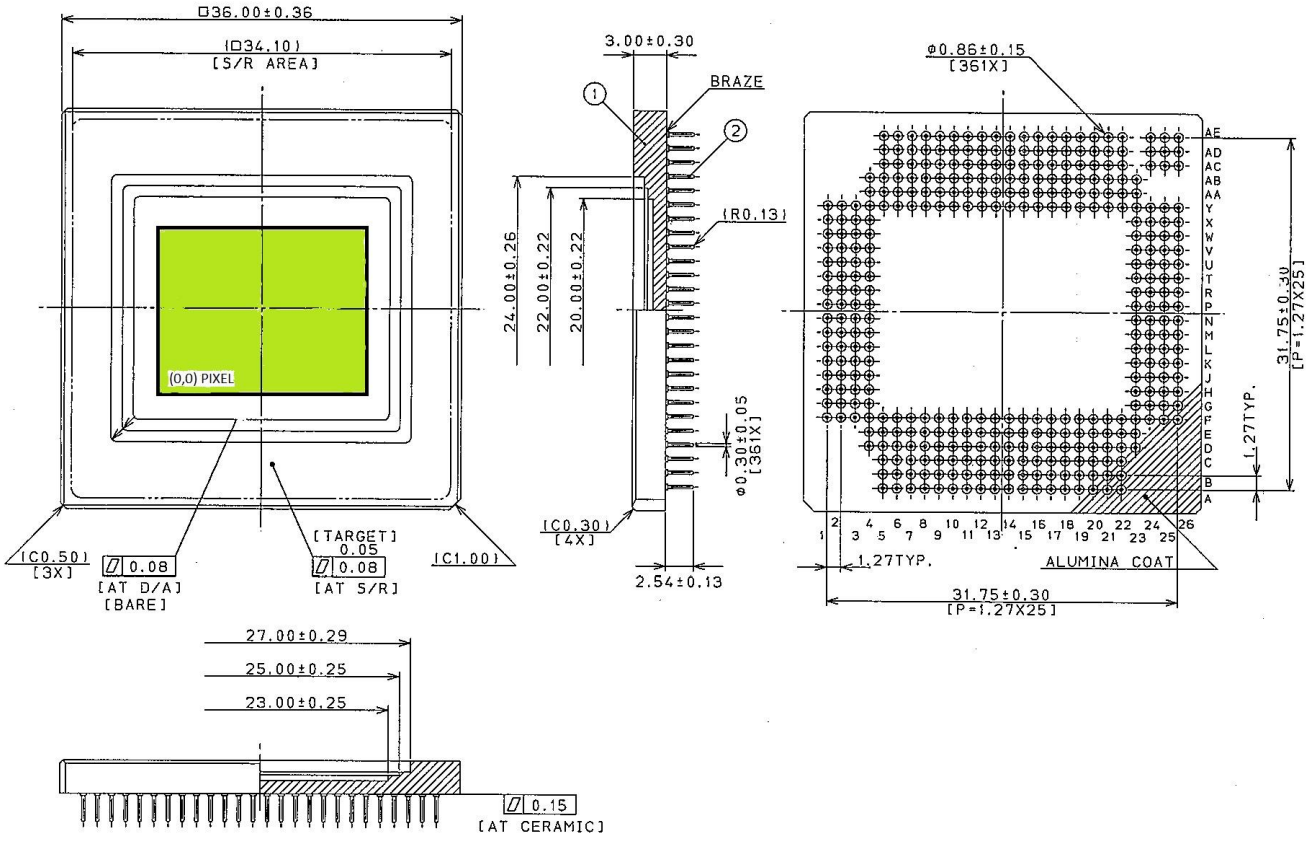

Fig.12. LUX13HS in 352 micro-PGA package. Chip position and pixel array position in the package are symmetrical top-bottom and left-right. Bottom LVDS outputs are rows A-F.

Pins AC24-AE26 (9 pins) are non-connect orientation pins.

Not shown on this picture:
Glass thickness 0.8mm
Sensor thickness 0.725mm
Thickness of the package under the cavity: 1.2mm

For the test socket, one may try to use the Intel mobile 478-479 socket
http://download.intel.com/design/mobile/applnots/29852001.pdf

Andon (AEC) has designed a hole-through socket for our package. The part number is 10-26-32-361-400T4-R27-L14

The advantage of a larger size package is a better cooling if the front of the sensor has a thermal sink to the camera enclosure.

17.0. PACKAGE 2 (FULL INTERFACE, SMALLER SIZE).

- a 1.27mm pitch 344 micro-PGA of ~30 (H) x 28 (V) mm size.

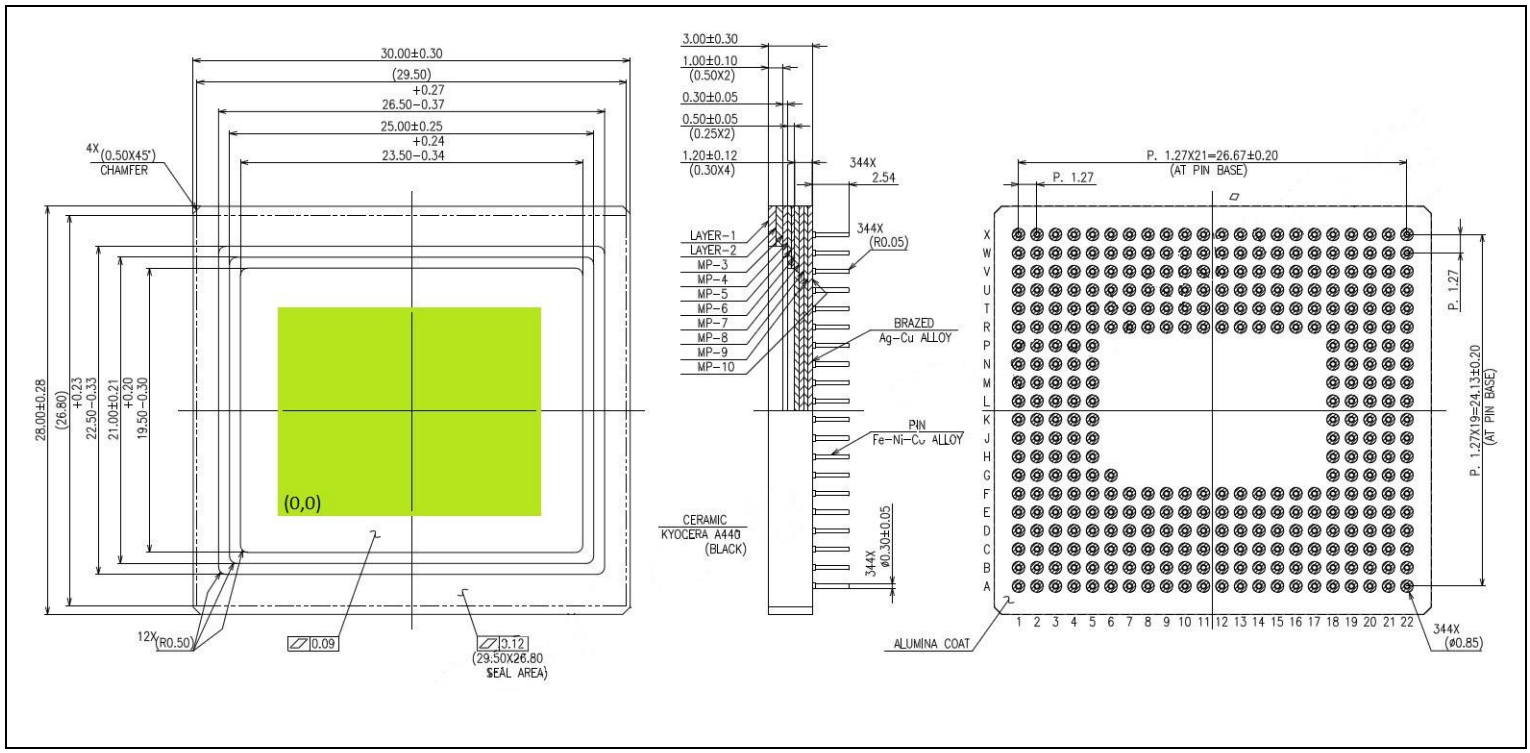

Fig.12. LUX13HS in 344 micro-PGA package. Chip position and pixel array position in the package are symmetrical top-bottom and left-right. Bottom LVDS outputs are rows A-F.

Known sockets:

1. Andon, 10-22-14A-345-281UM-R27-L14 (surface mount), 10-22-14A-345-274UM-R27-L14 (hole through). We did not try it yet so can not fully endorse. The terminal is wide so should have low insertion force, while 6 contact leaves should assure good contact.

18.0. PACKAGE 3 (REDUCED PIN OPTION).

- a 1.27mm pitch 237 micro-PGA of ~30.5 (H) x 28.5 (V) mm size.

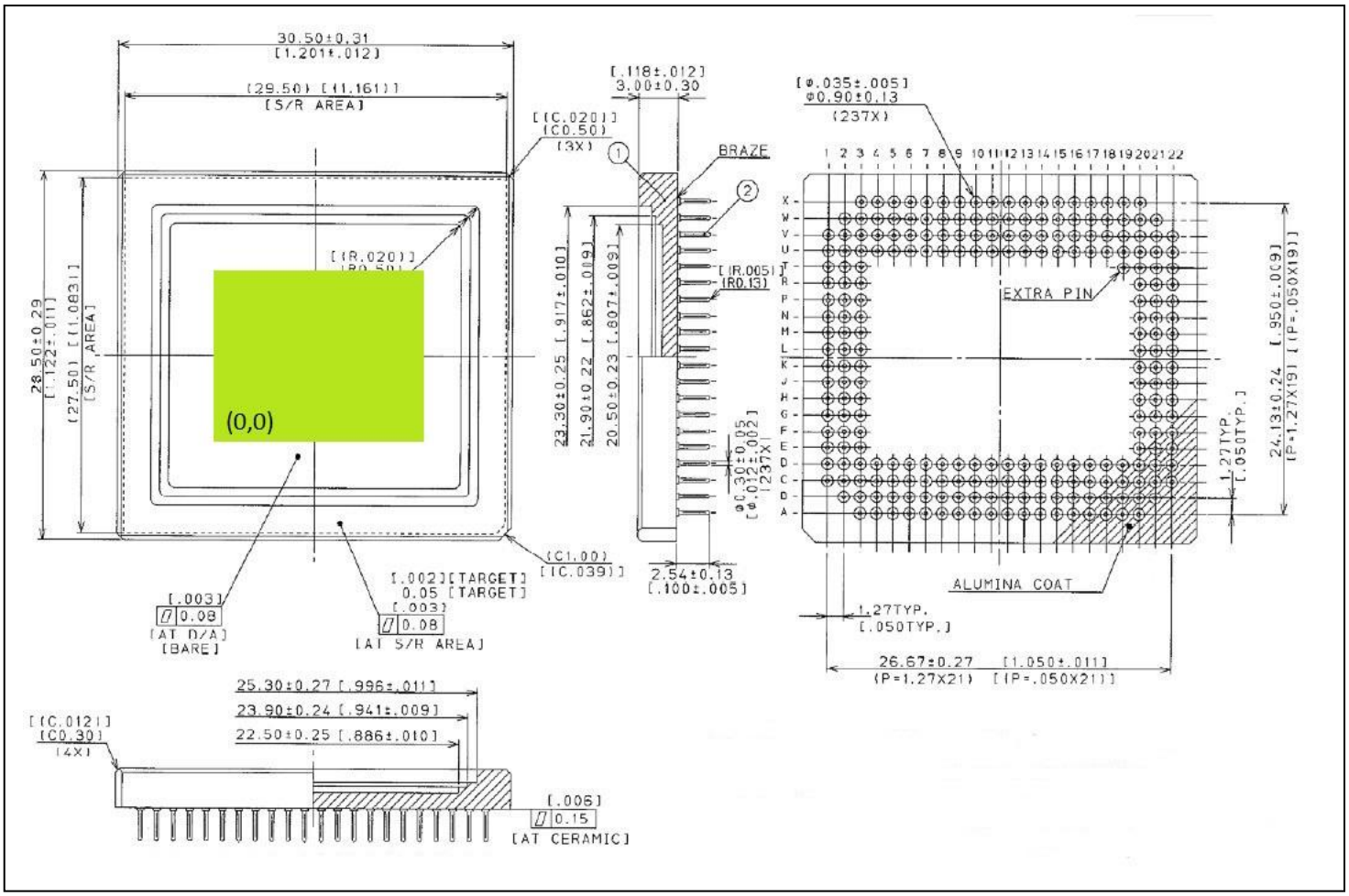

Fig.12. LUX13HS in a 237-pin micro-PGA package.

Status: pending.