A 1k x 1k 3-5 kFrames/s Shuttered CMOS Digital Image Sensor (AM1X5)

INTERFACE CONTROL DOCUMENT

Revision 4

August 20, 2015

Dr. Alexander I. Krymski, Chief Scientist
ALEXIMA

REVISION HISTORY

Date	Revision	Comments
11.17.06	1.0	First draft
01.05.07	2.0	Second draft
03.26.2011	3.0	Changes made after optimizing camera performance
08.30.2015	4.0	New small package and the pin list

INTRODUCTION

AM1X5 is a super high speed digital CMOS sensor. This sensor targets frame rate from 3,000 Fps minimum to 5,000 Fps maximum, with the data throughput of 3-5 Gpix/s. This is 2.5-4 times faster than the throughput of 1.3 Gpix/s from the previous generation MV03 sensor. An increase in data rate is achieved through using 4 ADCs per column, wider (8 pairs) width of the data register bus, and employing double data rate SSTL-2 I/O pads. Another feature of AM1X5 is a buried channel shutter pixel. We expect a breakthrough in sensitivity from the pixel.

The circuitry of AM1X5 is protected with a pending patents.

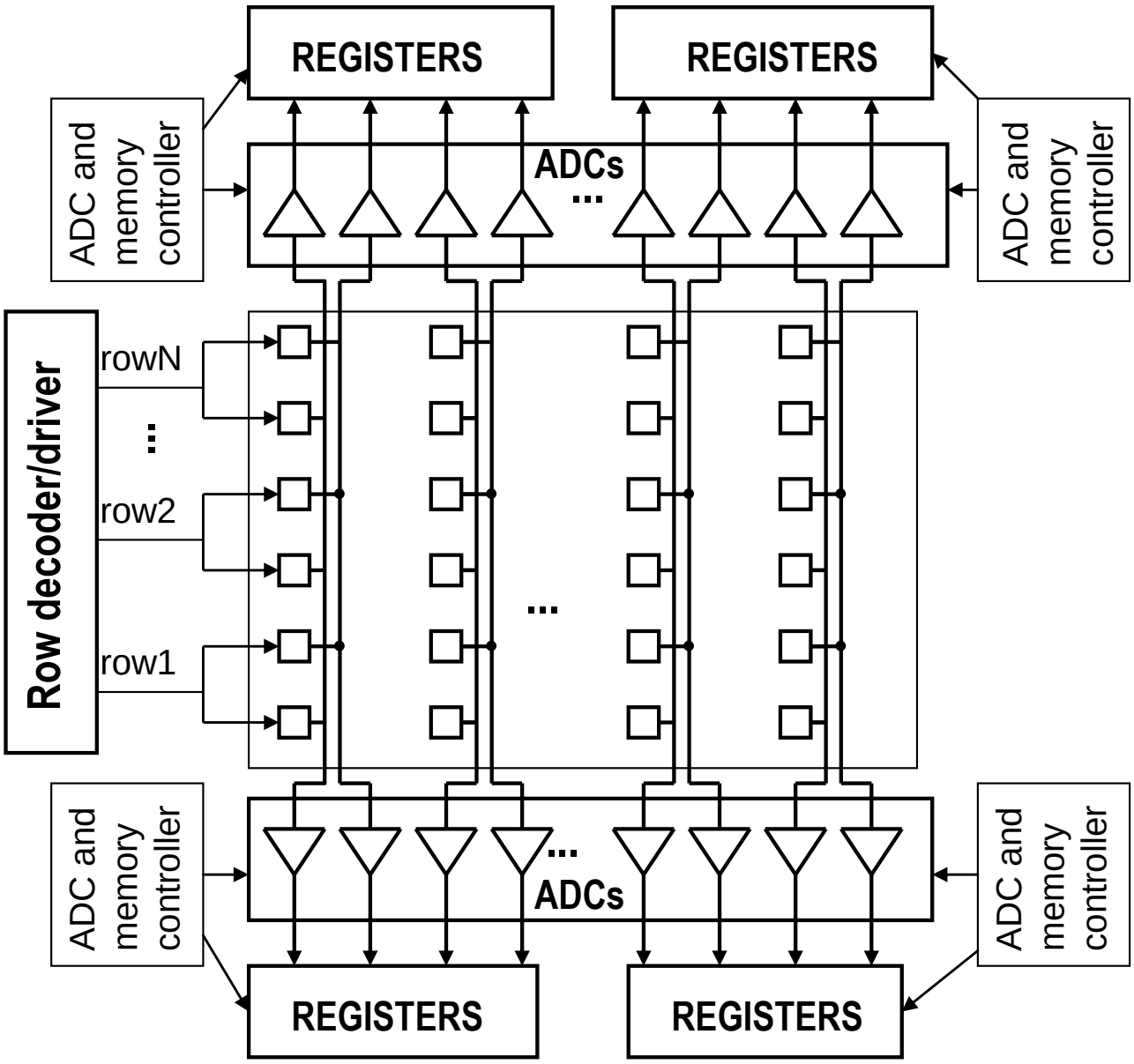


Fig. 1.0. AM1X5 Sensor high speed architecture.

The sensor has two column readout blocks (on top and in the bottom) which include amplifier circuits, ADCs utilizing SAR (successive-approximation) method, and Register block where the ADC data is temporarily stored for readout. The readout from the SAR registers as well as the sensor controls are arranged as a 4 quadrant readout & control architecture, which allows local control over SAR ADCs and local data readout, both essential for high speed operation of the sensor. The sensor also has some biases and all current sources generated internally. Although, many critical voltages to this chip are required to be generated externally.

2.0 PIXEL ARRAY

There are total of 1028x1026 pixels including 1014x1024 active pixels, 2 dark row and 14 dark column readable pixels, 7 on each side. Other boundary pixels are not readable and serve only for reducing of an edge effect in the response uniformity of the active pixels. A drawing of the pixel array is sketched in Fig.2.

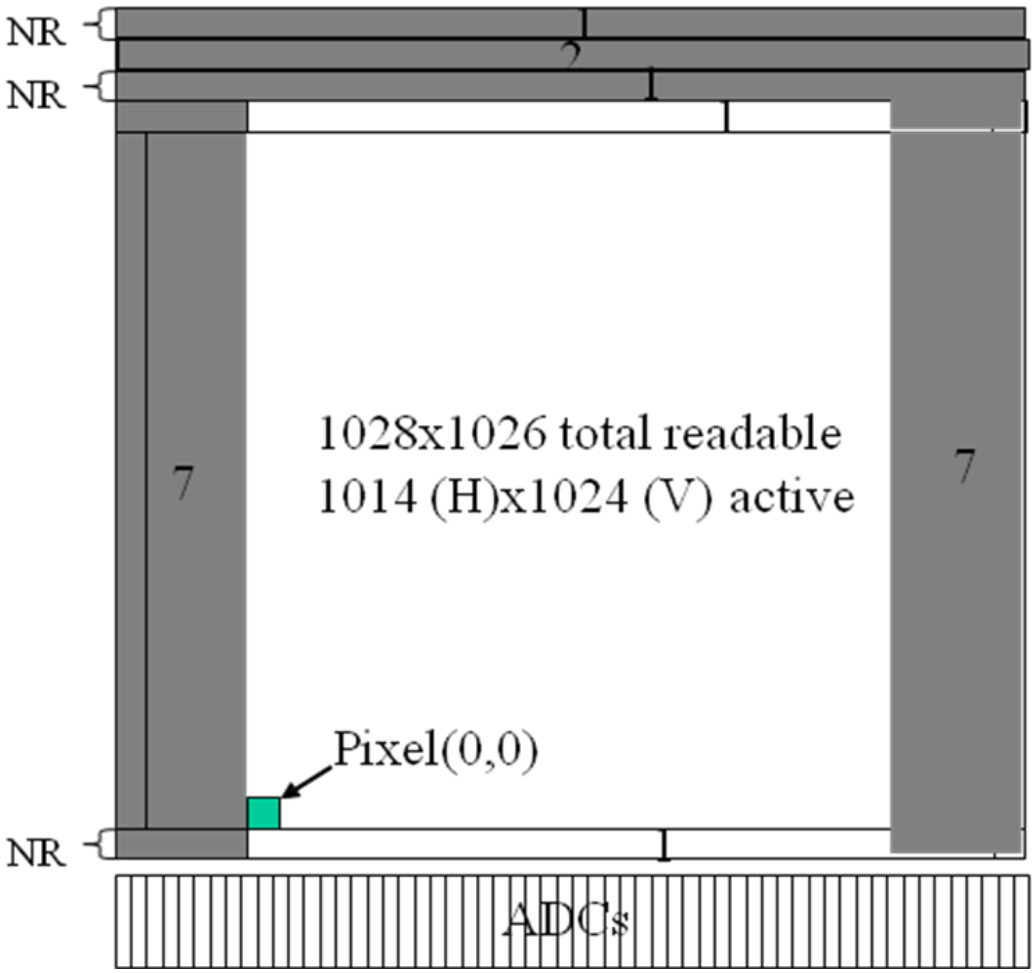


Fig.2. Pixel Array

3.0 PIXEL AND GLOBAL SHUTTER CONTROLS

Pixel is a 5T (five transistor) shutter pixel with simplified schematic presented in Fig.3.
The pixel needs two controls *TX_n, and PD_n* to operate the global shutter. The controls work as follows:

- *'PD_n' ("low")* makes the reset of the photodetector PD through AB gate
- *'TX_n' ("low")* makes the transfer of charge from the photodetector PD to the pixel memory FD

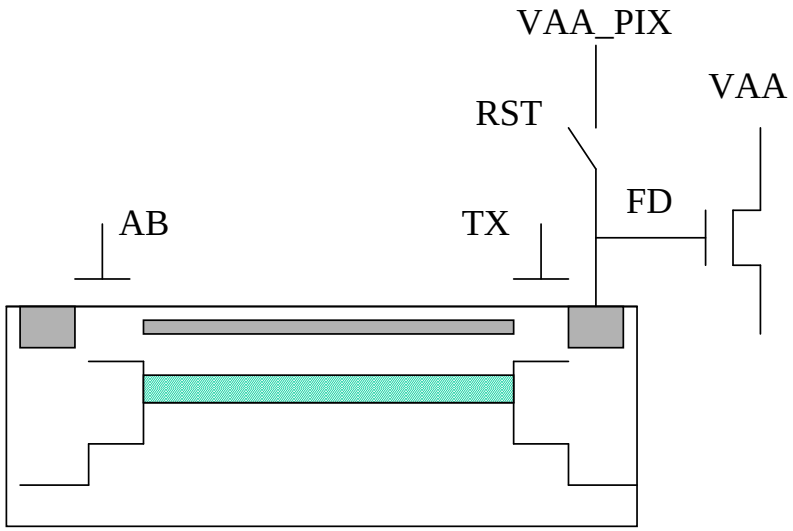


Fig.3. Simplified Topology of the Shutter Pixel

During the signal readout from the pixel the sensor control block generate an internal sequence of pulses. These operations include the readout of the signal stored at FD node, reset of the pixel using RST control (local to the row selected for readout), and reading out the signal corresponding to the reset pixel.

4.0 TIMING IN CONTINUOUS MODE

Sensor controls assume an external row addressing (row1- row10) using a simple binary encoding. The addresses corresponding to the active pixels are the ones 0 through 1023. The addresses of the dark rows are 1024 through 1025. The row address bit row0 normally used in other high speed sensors of MV- and AM- families is not needed for this sensor because the addressing is made in double rows. To read from the selected (double) row of pixels and perform A-to-D over pixel signals, one needs to send a Start Row control "st_row_nb". Reading out one

pixel (double) row and the digitization take certain number of clocks. This number is matched to the number of clocks needed to transfer all the digital data out of the chip. So, after the digitization of the pixel signals from the first row is completed, one may send the control Start Read ("st_read_nb") to read the digital data out. The Start Row pulse "st_row_nt" for the even double row is applied in the middle of the previous (odd) row cycle, as drawn in Fig.4-5. In other words, the row operations for the bottom readout and the top readout are interleaved.

Regarding the data readout, the bottom/top can operate either in interleaved mode (Fig.4a) or in parallel (Fig.4b). Both modes needs to be tried to find the best sensor/camera operation.

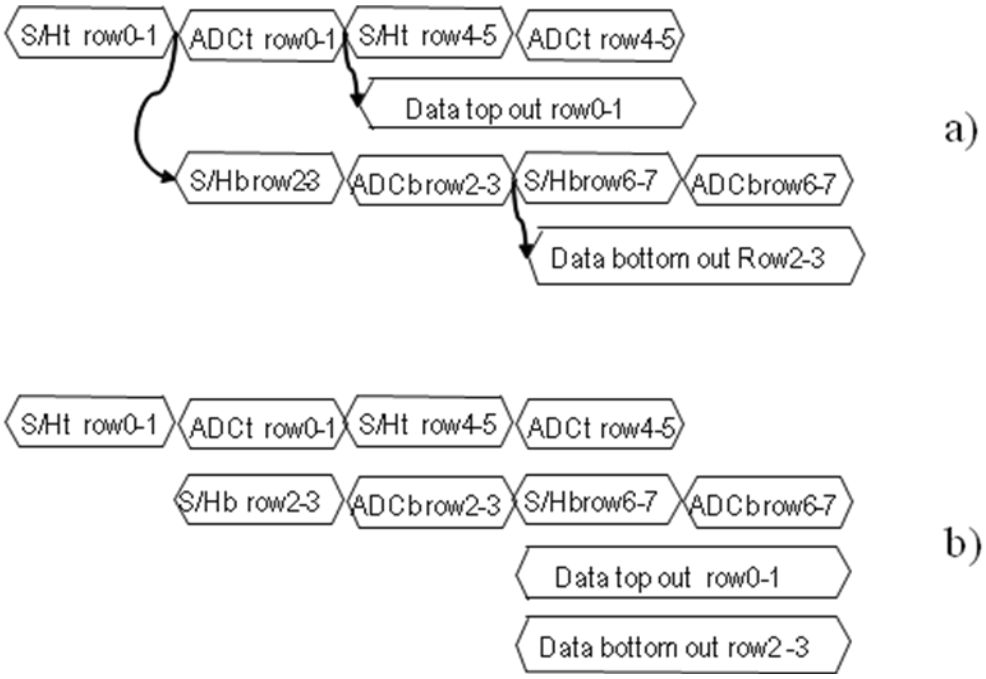


Fig.4. Relationship between Top/Bottom Row Operations (Pixel Sample/Hold and ADC), and the Data Readout operations for two possible readout schemes

In more detail, the timing for the row and the readout controls (only case 4a) is drawn for simplicity, is presented in Fig.5.

The readout rolls row after row, and these controls present in all rows except for the first one (when Start Read is not needed; no ADC data yet) and the last one (when another Start Row is no longer needed, but Start Read still needs to be applied to read out the ADC data from the last row).

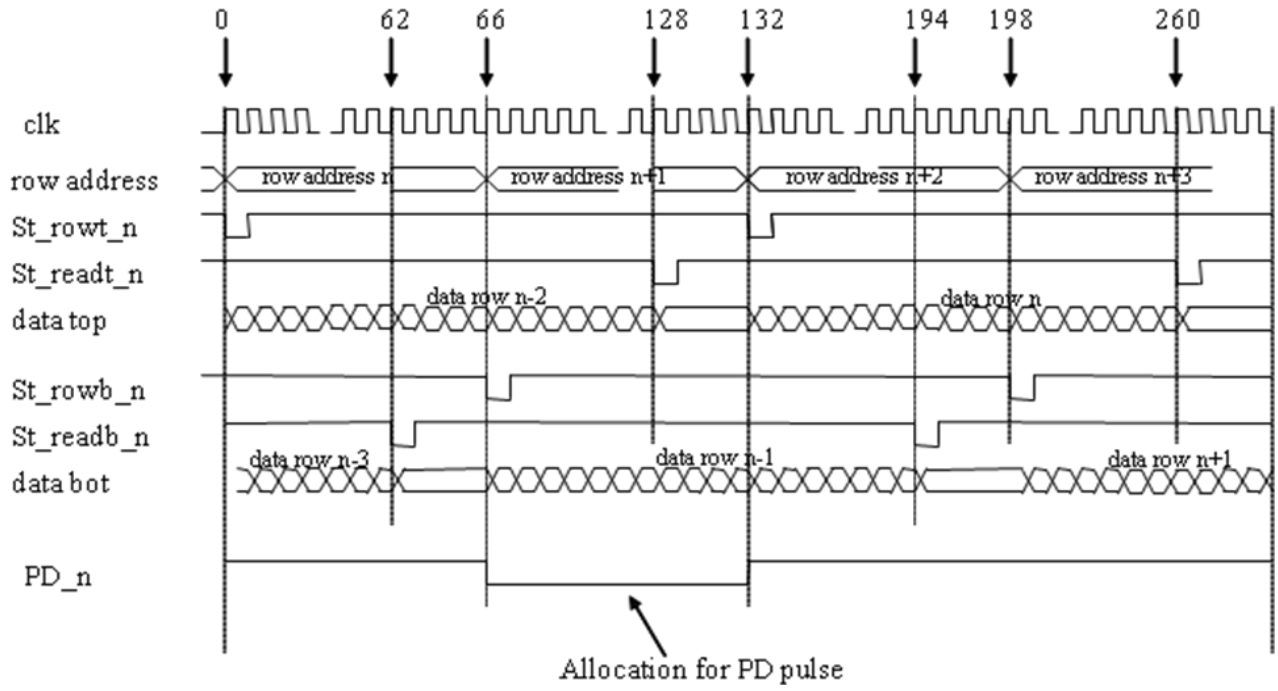


Fig.5. Example of row timing controls.

Frame timing is completed with the allocation of the pixel global controls as follows. The shutter width is defined by the time interval between the global PD_n pulse and the global TX_n pulse. The recommended timing for TX_n pulse is in the last row of the continuously rolling frames. The position of PD_n pulse is somewhere within the frame timing, and the best position should be found experimentally. PD_n control when overlaps with the readout of the particular row, does not affect the row readout directly. However, it may cause the appearance of a “shutter line”. The shutter line is believed through the capacitive feedthrough from the photodiode PD to the shutter node FD. One attempt to remove the shutter line is to make PD covering the entire S/H cycle, as drawn in Fig.5. This makes the crosstalk even between the pixel SHS and SHR cycles.

The sensor has the PD control split for odd and even rows PD_n and PD2_n. This allows for two different exposure times for odd and even rows.

We recommend the following relationship between Start_row and Start_read.

- Recommended semi-row width is 68 clocks minimum instead of 66 drawn. 70 gives a better result, and 72 clocks is even better
- We recommend to send Start_row 2 clocks After the address change. This reduces the chance of having static horizontal lines in the image at left-right.
- We recommend to send Start_read for the corresponding output at the clock 62. Please adjust this in your system for better noise result.

5.0 TIMING IN SEQUENTIAL (EXTERNAL TRIGGER) MODE

After power up and after a long (>10 ms) pause, the sensor pixel readout nodes FD need to be cleared by running at least one void frame readout cycle.

To start the exposure with an external trigger command, one should apply LOW to PD_n and PD2_n controls for 16-32 clock cycles. The rising edge of PD(PD2) starts the exposure.

The exposure is ended with applying LOW TX_n command to transfer the photo-charges to the sensor readout nodes FD.

A full readout cycle follows up to sample one frame of the image.

6.0 OUTPUT PORTS

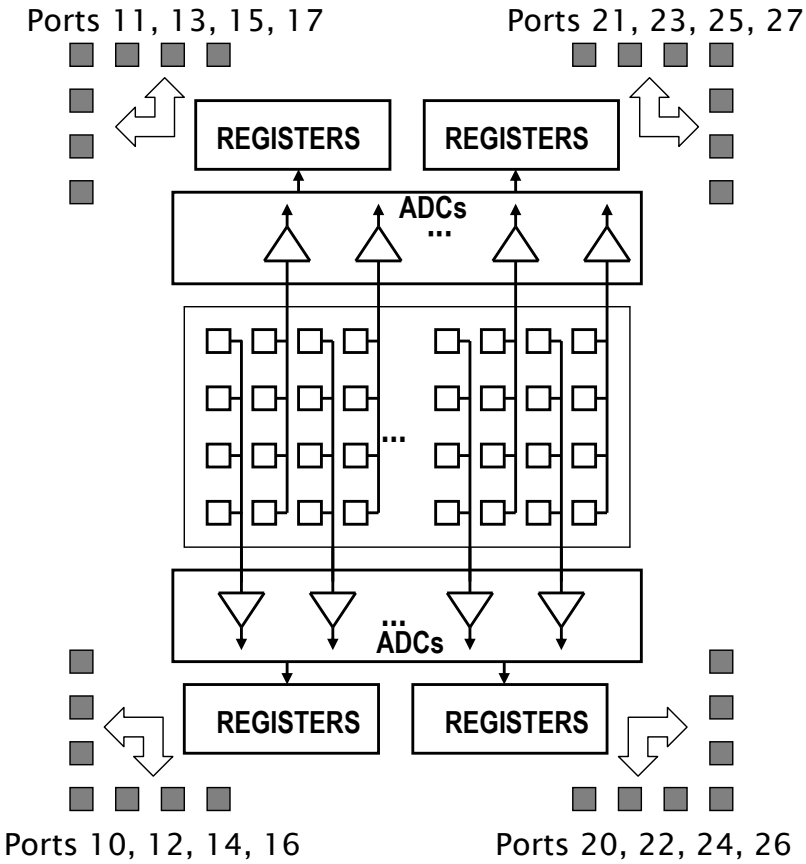


Fig.7. Output ports

AM40 has 16 double data rate ports 10 bit each. The data registers which store the ADC data are split into the left and the right ones, so that the left data registers serve only the left half of the

pixel array columns, and the right – only the right ones. This was done as a measure to speed up the data readout from the registers, avoiding very long bit lines.

A schematic drawing of the output port architecture is drawn in Fig.7.

7.0 SENSOR CONTROLS

7.1. Overview

There are four sensor control blocks in the four corners of the chip. The two upper control blocks serve the upper readout, the two bottom control blocks serve the bottom readout. The upper internal controls are somewhat autonomous from the bottom controls. Small timing misalignment between the top and the bottom internal control pulses shall not cause any conflict of drivers. But, there shall be good symmetry of operation between the left and the right controllers, because they are driving the pixel array and column ADCs from both sides. To facilitate this symmetry, the chip master clock is split into the *clk_top* and *clk_bot* serving the top and the bottom of the chip, respectively. Also, the clock pads are placed in the middle of the pad ring (at the top, and bottom) to built a clock tree which is left-right symmetrical.

To reduce the power consumption and increase reliability of controls, the internal controls are generated from the Clock divided by two. To synchronize the divided clock with external controls, an access to the divider reset is provided. Pin DIV_RB serves as an asynchronous reset bar control over two frequency dividers. A short 1-2 clock LOW pulse once a row or once a frame is OK to synchronize the counter.

Row driver is placed on one both sides of the chip, but the global shutter controls PD_n, PD2_n, and TX_n are on one side of the chip. To insure these controls come to the row drivers simultaneously, they are registered. However, if the setup time for these controls is too short, the controls after registering may get split by 1 clock cycle. This may cause some shutter artifacts, so we need to set up the setup time requirement.

Row addressing controls are also registered. For similar reason, they also need a proper setup time.

There are four important controls start_row/read which trigger row operations and readout operations. These pads are on one side of the chip, so the signal propagation time to the left and the right controllers is different. The difference can reach ~ 4 ns. This dictates a long setup time for these two pulses to exclude the situation when the left controller senses the “Start” command one clock earlier than the right controller, which may cause a chip malfunction.

The hold time > 0ns is needed because the clock signal delay may appear to be longer compared to the control delay. The clock signal experiences multi-stage buffering because of the clock tree structure made for this signal. If, for instance, the clock and a control signal are generated in the same FPGA, and the control signal is a derivative of the clock

Serial interface commands and the clock experience long internal delays. These controls use weak drivers over long distances. The clock frequency is recommended to be at least 1/10 of the master clock frequency.

Master Clock. ***Clk_top*** *and* ***Clk_bot*** are 110, 146 or 183 MHz for 3000, 4000, and 5000 Frames/s operation. Duration +-5%. This is essentially the same clock routed to two different pins of the sensor. A symmetric routing between the pins is strongly advised.

7.2. Setup and hold time for essential controls

Definition of setup/hold time is in Fig.4

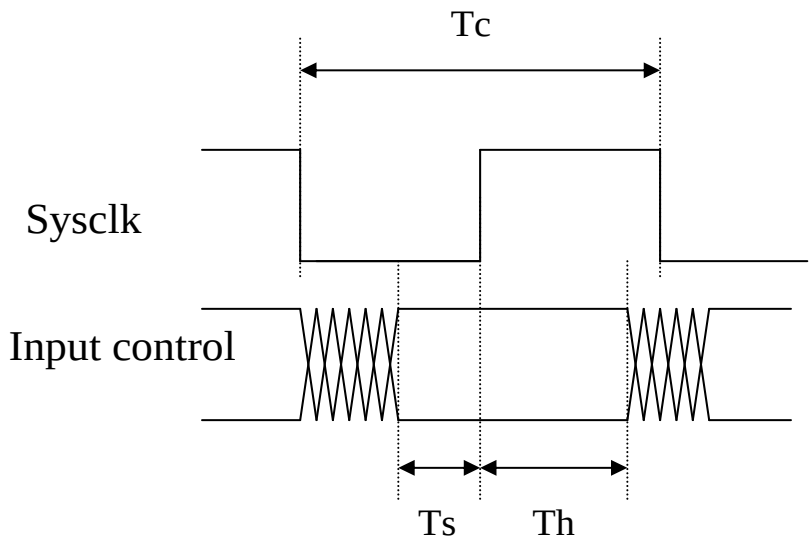


Fig.8.

For input controls st_row_n, st_read_n, use the following table

	Min	Typical	Max
Setup time Ts	4 ns		Tc- 1 ns
Hold time Th	0 ns	1 ns	

For input controls PD_n, PD2_n, TX_n and row addresses Rad1-Rad10 use the following table

	Min	Typical	Max
Setup time Ts	4 ns		Tc- 1 ns
Hold time Th	0 ns	1 ns	

The parameters of Lrst_n, Standby_n, are not critical.

The requirements to the timing of the serial interface are considered later.

Output data delay time with respect to the rising edge of clk_top, clk_bot.

	Min	Typical	Max
Data delay time Td*	1ns	2ns	4ns

*Load capacitance 10 pF and less

Both clock edges of the original clock might be tried to sample the data

8.0 DIGITAL I/O PADS ABSOLUTE RATINGS

A standard I/O library of 2.5V 0.25um UMC pads with 3.3V tolerance was acquired for AM1X5. The pads have the following ratings:

	Operating condition	Min	Typ	Max
VDDIO	I/O Power, operating ratings	2.0V	2.25V	2.5V
VDDIO	I/O Power, absolute maximum ratings	-0.3V		2.9V
	Input digital I/O pads, logic LOW level	-0.3V	0V	+0.5V
	Input digital I/O pads, logic HIGH level	2.25V	2.5V	+3.3V
	Input digital I/O pads, absolute maximum ratings	-0.3V		+4.0V
	Output digital I/O pads, logic LOW level	-0.3V	0V	+0.5V
	Output digital I/O pads, logic HIGH level	2.25V	2.5V	+2.75V

9.0 PIN LIST (36mm size 280uPGA, old style)

Bond pad	Package pin	Name	Comments
1	D4	d15out2	
2	B2	d15out1	
3	C3	VDDIO	
4	A1	GNDK	
5	C2	VDDK	
6	B1	d15out0	
7	D3	AGND	
8	C1	VAA	
9	E3	VADL	AGND
10	D1	VADH	
11	F3	AGND	
12	E1	VAA	
13	G3	VRSTL	
14	F1	d17out9	
15	D2	d17out8	
16	G1	d17out7	
17	H3	d17out6	
18	H1	VSSIO	
19	E2	d17out5	
20	J1	d17out4	
21	J3	d17out3	
22	K2	d17out2	
23	H2	VDDIO	
24	K1	d17out1	
25	K3	d17out0	
26	L2	TX_n	
27	J2	PD_n	
28	L1	rad10	
29	L3	rad8	
30	M2	rad6	
31	G2	rad4	
32	M1	rad2	
33	M3	St_readt_n	
34	N2	VSSIO	

35	F2	VDDIO	
36	N1	GNDK	
37	N3	VDDK	
38	P2	rad1	
39	P3	rad3	
40	P1	rad5	
41	R3	rad7	
42	R2	rad9	
43	X2	St_readb_n	
44	R1	lrst_n	
45	T3	PD2_n	
46	T2	d16out0	
47	W2	d16out1	
48	T1	VDDIO	
49	U3	d16out2	
50	U2	d16out3	
51	Y2	d16out4	
52	U1	d16out5	
53	V3	VSSIO	
54	V2	d16out6	
55	AA2	d16out7	
56	V1	d16out8	
57	W3	d16out9	
58	W1	VRSTH	
59	X3	VAA	
60	X1	AGND	
61	Y3	VADH	
62	Y1	VADL	AGND
63	AA3	VAA	
64	AA1	AGND	
65	AB2	d14out0	
66	AB1	VDDK	
67	AB3	GNDK	
68	AC1	VDDIO	
69	AC2	d14out1	
70	AD1	d14out2	
71	AB4	d14out3	
72	AD2	VDDK	
73	AC3	GNDK	
74	AE1	d14out4	
75	AD3	VSSIO	
76	AE2	d14out5	
77	AC4	d14out6	
78	AE3	d14out7	
79	AC5	d14out8	
80	AE4	d14out9	
81	AC6	VDDIO	

82	AE5	d12out0	
83	AC7	d12out1	
84	AE6	d12out2	
85	AD4	d12out3	
86	AE7	d12out4	
87	AC8	VSSIO	
88	AE8	d12out5	
89	AD5	d12out6	
90	AE9	d12out7	
91	AC9	d12out8	
92	AD10	d12out9	
93	AD8	VDDIO	
94	AE10	d10out0	
95	AC10	d10out1	
96	AD11	d10out2	
97	AD9	d10out3	
98	AE11	d10out4	
99	AC11	VSSIO	
100	AD12	d10out5	
101	AD7	d10out6	
102	AE12	d10out7	
103	AC12	d10out8	
104	AD13	d10out9	
105	AD6	VDDIO	
106	AE13	clk_bot	
107	AC13	d20out9	
108	AD14	d20out8	
109	AC14	d20out7	
110	AE14	d20out6	
111	AC15	d20out5	
112	AD15	VSSIO	
113	AD20	d20out4	
114	AE15	d20out3	
115	AC16	d20out2	
116	AD16	d20out1	
117	AD19	d20out0	
118	AE16	VDDIO	
119	AC17	d22out9	
120	AD17	d22out8	
121	AD21	d22out7	
122	AE17	d22out6	
123	AC18	d22out5	
124	AD18	VSSIO	
125	AD22	d22out4	
126	AE18	d22out3	
127	AC19	d22out2	
128	AE19	d22out1	

129	AC20	d22out0	
130	AE20	VDDIO	
131	AC21	d24out9	
132	AE21	d24out8	
133	AC22	d24out7	
134	AE22	d24out6	
135	AD23	d24out5	
136	AE23	VSSIO	
137	AC23	d24out4	
138	AE24	GNDK	
139	AD24	VDDK	
140	AE25	d24out3	
141	AB23	d24out2	
142	AD25	d24out1	
143	AC24	VDDIO	
144	AE26	GNDK	
145	AC25	VDDK	
146	AD26	d24out0	
147	AB24	AGND	
148	AC26	VAA	
149	AA24	VADL	AGND
150	AB26	VADH	
151	Y24	AGND	
152	AA26	VAA	
153	X24	VAA_PIX	
154	Y26	d26out9	
155	AB25	d26out8	
156	X26	d26out7	
157	W24	d26out6	
158	W26	VSSIO	
159	AA25	d26out5	
160	V26	d26out4	
161	V24	d26out3	
162	U25	d26out2	
163	W25	VDDIO	
164	U26	d26out1	
165	U24	d26out0	
166	T25	St_rowb_n	
167	V25	sdata	
168	T26	sclk	
169	T24	Tr_en	
170	R25	VLNT	
171	X25	VMUX1	
172	R26	VMUX2	
173	R24	VOFF	
174	P25	VLP	CONNECT TO VAA

175	Y25	AGND	
176	P26	VAA	
177	P24	VRSTH	
178	N25	VAD2	
179	N24	VREF	CONNECT TO VAA
180	N26	VLN	
181	M24	VABL_TST	
182	M25	St_rowt_n	
183	G25	Div_rb	
184	M26	OE	
185	L24	standby_n	
186	L25	d27out0	
187	H25	d27out1	
188	L26	VDDIO	
189	K24	d27out2	
190	K25	d27out3	
191	F25	d27out4	
192	K26	d27out5	
193	J24	VSSIO	
194	J25	d27out6	
195	E25	d27out7	
196	J26	d27out8	
197	H24	d27out9	
198	H26	VAA_PIX	
199	G24	VAA	
200	G26	AGND	
201	F24	VADH	
202	F26	VADL	AGND
203	E24	VAA	
204	E26	AGND	
205	D25	d25out0	
206	D26	VDDK	
207	D24	GNDK	
208	C26	VDDIO	
209	C25	d25out1	
210	B26	d25out2	
211	D23	d25out3	
212	B25	VDDK	
213	C24	GNDK	
214	A26	d25out4	
215	B24	VSSIO	
216	A25	d25out5	
217	C23	d25out6	
218	A24	d25out7	
219	C22	d25out8	
220	A23	d25out9	

221	C21	VDDIO	
222	A22	d23out0	
223	C20	d23out1	
224	A21	d23out2	
225	B23	d23out3	
226	A20	d23out4	
227	C19	VSSIO	
228	A19	d23out5	
229	B22	d23out6	
230	A18	d23out7	
231	C18	d23out8	
232	B17	d23out9	
233	B19	VDDIO	
234	A17	d21out0	
235	C17	d21out1	
236	B16	d21out2	
237	B18	d21out3	
238	A16	d21out4	
239	C16	VSSIO	
240	B15	d21out5	
241	B20	d21out6	
242	A15	d21out7	
243	C15	d21out8	
244	B14	d21out9	
245	B21	clk_top	
246	A14	VDDIO	
247	C14	d11out9	
248	B13	d11out8	
249	C13	d11out7	
250	A13	d11out6	
251	C12	d11out5	

252	B12	VSSIO	
253	B7	d11out4	
254	A12	d11out3	
255	C11	d11out2	
256	B11	d11out1	
257	B8	d11out0	
258	A11	VDDIO	
259	C10	d13out9	
260	B10	d13out8	
261	B6	d13out7	
262	A10	d13out6	
263	C9	d13out5	
264	B9	VSSIO	
265	B5	d13out4	
266	A9	d13out3	
267	C8	d13out2	
268	A8	d13out1	
269	C7	d13out0	
270	A7	VDDIO	
271	C6	d15out9	
272	A6	d15out8	
273	C5	d15out7	
274	A5	d15out6	
275	B4	d15out5	
276	A4	VSSIO	
277	C4	d15out4	
278	A3	GNDK	
279	B3	VDDK	
280	A2	d15out3	

9.1 PIN LIST (28mm size 280uPGA, small size)

Bond pad	Package pin	Name	Comments
1	A2	d15out2	
2	C2	d15out1	
3	B2	VDDIO	
4	A1	GNDK	
5	D2	VDDK	
6	B1	d15out0	
7	C1	AGND	
8	C3	VAA	

9	D3	VADL	AGND
10	E2	VADH	
11	D1	AGND	
12	D4	VAA	
13	E1	VRSTL	
14	E3	d17out9	
15	F2	d17out8	
16	E4	d17out7	
17	F3	d17out6	
18	F1	VSSIO	

19	G2	d17out5	
20	F4	d17out4	
21	G3	d17out3	
22	G1	d17out2	
23	G4	VDDIO	
24	H2	d17out1	
25	H3	d17out0	
26	H4	TX_n	
27	H1	PD_n	
28	J3	rad10	
29	J2	rad8	
30	J4	rad6	
31	J1	rad4	
32	K4	rad2	
33	K2	St_readt_n	
34	K3	VSSIO	
35	K1	VDDIO	
36	L1	GNDK	
37	L3	VDDK	
38	L2	rad1	
39	L4	rad3	
40	M1	rad5	
41	M4	rad7	
42	M2	rad9	
43	M3	St_readb_n	
44	N1	lrst_n	
45	N4	PD2_n	
46	N3	d16out0	
47	N2	d16out1	
48	P4	VDDIO	
49	P1	d16out2	
50	P3	d16out3	
51	R4	d16out4	
52	P2	d16out5	
53	R1	VSSIO	
54	R3	d16out6	
55	T4	d16out7	
56	R2	d16out8	
57	T3	d16out9	
58	T1	VRSTH	
59	U4	VAA	
60	U1	AGND	
61	T2	VADH	
62	U3	VADL	AGND
63	V3	VAA	
64	V1	AGND	
65	W1	d14out0	

66	U2	VDDK	
67	Y1	GNDK	
68	W2	VDDIO	
69	V2	d14out1	
70	Y2	d14out2	
71	W3	d14out3	
72	Y3	VDDK	
73	W4	GNDK	
74	Y4	d14out4	
75	V4	VSSIO	
76	V5	d14out5	
77	Y5	d14out6	
78	W5	d14out7	
79	U5	d14out8	
80	T5	d14out9	
81	W6	VDDIO	
82	Y6	d12out0	
83	V6	d12out1	
84	U6	d12out2	
85	T6	d12out3	
86	T7	d12out4	
87	Y7	VSSIO	
88	W7	d12out5	
89	V7	d12out6	
90	U7	d12out7	
91	T8	d12out8	
92	U8	d12out9	
93	Y8	VDDIO	
94	W8	d10out0	
95	V8	d10out1	
96	T9	d10out2	
97	U9	d10out3	
98	Y9	d10out4	
99	W9	VSSIO	
100	V9	d10out5	
101	T10	d10out6	
102	U10	d10out7	
103	Y10	d10out8	
104	W10	d10out9	
105	V10	VDDIO	
106	V11	clk_bot	
107	W11	d20out9	
108	Y11	d20out8	
109	U11	d20out7	
110	T11	d20out6	
111	V12	d20out5	
112	W12	VSSIO	

113	Y12	d20out4	
114	U12	d20out3	
115	T12	d20out2	
116	V13	d20out1	
117	W13	d20out0	
118	Y13	VDDIO	
119	U13	d22out9	
120	T13	d22out8	
121	U14	d22out7	
122	V14	d22out6	
123	W14	d22out5	
124	Y14	VSSIO	
125	T14	d22out4	
126	T15	d22out3	
127	U15	d22out2	
128	V15	d22out1	
129	Y15	d22out0	
130	W15	VDDIO	
131	T16	d24out9	
132	U16	d24out8	
133	W16	d24out7	
134	Y16	d24out6	
135	V16	d24out5	
136	V17	VSSIO	
137	Y17	d24out4	
138	W17	GNDK	
139	Y18	VDDK	
140	W18	d24out3	
141	Y19	d24out2	
142	V19	d24out1	
143	W19	VDDIO	
144	Y20	GNDK	
145	U19	VDDK	
146	W20	d24out0	
147	V20	AGND	
148	V18	VAA	
149	U18	VADL	AGND
150	T19	VADH	
151	U20	AGND	
152	U17	VAA	
153	T20	VAA_PIX	
154	T18	d26out9	
155	R19	d26out8	
156	T17	d26out7	
157	R18	d26out6	
158	R20	VSSIO	
159	P19	d26out5	

160	R17	d26out4	
161	P18	d26out3	
162	P20	d26out2	
163	P17	VDDIO	
164	N19	d26out1	
165	N18	d26out0	
166	N17	St_rowb_n	
167	N20	sdata	
168	M18	sclk	
169	M19	Tr_en	
170	M17	VLNT	
171	M20	VMUX1	
172	L17	VMUX2	
173	L19	VOFF	
174	L18	VLP	CONNECT TO VAA
175	L20	AGND	
176	K20	VAA	
177	K18	VRSTH	
178	K19	VAD2	
179	K17	VREF	CONNECT TO VAA
180	J20	VLN	
181	J17	VABL_TST	
182	J19	St_rowt_n	
183	J18	Div_rb	
184	H20	OE	
185	H17	standby_n	
186	H18	d27out0	
187	H19	d27out1	
188	G17	VDDIO	
189	G20	d27out2	
190	G18	d27out3	
191	F17	d27out4	
192	G19	d27out5	
193	F20	VSSIO	
194	F18	d27out6	
195	E17	d27out7	
196	F19	d27out8	
197	E18	d27out9	
198	E20	VAA_PIX	
199	D17	VAA	
200	D20	AGND	
201	E19	VADH	
202	D18	VADL	AGND
203	C18	VAA	
204	C20	AGND	

205	B20	d25out0	
206	D19	VDDK	
207	A20	GNDK	
208	B19	VDDIO	
209	C19	d25out1	
210	A19	d25out2	
211	B18	d25out3	
212	A18	VDDK	
213	B17	GNDK	
214	A17	d25out4	
215	C17	VSSIO	
216	C16	d25out5	
217	A16	d25out6	
218	B16	d25out7	
219	D16	d25out8	
220	E16	d25out9	
221	B15	VDDIO	
222	A15	d23out0	
223	C15	d23out1	
224	D15	d23out2	
225	E15	d23out3	
226	E14	d23out4	
227	A14	VSSIO	
228	B14	d23out5	
229	C14	d23out6	
230	D14	d23out7	
231	E13	d23out8	
232	D13	d23out9	
233	A13	VDDIO	
234	B13	d21out0	
235	C13	d21out1	
236	E12	d21out2	
237	D12	d21out3	
238	A12	d21out4	
239	B12	VSSIO	
240	C12	d21out5	
241	E11	d21out6	
242	D11	d21out7	
243	A11	d21out8	

244	B11	d21out9	
245	C11	clk_top	
246	C10	VDDIO	
247	B10	d11out9	
248	A10	d11out8	
249	D10	d11out7	
250	E10	d11out6	
251	C9	d11out5	
252	B9	VSSIO	
253	A9	d11out4	
254	D9	d11out3	
255	E9	d11out2	
256	C8	d11out1	
257	B8	d11out0	
258	A8	VDDIO	
259	D8	d13out9	
260	E8	d13out8	
261	D7	d13out7	
262	C7	d13out6	
263	B7	d13out5	
264	A7	VSSIO	
265	E7	d13out4	
266	E6	d13out3	
267	D6	d13out2	
268	C6	d13out1	
269	A6	d13out0	
270	B6	VDDIO	
271	E5	d15out9	
272	D5	d15out8	
273	B5	d15out7	
274	A5	d15out6	
275	C5	d15out5	
276	C4	VSSIO	
277	A4	d15out4	
278	B4	GNDK	
279	A3	VDDK	
280	B3	d15out3	

10. PIN DESCRIPTION

Data out *(16 x 10 pins)*- digital output. Format: *d*-n-*out*-m e.g. *d5o4*, where n is the number of the port, m denotes the bit significance: m=9 is MSB, m=0 is LSB.

The data from 4 neighboring columns and 2 rows is packed according to the following diagrams: The data changes twice per clock

	Port 10 (20)	Port 12 (22)	Port 14 (24)	Port 16 (26)
Clk = ‘0’	Col 2 row 0	Col 0 row 0	Col 2 row 1	Col 0 row 1
Clk = ‘1’	Col 3 row 0	Col 1 row 0	Col 3 row 1	Col 1 row 1

Period of columns =4. This means Port 12 also outputs columns 0, 4, 8 …+4*n at Low clock and columns 1, 5, 9 ..+4*n at High wave of the clock. Et cetera.

Output data I/O pads are tri-stated SSTL-2 pads. Output is enable by applying HIGH to the *OE* pad

VDDIO and ***VSSIO*** – digital I/O power and ground, 2.5V. Instantaneous current driving 160 of 10pF loads may reach +-3A. The current averaged over data period is, theoretically, +-300 mA.

To minimize ground noises you may try VDDIO in the range 1.8V- 2.3V. But the maximum data rate may not be achieved with smaller VDDIO

VDDK and ***GNDK*** – core digital power and ground, 1.8V+-0.18V. Consumption is 1/10 of the above or even less. To increase the data rate from the sensor, try 2.1-2.3V as well at the cost of adding some noise.

VAA and ***AGND*** are analog power and ground. Recommended *VAA* value is to be finalized during the characterization within 3.3V to 3.6V limits. Expected dc current consumption is 150 mA. There will also be a noticeable ac component of ~20-40 mA. It needs good decoupling.

VAA_PIX. Recommended *VAA_PIX* is to be finalized during the sensor characterization within 2.2V to 3.3V.

VADH- ADC High reference voltage, 0.2- 1.0V, nominal =0.7V. Requirements are equivalent to Vref1 voltage in MV-family of high speed sensors. Equivalent circuit: charges a 4 nF capacitor once in a row time. Shall settle within 1 mV for ~20 ns or have pulsations less than 1mV. If row operations stopped (No Start_row_n signals), there is no consumption from this pin.

VADL- connected internally to *AGND*, in this design.

VAD2 –second ADC reference voltage, Shall be ½ of VADH. The requirements are 500X weaker than those to VADH

VABL_TST- this is a double functionality voltage. It serves as a test voltage for ADC and column circuit tests. Shall graduate change from 0 to 1.2V in this mode. Sensor users are not supposed to run these tests. Main function is the row driver anti-blooming voltage. Fixed in the

range 0-1V based on the sensor characterization. Charges a 4pF capacitor few times a row time. The worst loading condition is during global shutter reset. Charges ~2-4 nF capacitor for ~100 ns.

VRSTH- row driver voltage 2.5-3.3V. Default value is to be determined during the sensor characterization. Same loading conditions as for *VABL_TST*. But, the noise from this supply is injected directly to the signal.

VRSTL- Reset gate low voltage. Shall be adjustable within 0- 0.7V. May be helpful to reduce the leakage from FD nodes in the form of white spots in the image.

VREF: REMOVED Please have the option to connect this to AGND or VAA (looks like the preferred)

VOFF- amplitude of the offset voltage added to all columns. The sign is controlled digitally via Bit1 of serial interface. Requirements: 1/100 of those for *VADH*. The range is 0-3.3V. Added to ADC signal with 1/20 attennuation.

VLN – current bias for pixel source follower load; generated internally, may need override. Recommended value is within 0.5V- 0.6V range

VLNT – current bias control for comparator latch may need override. Recommended value is within 0.8V- 1.0V range

VLP- keep at 3.3V in latest revisions of AM1X5. Failure to do so will cause high current consumption!

Biases below are for testing purpose. You may try to leave these floating.

VMUX1- multiplexed pad for external override to the following internal biases:
VCASNA, *VCASVLN*, *VCASN2*, *VCASN3*, all 0.8-1.5V
VMUX2- multiplexed pad for external override of one of the following:
VLN3, VLN2 all 0.8- 2V

11.0. SERIAL INTERFACE DESCRIPTION

Serial interface in AM40 serves two functions: to write in 16 sensor settings and to correct the gain/offset of the column ADCs using a programmable column DACs per column, with local SRAMs.

The sensor settings are written in using the following pins: sdata, sclk, Tr_en.
The per column FPN coefficients are written using the controls: sdata, sclk and WE_n

Serial interface allows to enable/disable 16 sensor setting controls:

Bit0 Col_test_en
Bit1 Offset_sign
Bit2 Gain_2_en: DISABLED
Bit3 Gain_4_en: DISABLED
Bit4 Rowdrv_dis
Bit5 Unipolar_ADC_mode
Bit6 SAR settling ctrl
Bit7 Row_change_en_b
Bit8 Sndrst_n MUST BE "1"WHEN USING FULL DATA INTERFACE
Bit9 VLN_cas_en
Bit10-11 VMUX1: VCASNA, VCASVLN, VCASN2, VCASN3
Bit12-13 VMUX2: VLN3, VLN2
Bit14 ADC_tst_en
Bit15 Gray_enable

Chip logic reset Lrst_n=0 sets all bits to default value of "0"

11.1. Description of the bits

Bit0, Col_test_en: '1' disables pixel readout and enables column test, where pixel signals are substituted with a pair of voltages: VTEST and AGND

Bit1, Offset_sign: The '1' makes the offset negative. '0' keeps it positive. Offset is always enabled in this chip, the value is controlled with VOFF voltage (which translates to ADC input with 20-30 times attenuation)

Bit2, Gain_2_en: CONTROL REMOVED

Bit3, Gain_4_en: CONTROL REMOVED

Bit4, Rdrv_dis: CONTROL REMOVED

Bit5, Unipolar_ADC_mode: This bit switches the chip between two operation modes. The modes relate to unipolar/differential way of processing signals in the column circuits. They may differ by amount of row/column noise. The best one of the two will be selected and recommended for future operation.

Bit6, SAR settling: This control tries two alternative modes to resolve ADC settling timing issues. The best one is selected after trying the both.

Bit7, Row_change_en_b: This control relates to optimization of the pixel FPN. There is a high possibility this control stays at default '0'.

Bit8, Sndrst_en_b: Also, relates to pixel FPN and shutter operation. Will be optimized during the sensor test.

Bit9, VLN_cas_en: This control enables cascoding in the VLN buffer and may reduce one of the column fpn components. By default, it enables the circuit w/o cascoding.

Bit10-11, VMUX1: Connect one of the following internal biases VCASNA (00), VCASVLN (01) , VCASN2 (10), VCASN3 (11) to the common I/O pad VMUX1 for debugging/override purposes. (01) means bit10='1', bit11='0'.

Bit12-13: This controls connect one of the internal biases VLN3 (00) and VLNT (01) to the pad VMUX2.

Bit14, ADC_tst_en: When '1' this control disconnects the ADC from the output of the column amplifier, and substitutes the amp signal with a pair of voltages VTEST and AGND.

Bit15, Gray_enable: High enables Gray encoding for the output data after sensamps. This is expected to reduce the amount of row-wise noise at major transitions.

11.2. Timing of the interface

The serial interface is a D-flop shift register clocked by Sclk. Every rising edge of Sclk samples new Sdata into the register and moves the data written before by 1 bit. 16 Sclks update the entire register. **The bit written first is the bit #15 (the last bit).** For new register data to take effect on the image sensor, one needs to apply a Transfer enable (Tr_en) HIGH pulse, and on the first Low-to-Hign transition of the Clk_top (Clk_bot), the new register data is overwritten into the Digital Block registers.

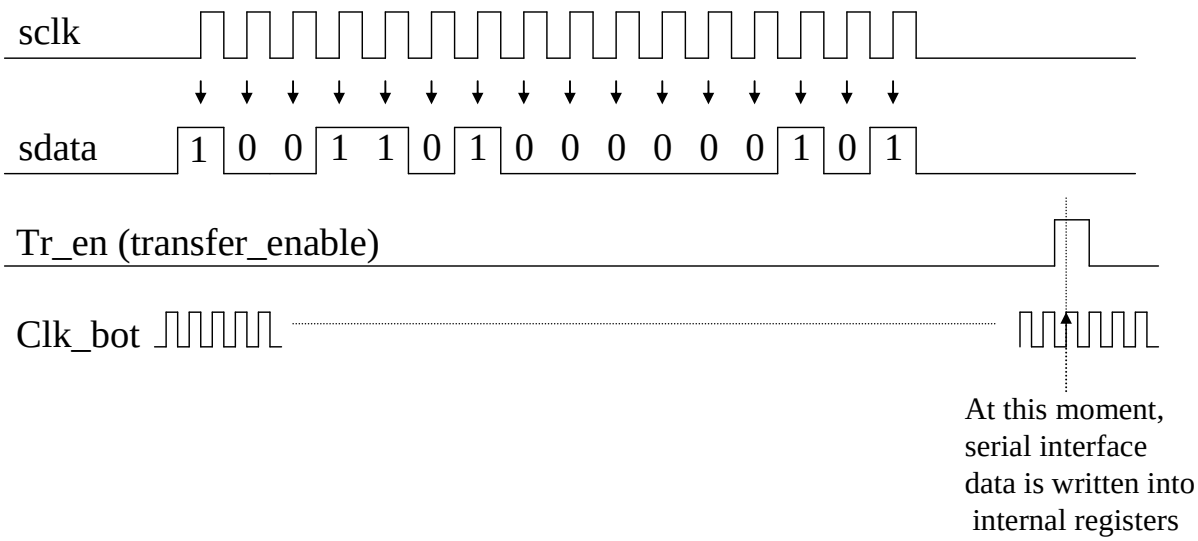
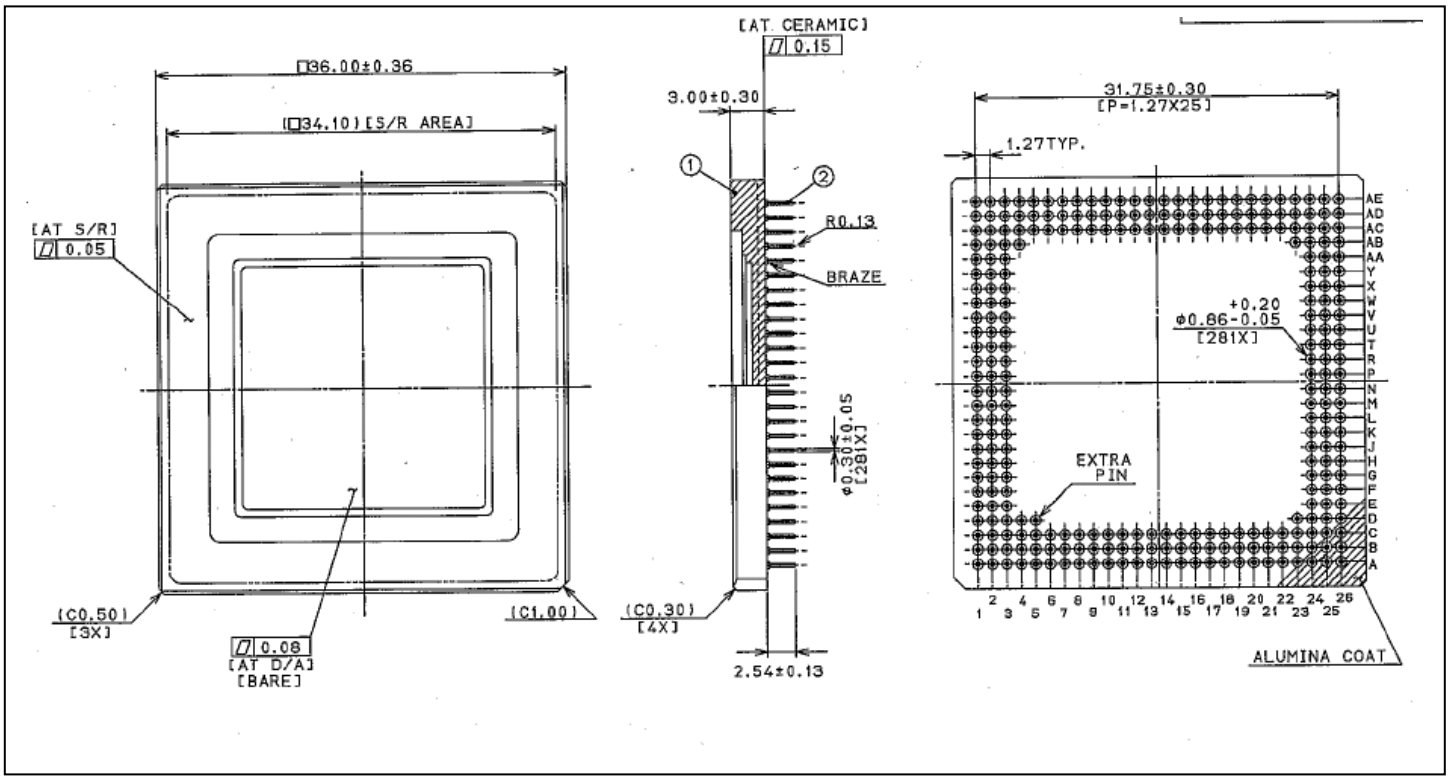


Fig.9. Operation of the serial register to set up the sensor settings

12.0. 36mm PACKAGE (old style)

- AM1X5 is offered in a 1.27mm pitch 280 micro-PGA of ~36mm size.



13.0. 28mm PACKAGE (small size)