SONY

Diagonal 6.43 mm (Type 1/2.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX715-AAQR1-C

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STARVIS

Description

The IMX715-AAQR1-C is a diagonal 6.4 mm (Type 1/2.8) CMOS active pixel type solid-state image sensor with a square pixel array and 8.46 M effective pixels. This chip operates with analog 2.9 V, digital 1.1 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Security cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Input frequency: 24 MHz / 27 MHz / 37.125 MHz / 72 MHz / 74.25 MHz
- ◆Number of recommended recording pixels: 3840 (H) × 2160 (V) approx. 8.29 M pixels
- ◆Readout mode
  - All-pixel scan mode
  - Horizontal/Vertical 2/2-line binning mode
  - Window cropping mode
  - Horizontal / Vertical direction - Normal / Inverted readout mode
- ◆Readout rate
  - Maximum frame rate in
  - All-pixel scan mode: 12-bit: 60.3 frame/s, 10-bit: 90.9 frame/s
- ◆High dynamic range (HDR) function
  - Multiple exposure HDR
  - Digital overlap HDR
- ◆Function of synchronizing sensors
- ◆Variable-speed shutter function (resolution 1H)
- ◆CDS / PGA function
  - 0 dB to 30 dB: Analog Gain 30 dB (step pitch 0.3 dB)
  - 30.3 dB to 72 dB: Analog Gain 30 dB + Digital Gain 0.3 dB to 42 dB (step pitch 0.3 dB)
- ◆Supported I/O
  - CSI-2 serial data output (2-lane / 4-lane), RAW10 / RAW12 output
- ◆AR coating on cover glass (both sides)

E21804A2X

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 6.4 mm (Type 1/2.8) approx. 8.40 M pixels, All pixels
- ◆ Total number of pixels
  3864 (H) × 2228 (V) approx. 8.60 M pixels
- ◆ Number of effective pixels
  3864 (H) × 2192 (V) approx. 8.46 M pixels
- ◆ Number of active pixels
  3864 (H) × 2176 (V) approx. 8.40 M pixels
- ◆ Number of recommended recording pixels
  3840 (H) × 2160 (V) approx. 8.29 M pixels
- ◆ Unit cell size
  1.45 µm (H) × 1.45 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 36 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 1 pixels, rear 1 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog: 2.9 V)	AV_{DD}	-0.3	3.3	V	
Supply voltage (interface: 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital: 1.1 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	
Storage temperature	Tstg	-40	85	˚C	

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog: 2.9 V)	AV_{DD}	2.80	2.90	3.00	V
Supply voltage (interface: 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital: 1.1 V)	DV_{DD}	1.00	1.10	1.20	V
Performance guarantee temperature	Tspec	-10	—	60	˚C

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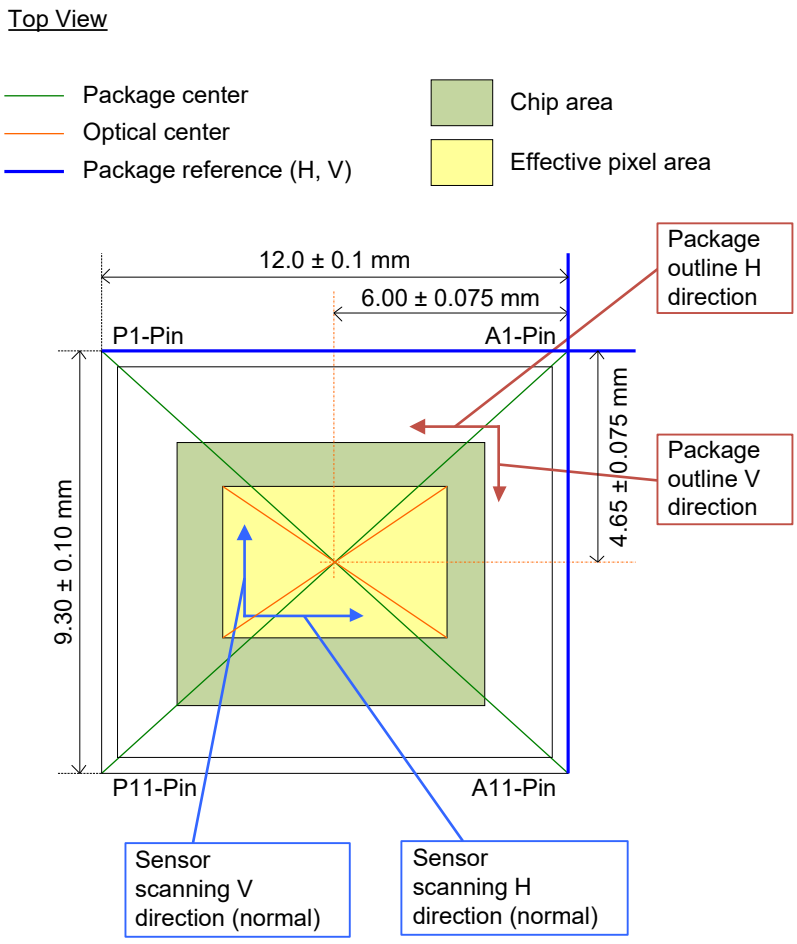
General-0.0.9

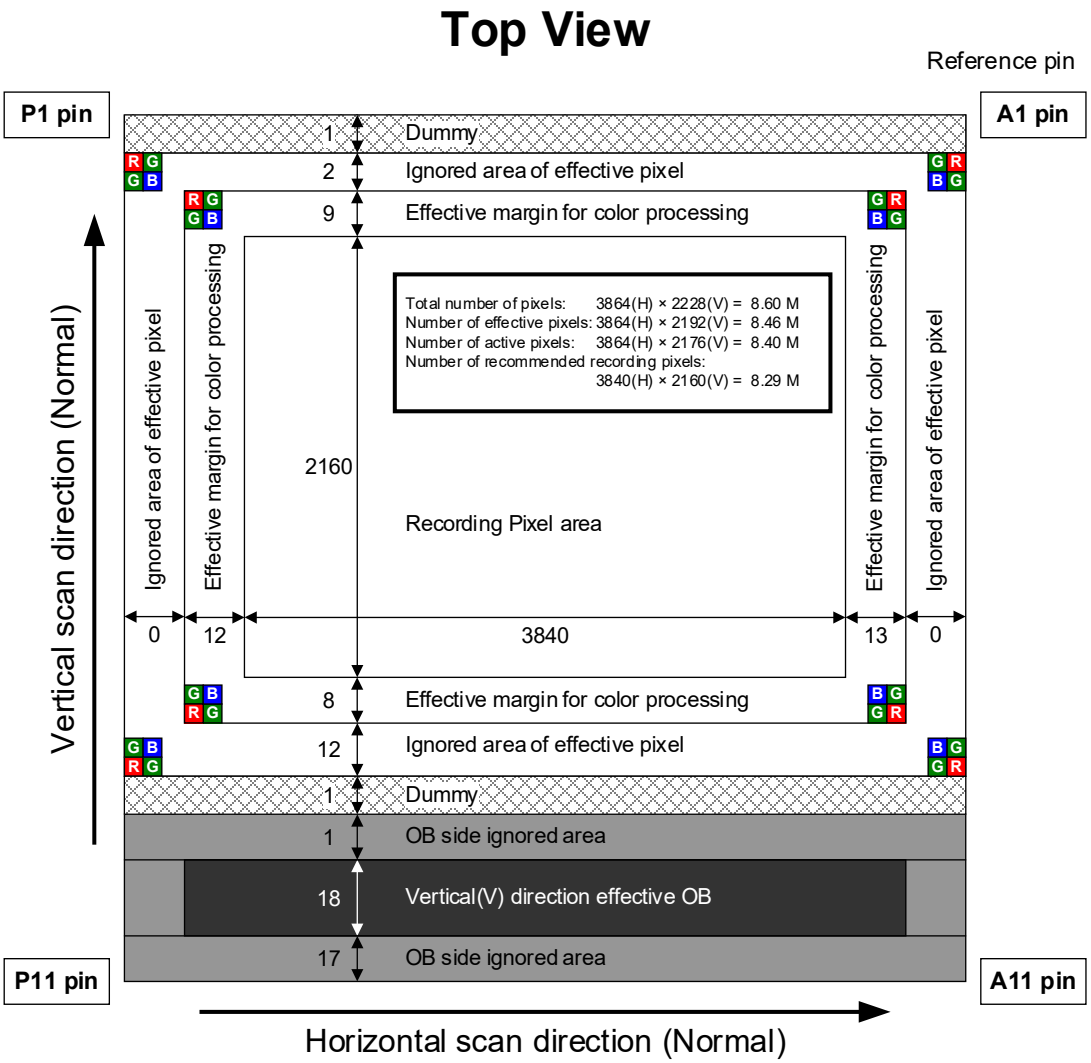
Contents

Optical Center



Optical Center

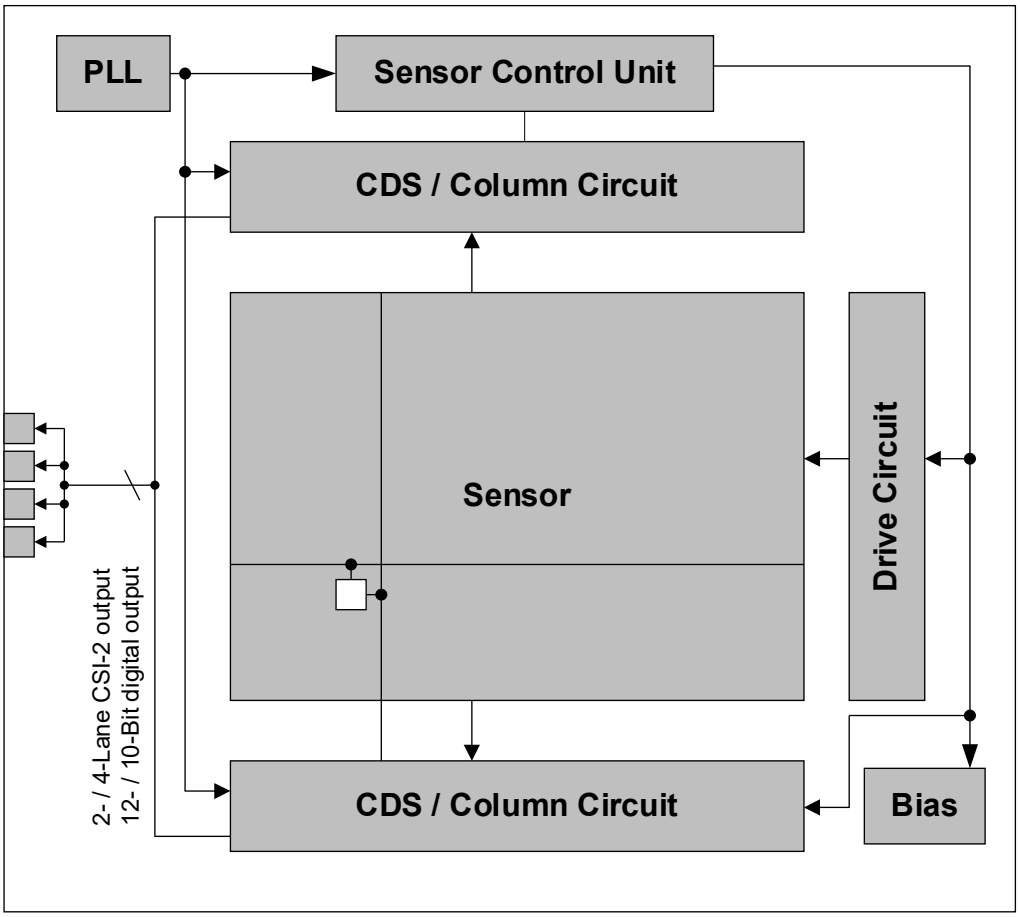
Pixel Arrangement



* The reference pin numbers are consecutive numbers in the package pin array.
For each pin number, see the “Pin Configuration” diagram on a few pages later.
Dummy is effective pixels whose data content should be ignored.
The last effective line and column are not read out.

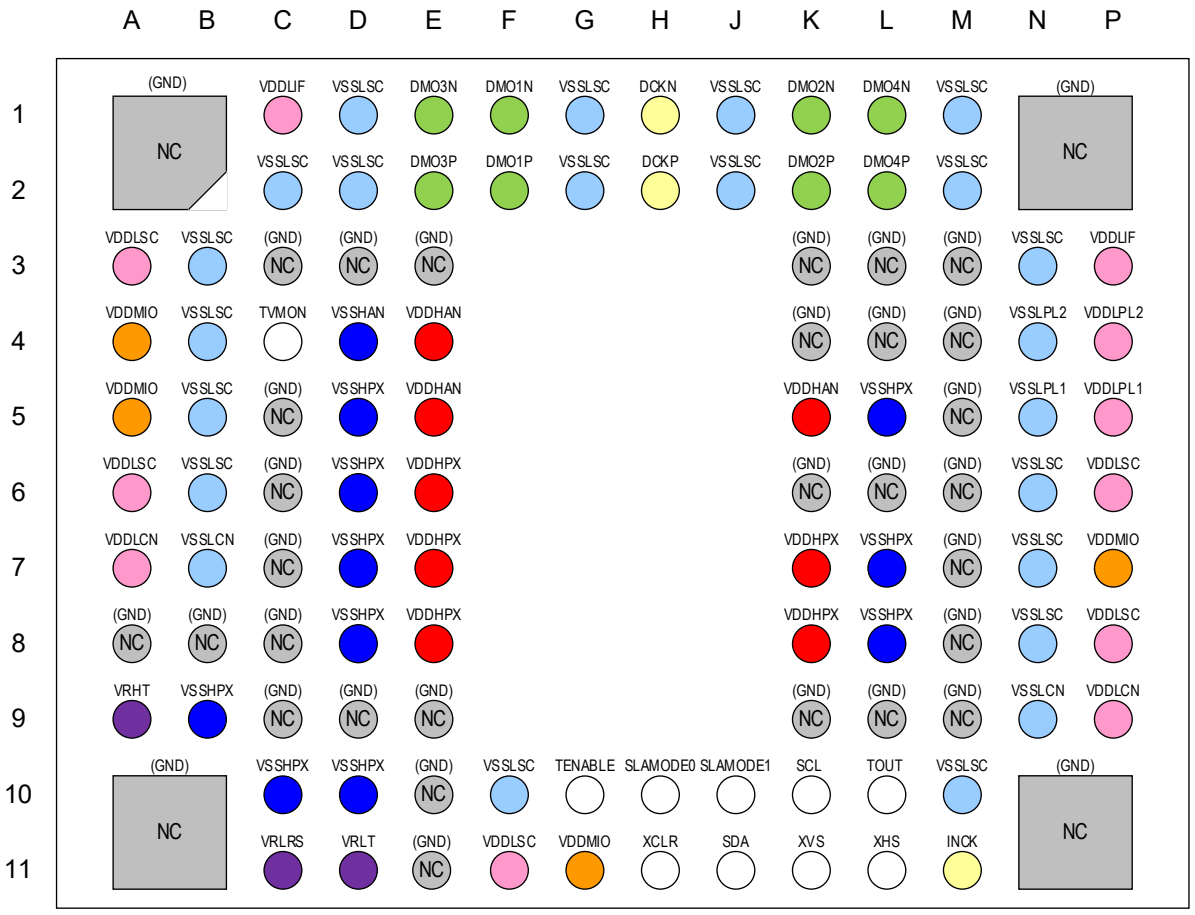
Pixel Arrangement

Block Diagram and Pin Configuration



Block Diagram

Bottom View



*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

Pin Description

No.	Pin No	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connectable
2	A3	Power	D	VDDLSC	1.1 V power supply
3	A4	Power	D	VDDMIO	1.8 V power supply
4	A5	Power	D	VDDMIO	1.8 V power supply
5	A6	Power	D	VDDLSC	1.1 V power supply
6	A7	Power	D	VDDLCN	1.1 V power supply
7	A8	—	—	N.C.	GND connectable
8	A9	O	A	VRHT	Capacitor connection
9	A11	—	—	N.C.	GND connectable
10	B3	GND	D	VSSLSC	1.1 V / 1.8 V GND
11	B4	GND	D	VSSLSC	1.1 V / 1.8 V GND
12	B5	GND	D	VSSLSC	1.1 V / 1.8 V GND
13	B6	GND	D	VSSLSC	1.1 V / 1.8 V GND
14	B7	GND	D	VSSLCN	1.1 V / 1.8 V GND
15	B8	—	—	N.C.	GND connectable
16	B9	GND	A	VSSHPX	2.9 V GND
17	C1	Power	D	VDDLIF	1.1 V power supply
18	C2	GND	D	VSSLSC	1.1 V / 1.8 V GND
19	C3	—	—	N.C.	GND connectable
20	C4	O	A	TVMON	TEST output pin, OPEN
21	C5	—	—	N.C.	GND connectable
22	C6	—	—	N.C.	GND connectable
23	C7	—	—	N.C.	GND connectable
24	C8	—	—	N.C.	GND connectable
25	C9	—	—	N.C.	GND connectable
26	C10	GND	A	VSSHPX	2.9 V GND
27	C11	O	A	VRLRS	Capacitor connection
28	D1	GND	D	VSSLSC	1.1 V / 1.8 V GND
29	D2	GND	D	VSSLSC	1.1 V / 1.8 V GND
30	D3	—	—	N.C.	GND connectable
31	D4	GND	A	VSSHAN	2.9 V GND
32	D5	GND	A	VSSHPX	2.9 V GND
33	D6	GND	A	VSSHPX	2.9 V GND
34	D7	GND	A	VSSHPX	2.9 V GND
35	D8	GND	A	VSSHPX	2.9 V GND
36	D9	—	—	N.C.	GND connectable
37	D10	GND	A	VSSHPX	2.9 V GND
38	D11	O	A	VRLT	Capacitor connection
39	E1	O	D	DMO3N	CSI-2 output (data)
40	E2	O	D	DMO3P	CSI-2 output (data)
41	E3	—	—	N.C.	GND connectable
42	E4	Power	A	VDDHAN	2.9 V power supply
43	E5	Power	A	VDDHAN	2.9 V power supply
44	E6	Power	A	VDDHPX	2.9 V power supply
45	E7	Power	A	VDDHPX	2.9 V power supply
46	E8	Power	A	VDDHPX	2.9 V power supply

No.	Pin No	I/O	Analog / Digital	Symbol	Description
47	E9	—	—	N.C.	GND connectable
48	E10	—	—	N.C.	GND connectable
49	E11	—	—	N.C.	GND connectable
50	F1	O	D	DMO1N	CSI-2 output (data)
51	F2	O	D	DMO1P	CSI-2 output (data)
52	F10	GND	D	VSSLSC	1.1 V / 1.8 V GND
53	F11	Power	D	VDDLSC	1.1 V power supply
54	G1	GND	D	VSSLSC	1.1 V / 1.8 V GND
55	G2	GND	D	VSSLSC	1.1 V / 1.8 V GND
56	G10	I	D	TENABLE	Test enable, OPEN
57	G11	Power	D	VDDMIO	1.8 V power supply
58	H1	O	D	DCKN	CSI-2 output (clock)
59	H2	O	D	DCKP	CSI-2 output (clock)
60	H10	I	D	SLAMODE0	Select slave address
61	H11	I	D	XCLR	System clear
62	J1	GND	D	VSSLSC	1.1 V / 1.8 V GND
63	J2	GND	D	VSSLSC	1.1 V / 1.8 V GND
64	J10	I	D	SLAMODE1	Select slave address
65	J11	I/O	D	SDA	Serial data communication
66	K1	O	D	DMO2N	CSI-2 output (data)
67	K2	O	D	DMO2P	CSI-2 output (data)
68	K3	—	—	N.C.	GND connectable
69	K4	—	—	N.C.	GND connectable
70	K5	Power	A	VDDHAN	2.9 V power supply
71	K6	—	—	N.C.	GND connectable
72	K7	Power	A	VDDHPX	2.9 V power supply
73	K8	Power	A	VDDHPX	2.9 V power supply
74	K9	—	—	N.C.	GND connectable
75	K10	I/O	D	SCL	Serial clock input
76	K11	I/O	D	XVS	Vertical sync signal
77	L1	O	D	DMO4N	CSI-2 output (data)
78	L2	O	D	DMO4P	CSI-2 output (data)
79	L3	—	—	N.C.	GND connectable
80	L4	—	—	N.C.	GND connectable
81	L5	GND	A	VSSHPX	2.9 V GND
82	L6	—	—	N.C.	GND connectable
83	L7	GND	A	VSSHPX	2.9 V GND
84	L8	GND	A	VSSHPX	2.9 V GND
85	L9	—	—	N.C.	GND connectable
86	L10	I/O	D	TOUT	Digital TEST output pin, OPEN
87	L11	I/O	D	XHS	Horizontal sync signal
88	M1	GND	D	VSSLSC	1.1 V / 1.8 V GND
89	M2	GND	D	VSSLSC	1.1 V / 1.8 V GND
90	M3	—	—	N.C.	GND connectable
91	M4	—	—	N.C.	GND connectable
92	M5	—	—	N.C.	GND connectable
93	M6	—	—	N.C.	GND connectable
94	M7	—	—	N.C.	GND connectable
95	M8	—	—	N.C.	GND connectable

No.	Pin No	I/O	Analog / Digital	Symbol	Description
96	M9	—	—	N.C.	GND connectable
97	M10	GND	D	VSSLSC	1.1 V / 1.8 V GND
98	M11	I	D	INCK	Master clock input
99	N3	GND	D	VSSLSC	1.1 V / 1.8 V GND
100	N4	GND	A	VSSLPL2	1.1 V / 1.8 V GND
101	N5	GND	A	VSSLPL1	1.1 V / 1.8 V GND
102	N6	GND	D	VSSLSC	1.1 V / 1.8 V GND
103	N7	GND	D	VSSLSC	1.1 V / 1.8 V GND
104	N8	GND	D	VSSLSC	1.1 V / 1.8 V GND
105	N9	GND	D	VSSLCN	1.1 V / 1.8 V GND
106	P1	—	—	N.C.	GND connectable
107	P3	Power	D	VDDLIF	1.1 V power supply
108	P4	Power	A	VDDLPL2	1.1 V power supply
109	P5	Power	A	VDDLPL1	1.1 V power supply
110	P6	Power	D	VDDLSC	1.1 V power supply
111	P7	Power	D	VDDMIO	1.8 V power supply
112	P8	Power	D	VDDLSC	1.1 V power supply
113	P9	Power	D	VDDLCN	1.1 V power supply
114	P11	—	—	N.C.	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}		2.80	2.90	3.00	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.00	1.10	1.20	V
Digital input voltage		XHS XVS XCLR INCK SLAMODE0 SLAMODE1	VIH	XVS / XHS slave mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS TOUT	VOH	XVS / XHS master mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

Current Consumption

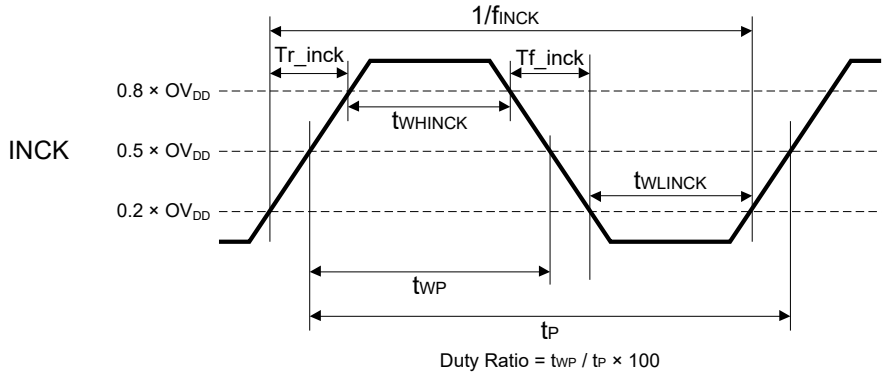
Item	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 / 4-lane, 2079 Mbps 12-bit, 60 frame/s All-pixel mode	I_{AVDD}	128	156	mA
	I_{OVDD}	3	3	mA
	I_{DVDD}	187	250	mA
Standby current	I_{AVDD_STB}	—	0.2	mA
	I_{OVDD_STB}	—	0.2	mA
	I_{DVDD_STB}	—	15.1	mA

Operating current: (Typ.) Supply voltage 2.9 V / 1.8 V / 1.1 V, Tj = 25 ˚C, standard luminous intensity.
(Max.) Supply voltage 3.0 V / 1.9 V / 1.2 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption.

Standby: (Max.) Supply voltage 3.0 V / 1.9 V / 1.2 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

AC Characteristics

Master Clock Waveform (INCK)

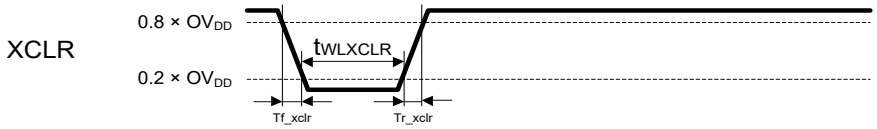


INCK 24 MHz, 27 MHz, 37.125 MHz, 72 MHz, 74.25 MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 24 MHz, 27 MHz, 37.125 MHz, 72 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

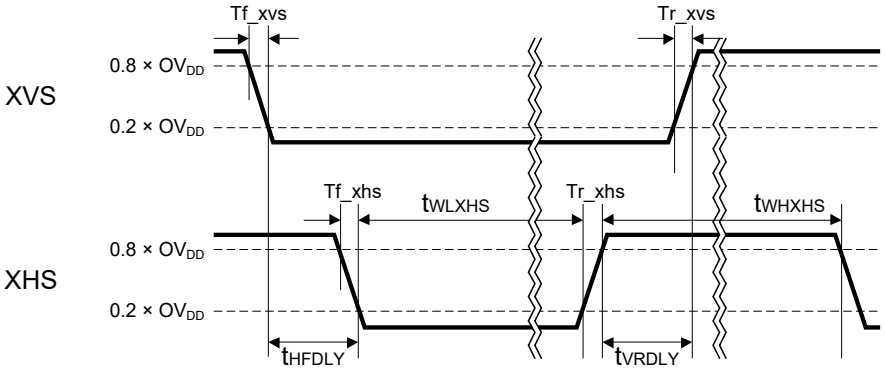
* The INCK fluctuation affects the frame rate.

System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	4 / f_{INCK}	—	—	ns	
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Slave Mode (Register XMASTER = 1)



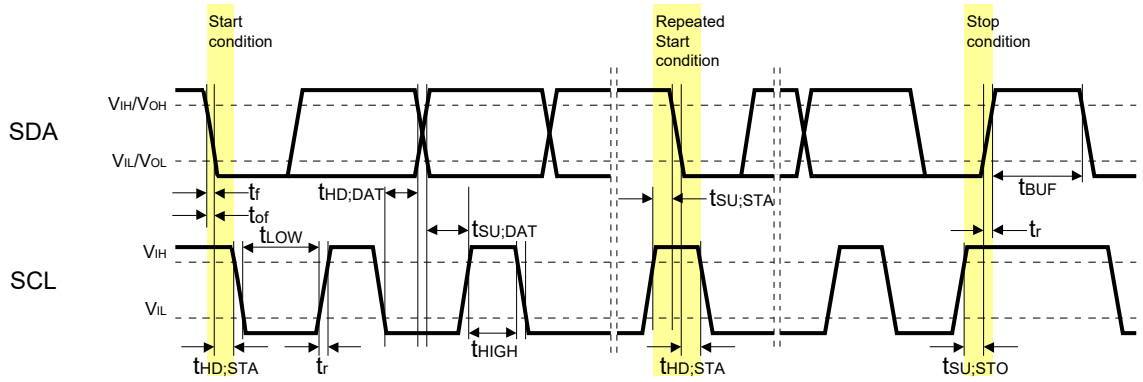
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %

XVS / XHS Output Characteristics in Master Mode (Register XMASTER = 0)

* XVS and XHS cannot be used as sync signals for pixel data.
  In order to detect the output start of each line, make sure to detect the sync code.
  For the output waveforms in master mode, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.

Serial Communication

I²C



I²C Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	–0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Input current	Ii	–10	—	10	µA	0.1 × OV_{DD} to 0.9 × OV_{DD}
Input capacitance for SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics (Standard-mode, Fast-mode)

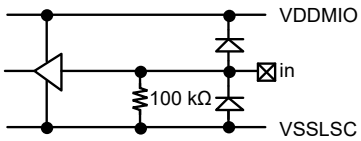
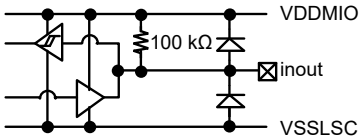
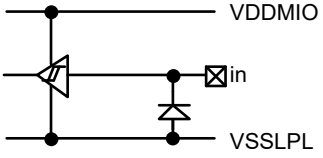
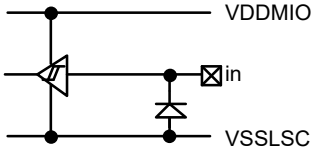
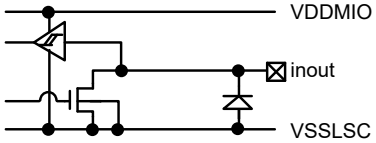
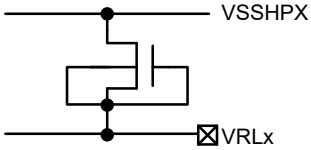
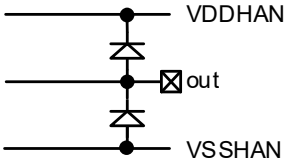
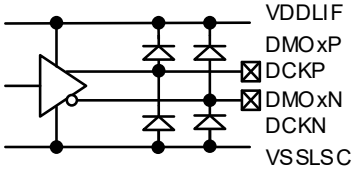
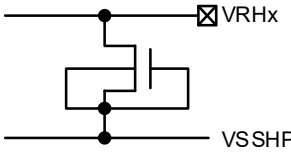
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	400	kHz	
Hold time (Start condition)	$t_{HD;STA}$	0.6	—	—	µs	
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs	
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs	
Set-up time (Repeated Start condition)	$t_{SU;STA}$	0.6	—	—	µs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs	
Data set-up time	$t_{SU;DAT}$	100	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	300	ns	
Fall time of both SDA and SCL signals	t_f	—	—	300	ns	
Set-up time (Stop condition)	$t_{SU;STO}$	0.6	—	—	µs	
Bus free time between a Stop and Start condition	t_{BUF}	1.3	—	—	µs	
Output fall time	t_{of}	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I²C AC Characteristics (Fast-mode Plus)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	1000	kHz	INCK ≥ 16 MHz
Hold time (Start condition)	$t_{HD;STA}$	0.26	—	—	µs	
Low period of the SCL clock	t_{LOW}	0.5	—	—	µs	
High period of the SCL clock	t_{HIGH}	0.26	—	—	µs	
Set-up time (Repeated Start condition)	$t_{SU;STA}$	0.26	—	—	µs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs	
Data set-up time	$t_{SU;DAT}$	50	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	120	ns	
Fall time of both SDA and SCL signals	t_f	—	—	120	ns	
Set-up time (Stop condition)	$t_{SU;STO}$	0.26	—	—	µs	
Bus free time between a Stop and Start condition	t_{BUF}	0.5	—	—	µs	
Output fall time	t_{of}	—	—	120	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I/O Equivalent Circuit Diagrams

☒: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS TOUT	
INCK		XCLR SLAMODE0 SLAMODE1	
SDA SCL		VRLRS VRLT	
TVMON		DMOxP DMOxN DCKP DCKN	
VRHT			

Spectral Sensitivity Characteristics

(Include AR coating characteristics but exclude light source characteristics.)

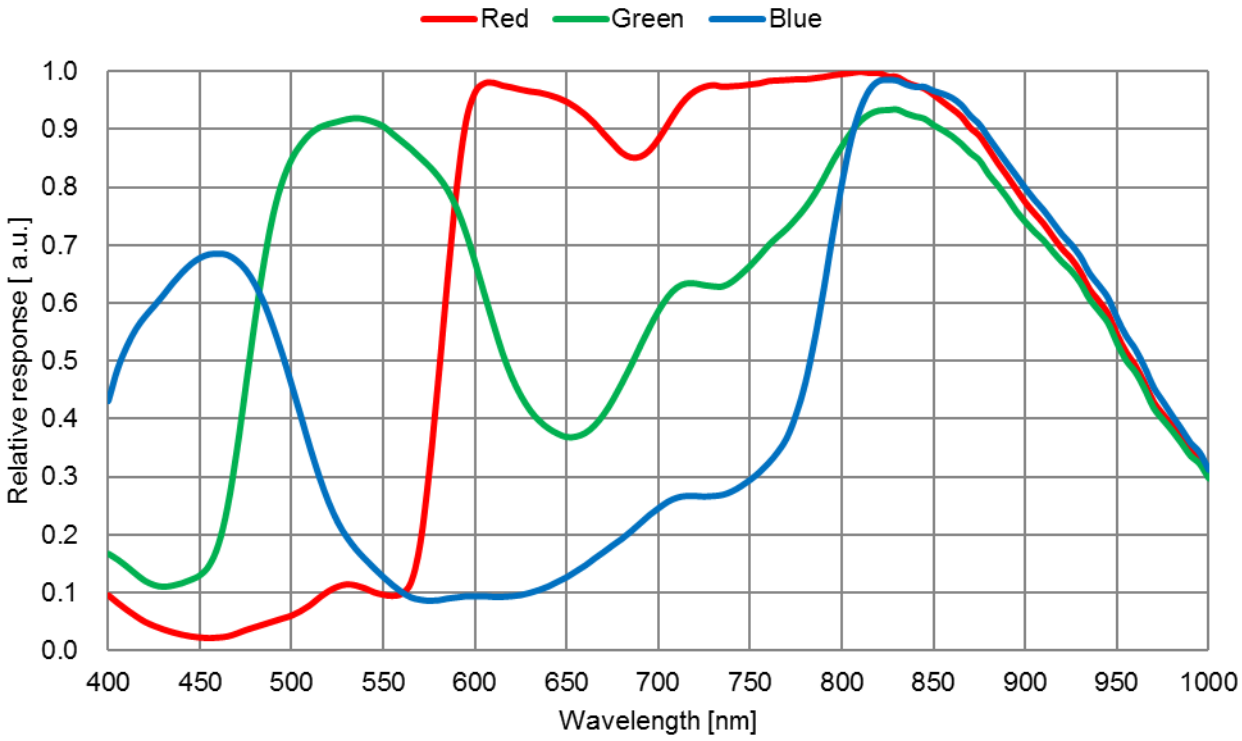


Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, All-pixel mode, 12-bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity (New measurement conditions)		S	5025 (736)	5912 (866)	—	Digit/lx/s (mV/lx/s)	1	12-bit converted value
G sensitivity (Old measurement conditions)		S	2019 (296)	2375 (348)	—	Digit (mV)	1	1/30 s storage 12-bit converted value
Sensitivity ratio	R / G	RG	0.47	—	0.63	—	2	—
	B / G	BG	0.31	—	0.49	—		
Saturation signal		Vsat	3895 (570)	—	—	Digit (mV)	3	12-bit converted value
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	μV	5	12-bit converted value
Dark signal		Vdt	—	—	0.89 (0.13)	Digit (mV)	6	1/30 s storage 12-bit converted value
Dark signal shading		ΔVdt	—	—	0.89 (0.13)	Digit (mV)	7	1/30 s storage 12-bit converted value

Note) 1. Converted value into mV using 1 Digit = 0.1465 mV for 12-bit output and 1 Digit = 0.5865 mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.
3. The characteristics above apply to the effective pixel area.
4. Since the measurement conditions are in transition, the old conditions are also described.

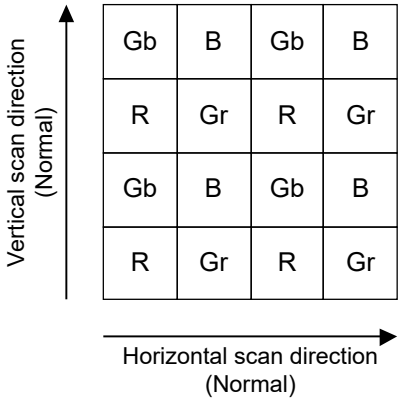
How to Measure Image Sensor Characteristics

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.



Color Coding Diagram

Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
[New measurement conditions]
Using a purple excitation LED light source with a color temperature of 2850 K, an IR cut filter CM700 (t = 1.0 mm) is placed between the LED light source and the sensor receiving surface to irradiate substantially parallel light.

[Old measurement conditions]
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Methods

1. Sensitivity
   [New measurement conditions]
   Set the measurement condition to the standard imaging condition I, and calculate using the illuminance (Ev) of the sensor receiving surface, the signal values (VGr, VGb, VR, VB) at the center of the screen, and the integration time (T).

   VG = (VGr + VGb) / 2
   S = VG / (Ev × T) [Digit/lx/s]

   [Old measurement conditions]
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100 / 30 [mV]

2. Sensitivity ratio
   By using the R and B signal outputs (VR, VB) obtained from the sensitivity measurement under the new measurement conditions, substitute the values into the following formulas.

   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 300 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 300 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 300 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculate each average output of Gr, Gb, R and B on respective columns. Calculate maximum value of difference with adjacent column on the same color (VL [μV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 6, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

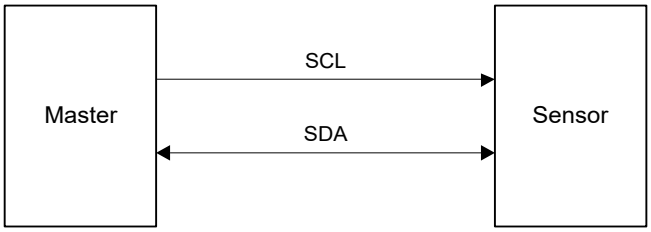
   ΔVdt = Vdmax – Vdmin [mV]

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I²C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I²C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE0 and SLAMODE1 pins, SLAVE address can be changed.



Pin Connections of Serial Communication

SLAVE Addresses

SLAMODE1 pin	SLAMODE0 pin	MSB							LSB
Low	Low	0	0	1	1	0	1	0	R / W
Low	High	0	0	1	0	0	0	0	R / W
High	Low	0	1	1	0	1	1	0	R / W
High	High	0	1	1	0	1	1	1	R / W

* R / W is the data direction bit.

R / W

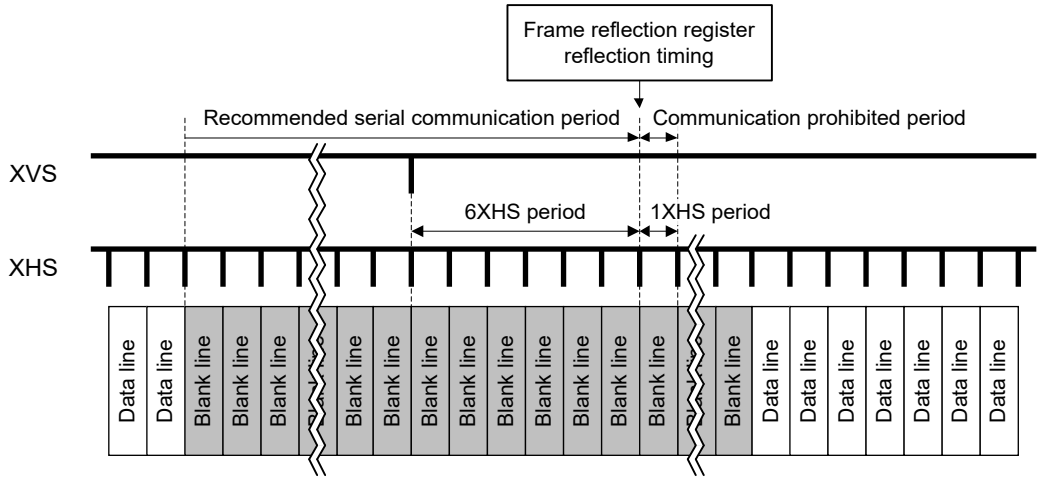
R / W bit	Data direction
0	Write (Master to Sensor)
1	Read (Sensor to Master)

Description of I²C pins

Symbol	Pin No.	Remarks
SCL	K10	I²C serial clock input
SDA	J11	I²C serial data communication

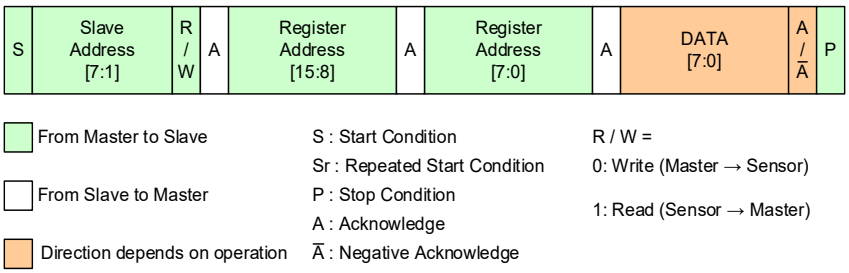
Register Communication Timing (I²C)

In I²C communication system, communication can be performed during the period excluding the communication prohibited period (1 XHS period) shown below.
The registers whose reflection timing is “V” in the register map are reflected by the “Frame reflection register reflection timing” when communication is performed during the communication period shown in the figure below.
Registers whose reflection timing is “I” (Immediately) are reflected when the communication is performed.
Using REGHOLD function is recommended for register setting using I²C communication. For REGHOLD function, see the item of “Register Hold Setting” in the section of “Description of Various Functions”.



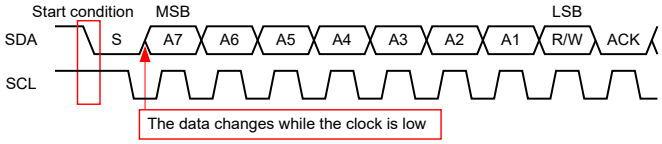
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

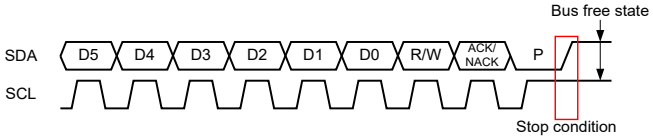


Communication Protocol

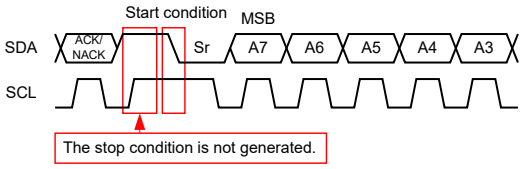
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

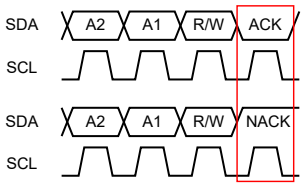


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and releases (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop condition and end the communication.



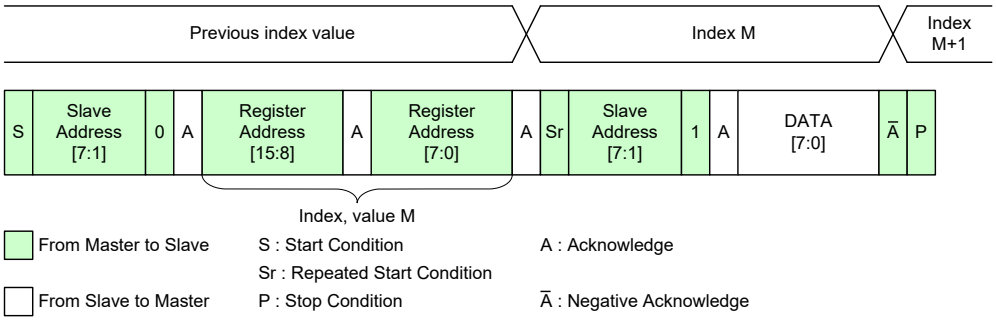
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

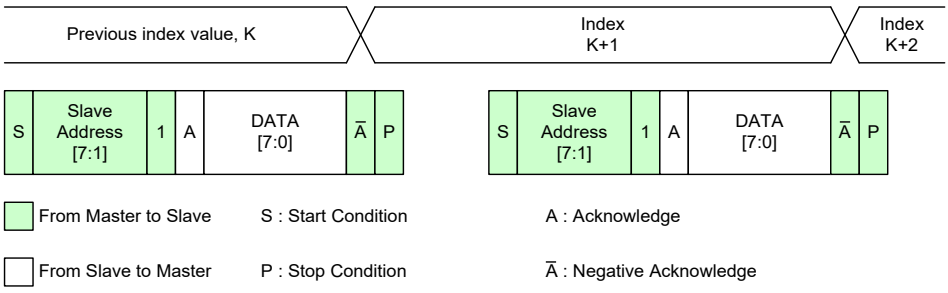
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose, it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.



Single Read from Random Location

Single Read from Current Location

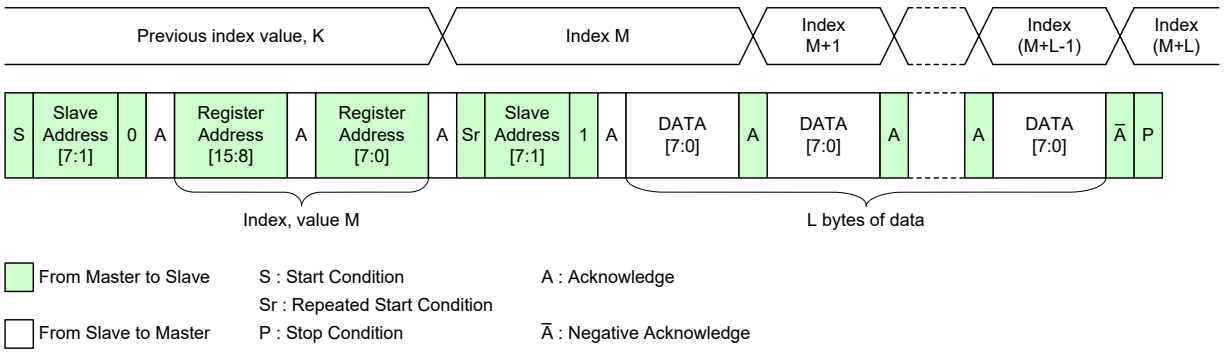
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

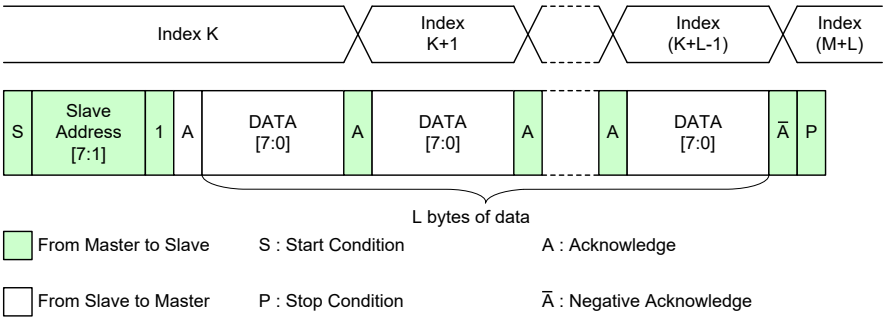
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting.
The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start condition.
Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

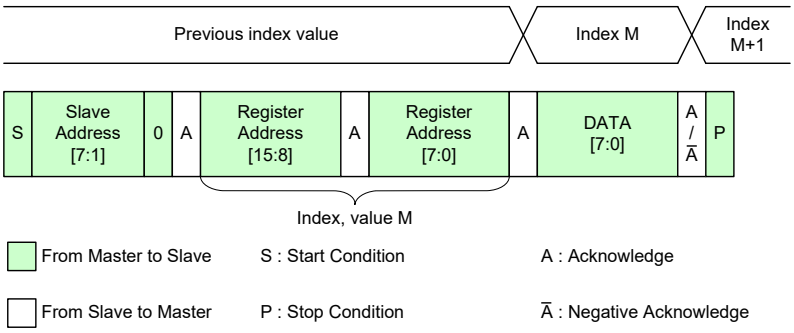
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA.
This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

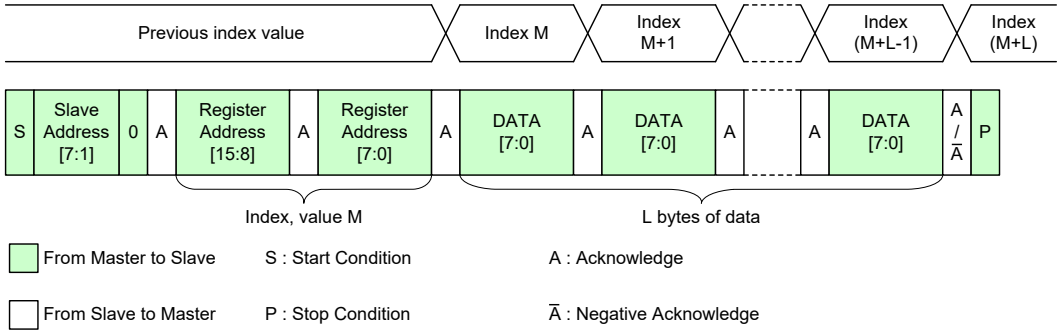
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 4352 (256 × 17) bytes of registers. Each register has an address consisting of the MSB address in the range 30h to 40h and the LSB address in the range 00h to FFh. Use the default values for addresses not listed in the Register Map. Since there are registers that need to be changed from the default values, make sure that the sensor control side can set a total of 4352 bytes.

There are three different register reflection timings.
About the reflection timing column of the Register Map, registers noted as “I” are reflected immediately after writing to register, registers noted as “S” are set during standby mode and reflected after standby cancel, registers noted as “V” are reflected at “Frame reflection register reflection timing” described in the item of “Register Communication Timing (I^2C)” in the section of “Setting Registers Using Serial Communication”.

Do not communicate or set to an address not listed in the Register Map. Doing so may result in operation errors. However, registers may be added to addresses not currently listed in the Register Map, so be prepared to enable register communication for the entire range from addresses 3000h to 40FFh.

* For registers in which the description column is written in red, change the default value to the setting value written in red after reset.
** Only the gain setting is reflected and output in the frame that is delayed by one frame from the set frame.
*** Settings other than those described in the description column are prohibited.

(1) Registers corresponding to address = 30**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3001h	0	REGHOLD	Register hold (Function not to update V reflection registers) 0: Invalid 1: Valid	0h	00h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3003h	0	XMASTER	Select master or slave mode. 0: Master mode 1: Slave mode	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3008h	0	BCWAIT_TIME [9:0]	LSB	0FFh	FFh	S
	1					
	2					
	3					
	4		The value is set according to INCK. See “INCK Setting”.			
	5					
	6					
	7					
3009h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
300Ah	0	CPWAIT_TIME [9:0]	LSB	0B6h	B6h	S
	1					
	2					
	3					
	4		The value is set according to INCK. See “INCK Setting”.			
	5					
	6					
	7					
300Bh	0				A0h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “1h”	1h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “1h”	1h		—
301Ch	0	WINMODE [3:0]	Window mode setting 0: All-pixel mode, Horizontal/Vertical 2/2-line binning 4: Window cropping mode	0h	00h	V
	1					
	2					
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3020h	0	HADD	Mode setting 0h: All-pixel mode 1h: Horizontal 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3021h	0	VADD	Mode setting 0h: All-pixel mode 1h: Vertical 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3022h	0	ADDMODE [1:0]	Mode setting 0h: All-pixel mode 1h: Horizontal/Vertical 2/2-line binning	0h	00h	S
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3024h	0	VMAX [19:0]	LSB	008CAh	CAh	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		In sensor master mode Vertical period For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.			
3025h	0				08h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3026h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3028h	0	HMAX [15:0]	LSB	0226h	26h	V
	1					
	2					
	3					
	4					
	5		In sensor master mode Horizontal period For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.			
	6					
	7					
3029h	0				02h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3030h	0	HREVERSE	Horizontal direction Readout inversion control 0: Normal 1: Inverted	0h	00h	V
	1	VREVERSE	Vertical direction Readout inversion control 0: Normal 1: Inverted	0h		V
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3031h	0	ADBIT [1:0]	AD conversion bit width setting 0: AD 10-bit 1: AD 12-bit (11 bits + digital dither)	1h	01h	S
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3032h	0	MDBIT	Bit width setting for pixel data output from the sensor 0: 10-bit 1: 12-bit	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3033h	0	SYS_MODE [3:0]	Output IF mode setting 0: 2376 Mbps 2: 2079 Mbps 4: 1782 Mbps 5: 891 Mbps 6: 1188 Mbps 7: 594 Mbps 8: 1440 / 1485 Mbps 9: 720 Mbps	4h	04h	S
	1					
	2					
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3040h	0	PIX_HST [12:0]	LSB In Window cropping mode Start position (Horizontal direction)	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3041h	0		Multiples of 2		00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3042h	0	PIX_HWIDTH [12:0]	LSB In Window cropping mode Cropping width (Horizontal direction)	0F18h	18h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3043h	0		Multiples of 24		0Fh	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3044h	0	PIX_VST [12:0]	LSB In Window cropping mode Start position (Vertical direction)	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3045h	0		Designated in Line × 2, Multiples of 4		00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3046h	0	PIX_VWIDTH [12:0]	LSB	1120h	20h	V
	1					
	2					
	3					
	4		In Window cropping mode Cropping width (Vertical direction)			
	5					
	6					
	7		Designated in Line × 2, Multiples of 4			
3047h	0				11h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3050h	0	SHR0 [19:0]	LSB	00066h	66h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3051h	0		Storage time adjustment Designated in line units.		00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3052h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3090h	0	GAIN_PGC_0 [8:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4		Gain setting (0.0 dB to 72.0 dB / 0.3 dB step)			
	5					
	6					
	7					
3091h	0		MSB		00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30C0h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to Low 2: VSYNC output	2h	2Ah	I
	1					
	2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to Low 2: HSYNC output	2h		I
	3					
	4	—	Fixed to “2h”	2h		—
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30C1h	0	XVS_DRV [1:0]	XVS pin setting 0: XVS output (master mode) 3: Hi-Z (slave mode)	3h	0Fh	S
	1					
	2	XHS_DRV [1:0]	XHS pin setting 0: XHS output (master mode) 3: Hi-Z (slave mode)	3h		S
	3					
	4	—	Fixed to “0h”	0h		—
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30CCh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XVSLNG [1:0]	XVS pulse width setting in master mode. 0: 1H 1: 2H 2: 4H 3: 8H	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30CDh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XHSLNG [1:0]	XHS pulse width setting in master mode. 0: 16 clocks 1: 32 clocks 2: 64 clocks 3: 128 clocks	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30D9h	0	DIG_CLP_VSTART [4:0]	The value is set according to the readout mode. 2: Horizontal/Vertical 2/2-line binning mode 6: All-pixel scan mode	06h	06h	S
	1					
	2					
	3					
	4					
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30DAh	0	DIG_CLP_VNUM [1:0]	The value is set according to the readout mode. 1: Horizontal/Vertical 2/2-line binning mode 2: All-pixel scan mode	2h	02h	S
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30E2h	0	BLKLEVEL [9:0]	LSB	032h	32h	I
	1					
	2					
	3		Black level offset value setting			
	4					
	5		10-bit readout mode: 1 Digit/1h			
	6		12-bit readout mode: 4 Digits/1h			
	7					
30E3h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

(2) Registers corresponding to address = 31**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3115h	[7:0]	INCKSEL1 [7:0]	The value is set according to the INCK. See “INCK Setting”.	00h	00h	S
3116h	[7:0]	INCKSEL2 [7:0]	The value is set according to the INCK. See “INCK Setting”.	28h	28h	S
3118h	0	INCKSEL3 [10:0]	LSB	0C0h	C0h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3119h	0		The value is set according to the INCK. See “INCK Setting”.		00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
311Ah	0	INCKSEL4 [10:0]	LSB	0E0h	E0h	S
	1					
	2					
	3					
	4					
	5					
	6					
	7					
311Bh	0		The value is set according to the INCK. See “INCK Setting”.		00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
311Eh	[7:0]	INCKSEL5 [7:0]	The value is set according to the INCK. See “INCK Setting”.	28h	28h	S

(3) Registers corresponding to address = 32**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
32D4h	[7:0]	—	Set to “21h”	20h	20h	S
32ECh	[7:0]	—	Set to “A1h”	A0h	A0h	S

(4) Registers corresponding to address = 34**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
344Ch	[7:0]	—	Set to “2Bh”	00h	00h	S
344Dh	[7:0]	—	Set to “01h”	00h	00h	S
344Eh	[7:0]	—	Set to “EDh”	00h	00h	S
344Fh	[7:0]	—	Set to “01h”	00h	00h	S
3450h	[7:0]	—	Set to “F6h”	00h	00h	S
3451h	[7:0]	—	Set to “02h”	00h	00h	S
3452h	[7:0]	—	Set to “7Fh”	00h	00h	S
3453h	[7:0]	—	Set to “03h”	00h	00h	S

(5) Registers corresponding to address = 35**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
358Ah	[7:0]	—	Set to “04h”	06h	06h	S
35A1h	[7:0]	—	Set to “02h”	00h	00h	S
35ECh	[7:0]	—	Set to “27h”	04h	04h	S
35EEh	[7:0]	—	Set to “8Dh”	27h	27h	S
35F0h	[7:0]	—	Set to “8Dh”	29h	29h	S
35F2h	[7:0]	—	Set to “29h”	04h	04h	S

(6) Registers corresponding to address = 36**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
36BCh	[7:0]	—	Set to “0Ch”	00h	00h	S
36CCh	[7:0]	—	Set to “53h”	FFh	FFh	S
36CDh	[7:0]	—	Set to “00h”	01h	01h	S
36CEh	[7:0]	—	Set to “3Ch”	00h	00h	S
36D0h	[7:0]	—	Set to “8Ch”	FFh	FFh	S
36D1h	[7:0]	—	Set to “00h”	01h	01h	S
36D2h	[7:0]	—	Set to “71h”	00h	00h	S
36D4h	[7:0]	—	Set to “3Ch”	00h	00h	S
36D6h	[7:0]	—	Set to “53h”	FFh	FFh	S
36D7h	[7:0]	—	Set to “00h”	01h	01h	S
36D8h	[7:0]	—	Set to “71h”	00h	00h	S
36DAh	[7:0]	—	Set to “8Ch”	FFh	FFh	S
36DBh	[7:0]	—	Set to “00h”	01h	01h	S

(7) Registers corresponding to address = 37**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3701h	[7:0]	ADBIT1 [7:0]	The value is set according to the AD conversion bit width. 00h: AD 10-bit 03h: AD 12-bit (11 bits + digital dither)	03h	03h	S
3720h	[7:0]	—	Set to “00h”	07h	07h	S
3724h	[7:0]	—	Set to “02h”	0Ah	0Ah	S
3726h	[7:0]	—	Set to “02h”	0Ah	0Ah	S
3732h	[7:0]	—	Set to “02h”	00h	00h	S
3734h	[7:0]	—	Set to “03h”	0Ah	0Ah	S
3736h	[7:0]	—	Set to “03h”	0Ah	0Ah	S
3742h	[7:0]	—	Set to “03h”	00h	00h	S

(8) Registers corresponding to address = 38**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3862h	[7:0]	—	Set to “E0h”	7Fh	7Fh	S
38CCh	[7:0]	—	Set to “30h”	33h	33h	S
38CDh	[7:0]	—	Set to “2Fh”	33h	33h	S

(9) Registers corresponding to address = 39**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
395Ch	[7:0]	—	Set to “0Ch”	00h	00h	S
39A4h	[7:0]	—	Set to “07h”	00h	00h	S
39A8h	[7:0]	—	Set to “32h”	1Eh	1Eh	S
39AAh	[7:0]	—	Set to “32h”	1Eh	1Eh	S
39ACh	[7:0]	—	Set to “32h”	19h	19h	S
39AEh	[7:0]	—	Set to “32h”	19h	19h	S
39B0h	[7:0]	—	Set to “32h”	19h	19h	S
39B2h	[7:0]	—	Set to “2Fh”	19h	19h	S
39B4h	[7:0]	—	Set to “2Dh”	19h	19h	S
39B6h	[7:0]	—	Set to “28h”	19h	19h	S
39B8h	[7:0]	—	Set to “30h”	1Eh	1Eh	S
39BAh	[7:0]	—	Set to “30h”	1Eh	1Eh	S
39BCh	[7:0]	—	Set to “30h”	19h	19h	S
39BEh	[7:0]	—	Set to “30h”	19h	19h	S
39C0h	[7:0]	—	Set to “30h”	19h	19h	S
39C2h	[7:0]	—	Set to “2Eh”	19h	19h	S
39C4h	[7:0]	—	Set to “2Bh”	19h	19h	S
39C6h	[7:0]	—	Set to “25h”	19h	19h	S

(10) Registers corresponding to address = 3A**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3A42h	[7:0]	—	Set to “D1h”	11h	11h	S
3A4Ch	[7:0]	—	Set to “77h”	37h	37h	S
3AE0h	[7:0]	—	Set to “02h”	00h	00h	S
3AECh	[7:0]	—	Set to “0Ch”	00h	00h	S

(11) Registers corresponding to address = 3B**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3B00h	[7:0]	—	Set to “2Eh”	28h	28h	S
3B06h	[7:0]	—	Set to “29h”	23h	23h	S
3B98h	[7:0]	—	Set to “25h”	19h	19h	S
3B99h	[7:0]	—	Set to “21h”	19h	19h	S
3B9Bh	[7:0]	—	Set to “13h”	19h	19h	S
3B9Ch	[7:0]	—	Set to “13h”	19h	19h	S
3B9Dh	[7:0]	—	Set to “13h”	19h	19h	S
3B9Eh	[7:0]	—	Set to “13h”	16h	16h	S
3BA1h	[7:0]	—	Set to “00h”	04h	04h	S
3BA2h	[7:0]	—	Set to “06h”	09h	09h	S
3BA3h	[7:0]	—	Set to “0Bh”	09h	09h	S
3BA4h	[7:0]	—	Set to “10h”	0Dh	0Dh	S
3BA5h	[7:0]	—	Set to “14h”	0Dh	0Dh	S
3BA6h	[7:0]	—	Set to “18h”	0Dh	0Dh	S
3BA7h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BA8h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BA9h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BACh	[7:0]	—	Set to “EDh”	00h	00h	S
3BADh	[7:0]	—	Set to “01h”	00h	00h	S
3BAEh	[7:0]	—	Set to “F6h”	22h	22h	S
3BAFh	[7:0]	—	Set to “02h”	00h	00h	S
3BB0h	[7:0]	—	Set to “A2h”	84h	84h	S
3BB1h	[7:0]	—	Set to “03h”	00h	00h	S
3BB2h	[7:0]	—	Set to “E0h”	A2h	A2h	S
3BB3h	[7:0]	—	Set to “03h”	00h	00h	S
3BB4h	[7:0]	—	Set to “E0h”	11h	11h	S
3BB5h	[7:0]	—	Set to “03h”	01h	01h	S
3BB6h	[7:0]	—	Set to “E0h”	ECh	ECh	S
3BB7h	[7:0]	—	Set to “03h”	01h	01h	S
3BB8h	[7:0]	—	Set to “E0h”	7Ah	7Ah	S
3BBAh	[7:0]	—	Set to “E0h”	D1h	D1h	S
3BBCh	[7:0]	—	Set to “DAh”	ECh	ECh	S
3BBEh	[7:0]	—	Set to “88h”	F5h	F5h	S
3BC0h	[7:0]	—	Set to “44h”	43h	43h	S
3BC2h	[7:0]	—	Set to “7Bh”	7Ah	7Ah	S
3BC4h	[7:0]	—	Set to “A2h”	A1h	A1h	S
3BC8h	[7:0]	—	Set to “BDh”	D1h	D1h	S
3BCAh	[7:0]	—	Set to “BDh”	DBh	DBh	S

(12) Registers corresponding to address = 40**h.

Address	bit	Register name	Description	Default value		Reflection timing
				By register	By address	
4001h	0	LANEMODE [2:0]	Output interface selection 1: CSI-2 2-lane 3: CSI-2 4-lane	3h	03h	S
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
4004h	[7:0]	TXCLKESC_FREQ [15:0]	The value is set according to the INCK. See “INCK Setting”.	1290h	90h	S
4005h	[7:0]				12h	
400Ch	0	INCKSEL6	The value is set according to the INCK. See “INCK Setting”.	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
4018h	[7:0]	TCLKPOST [15:0]	Global timing setting	00B7h	B7h	S
4019h	[7:0]				00h	
401Ah	[7:0]	TCLKPREPARE [15:0]	Global timing setting	0067h	67h	S
401Bh	[7:0]				00h	
401Ch	[7:0]	TCLKTRAIL [15:0]	Global timing setting	006Fh	6Fh	S
401Dh	[7:0]				00h	
401Eh	[7:0]	TCLKZERO [15:0]	Global timing setting	01DFh	DFh	S
401Fh	[7:0]				01h	
4020h	[7:0]	THSPREPARE [15:0]	Global timing setting	006Fh	6Fh	S
4021h	[7:0]				00h	
4022h	[7:0]	THSZERO [15:0]	Global timing setting	00CFh	CFh	S
4023h	[7:0]				00h	
4024h	[7:0]	THSTRAIL [15:0]	Global timing setting	006Fh	6Fh	S
4025h	[7:0]				00h	
4026h	[7:0]	THSEXIT [15:0]	Global timing setting	00B7h	B7h	S
4027h	[7:0]				00h	
4028h	[7:0]	TLPX [15:0]	Global timing setting	005Fh	5Fh	S
4029h	[7:0]				00h	
4074h	0	INCKSEL7 [2:0]	The value is set according to the INCK. See “INCK Setting”.	0h	00h	S
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Readout Drive Modes

Operating Modes

The table below shows the operating modes available with this sensor.
These frame rates indicate the maximum rates for each mode. For typical frame rates, see “List of Setting Registers” in the section of “Details of Each Readout Drive Mode”.

Mode	Lane	Data rate [Mbps/lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording pixels H [pixel]	Recording pixels V [line]	INCK [MHz]	1H period [clock]	1V period [XHS]
All-pixel	2	2079	10	10	44.4	3840	2160	27, 37.125, 74.25	746 (*1)	2238
			12	12	37.5				884 (*1)	
		1782	10	10	38.5			27, 37.125, 74.25	861 (*1)	
			12	12	32.4				1022 (*1)	
		1440	10	10	31.6			24, 72	1016 (*2)	
		1188	10	10	26.5			24, 27, 37.125, 72, 74.25	1250 (*1)	
			12	12	22.2				1494 (*1)	
		891	10	10	19.8			27, 37.125, 74.25	1668 (*1)	
			12	12	16.6				1990 (*1)	
		720	10	10	16.2			24, 72	1985 (*2)	
		594	10	10	13.4			27, 37.125, 74.25	2475 (*1)	
			12	12	11.2				2958 (*1)	
	4	2376	10	10	90.9			27, 37.125, 74.25	365 (*1)	
		2079	10	10	82.9			27, 37.125, 74.25	400 (*1)	
			12	12	60.3				550 (*1)	
		1782	10	10	72.4			27, 37.125, 74.25	458 (*1)	
			12	12	60.3				550 (*1)	
		1485	10	10	61.6			27, 37.125, 74.25	538 (*1)	
			12	12	52.2				635 (*1)	
		1440	10	10	60.4			24, 72	532 (*2)	
			12	12	51.1				629 (*2)	
		1188	10	10	51.5			24, 27, 37.125, 72, 74.25	644 (*1)	
			12	12	43.3				766 (*1)	
		891	10	10	38.5			27, 37.125, 74.25	861 (*1)	
			12	12	32.4				1022 (*1)	
		720	10	10	31.6			24, 72	1017 (*2)	
			12	12	26.5				1210 (*2)	
		594	10	10	26.2			27, 37.125, 74.25	1265 (*1)	
			12	12	22.0				1506 (*1)	

(*1) Clock frequency = 74.25 [MHz]
(*2) Clock frequency = 72 [MHz]

Mode	Lane	Data rate [Mbps/lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording pixels		INCK [MHz]	1H period [clock]	1V period [XHS]
						H [pixel]	V [line]			
Horizontal/ Vertical 2/2-line binning	2	2079	10	12	70.2	1920	1080	27, 37.125, 74.25	472 (*1)	2238
		1782	10	12	61.2			27, 37.125, 74.25	542 (*1)	
		891	10	12	32.2			27, 37.125, 74.25	1030 (*1)	
		594	10	12	21.8			27, 37.125, 74.25	1518 (*1)	
	4	2079	10	12	90.9			27, 37.125, 74.25	365 (*1)	
		1782	10	12	90.9			27, 37.125, 74.25	365 (*1)	
		1440	10	12	88.1			24, 72	365 (*2)	
		891	10	12	61.2			27, 37.125, 74.25	542 (*1)	
		720	10	12	50.7			24, 72	634 (*2)	
		594	10	12	42.2			27, 37.125, 74.25	786 (*1)	

(*1) Clock frequency = 74.25 [MHz]
(*2) Clock frequency = 72 [MHz]

Image Data Output Format (CSI-2 Output)

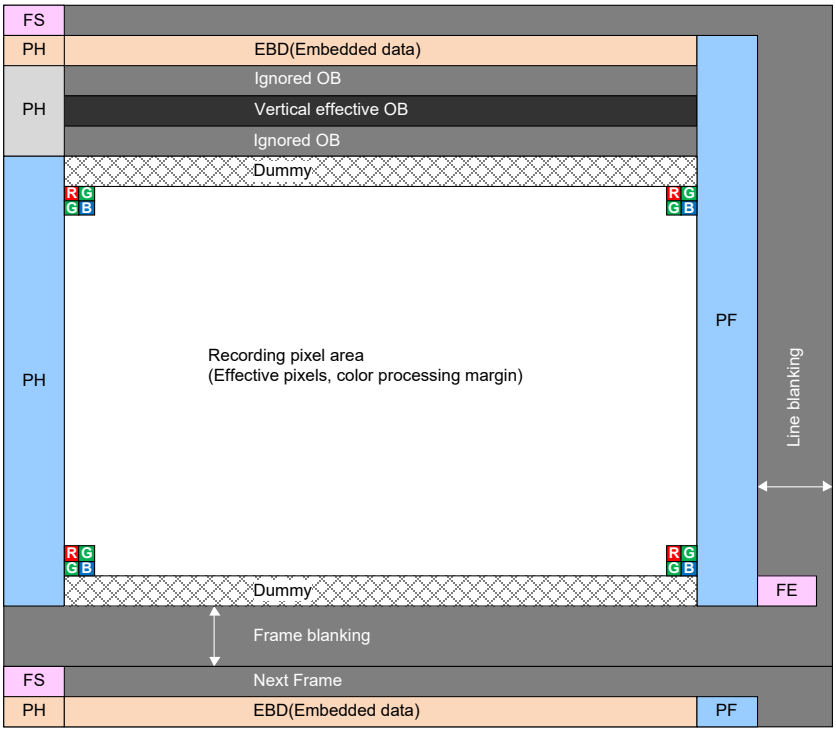
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. Types of data in each line are shown below.

Data Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 3032h MDBIT [0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

Frame Structure



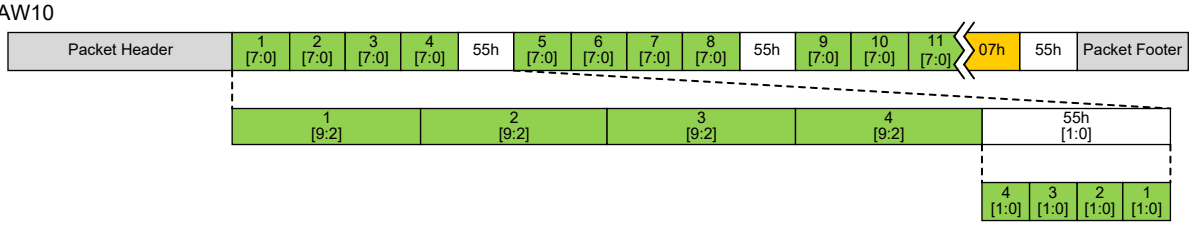
Frame Structure of CSI-2 Output

Embedded Data Line

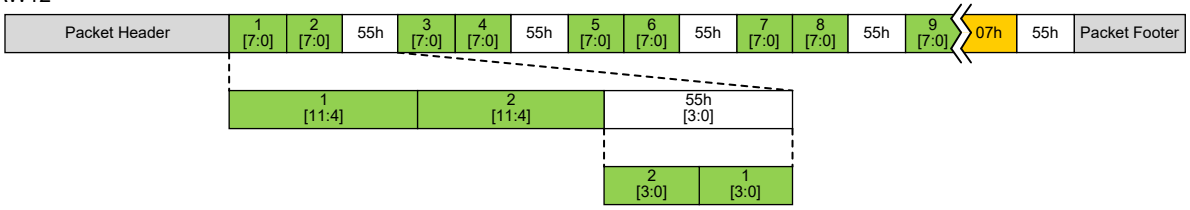
The Embedded data line is output to the line following the sync code FS.

Embedded Data Format

RAW10



RAW12



The detailed output is shown below.

Pixel (8-bit)	bit	I²C address [HEX]	Data byte description	Description
1	[7:0]	–	–	Ignored
2	[3:0]	301C [3:0]	WINMODE	
3	[3:0]	–	–	Ignored
	[4]	3030 [0]	HREVERSE	
	[6:5]	3022 [1:0]	ADDMODE	
	[7]	–	–	Ignored
4 to 8	[7:0]	–	–	Ignored
9	[4:0]	–	–	Ignored
	[5]	3030 [1]	VREVERSE	
	[7:6]	–	–	Ignored
10	[7:0]	–	–	Ignored
11	[5:0]	–	–	Ignored
	[7:6]	3031 [1:0]	ADBIT	
12	[7:0]	–	–	Ignored
13	[2:0]	4001 [2:0]	LANEMODE	
	[3]	3032 [0]	MDBIT	
	[7:4]	3033 [3:0]	SYS_MODE	
14 to 23	[7:0]	–	–	Ignored
24	[7:0]	3050 [7:0]	SHR0	
25	[7:0]	3051 [7:0]		
26	[3:0]	3052 [3:0]		
	[7:4]	–	–	Ignored
27 to 53	[7:0]	–	–	Ignored
54	[7:0]	30E2 [7:0]	BLKLEVEL	
55	[1:0]	30E3 [1:0]		
	[7:2]	–	–	Ignored
56 to 216	[7:0]	–	–	Ignored

Output data is Data [7:0] = 00h from 217 to 224 pixel.
Output data is Data [7:0] = 07h from 225 to end pixel.

Details of Each Readout Drive Mode

The tables below show the register setting examples of typical frame rates.
For frame rates other than the typical frame rates, the frame rate can be calculated using the following formula.

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))

V_{TTL} : Length of one frame in line units, or VMAX.
A value greater than or equal to the “1V period” in the “Operating Modes” table.

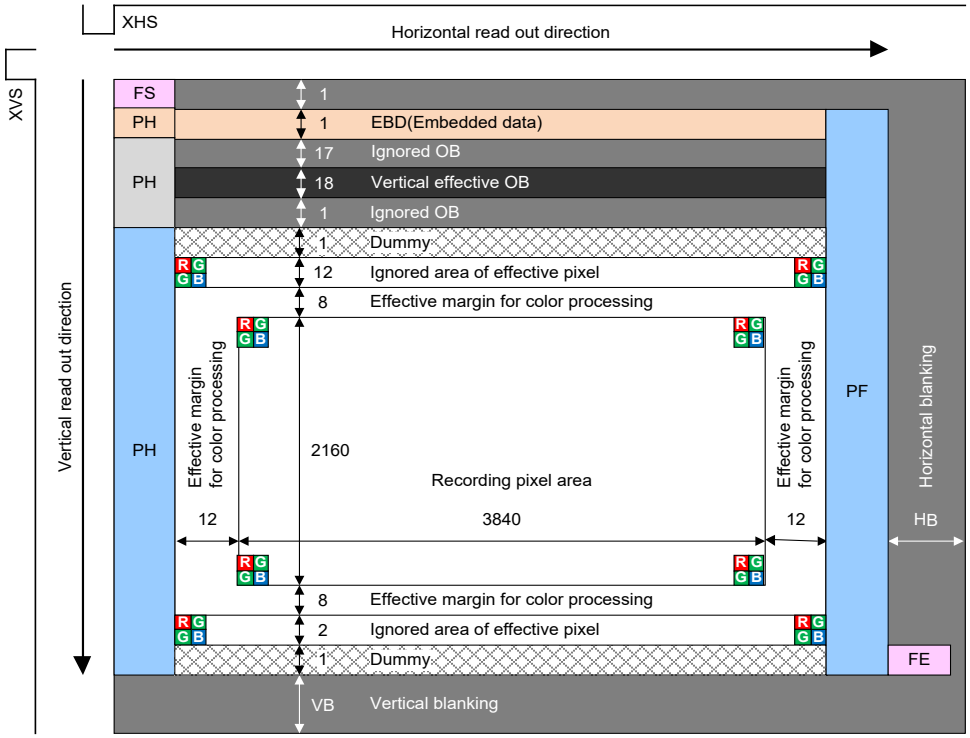
1H period (set in units [s]) : A value greater than or equal to the “1H period” in the “Operating Modes” table.

All-pixel Mode

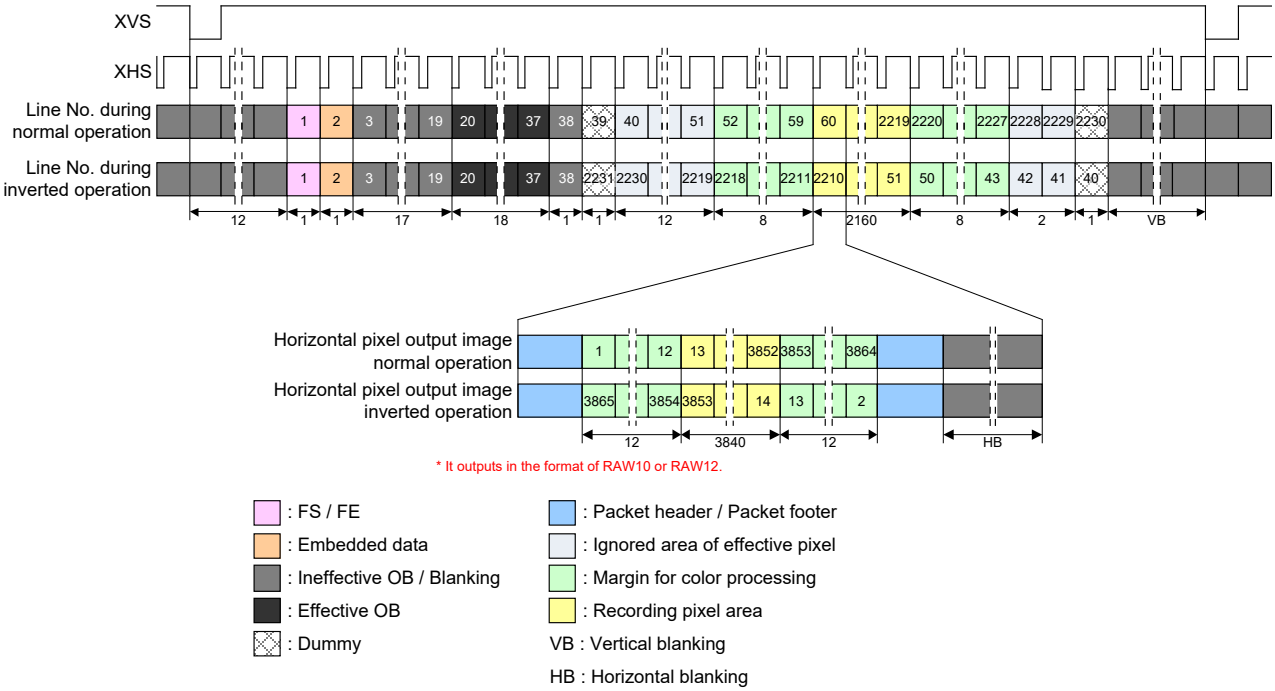
List of Setting Registers

Address	bit	Register name	Initial value	CSI-2 serial 2-lane												Remarks
				12	10	10	12	10	12	10	10	12	10	12	10	Bit width
				10		15.74	15		15	25	30.01	30		30		[frame/s]
				594		720	891		1188		1440	1782		2079		[Mbps/lane]
				44.5		28.3	29.7		29.7	17.8	14.9	14.9		14.9		1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	See “INCK Setting”.												
3009h	[1:0]															
300Ah	[7:0]	CPWAIT_TIME	0B6h													
300Bh	[1:0]															
301Ch	[3:0]	WINMODE	0h	0h												All-pixel mode
3022h	[1:0]	ADDMODE	0h	0h												All-pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh												
3025h	[7:0]															
3026h	[3:0]															
3028h	[7:0]	HMAX	226h	CE4h		7F0h	898h		898h	528h	42Ah	44Ch		44Ch		
3029h	[7:0]															
3030h	[0]	HREVERSE	0h	0h or 1h												0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h or 1h												0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	1h	0h	0h	1h	0h	1h	0h	0h	1h	0h	1h	0h	0: 10-bit, 1: 12-bit
3032h	[0]	MDBIT	1h	1h	0h	0h	1h	0h	1h	0h	0h	1h	0h	1h	0h	0: 10-bit, 1: 12-bit
3033h	[3:0]	SYS_MODE	4h	7h		9h	5h		6h		8h	4h		2h		
3115h	[7:0]	INCKSEL1	00h	See “INCK Setting”.												
3116h	[7:0]	INCKSEL2	28h													
3118h	[7:0]	INCKSEL3	0C0h													
3119h	[2:0]															
311Ah	[7:0]	INCKSEL4	0E0h													
311Bh	[2:0]															
311Eh	[7:0]	INCKSEL5	28h													
3200h to 3BFFh	[7:0]	See “Register Map”.														
4001h	[2:0]	LANEMODE	3h	1h												2-lane
4004h	[7:0]	TXCLKESC_FREQ	1290h	See “INCK Setting”.												
4005h	[7:0]															
400Ch	[0]	INCKSEL6	1h													
4018h	[7:0]	TCLKPOST	00B7h	0067h		006Fh	007Fh		008Fh		009Fh	00B7h		00D7h		Global timing
4019h	[7:0]															
401Ah	[7:0]	TCLKPREPARE	0067h	0027h		002Fh	0037h		004Fh		0057h	0067h		007Fh		Global timing
401Bh	[7:0]															
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h		002Fh	0037h		0047h		0057h	006Fh		007Fh		Global timing
401Dh	[7:0]															
401Eh	[7:0]	TCLKZERO	01DFh	00B7h		00BFh	00F7h		0137h		0187h	01DFh		0237h		Global timing
401Fh	[7:0]															
4020h	[7:0]	THSPREPARE	006Fh	002Fh		002Fh	003Fh		004Fh		005Fh	006Fh		0087h		Global timing
4021h	[7:0]															
4022h	[7:0]	THSZERO	00CFh	004Fh		0057h	006Fh		0087h		00A7h	00CFh		00EFh		Global timing
4023h	[7:0]															
4024h	[7:0]	THSTRAIL	006Fh	002Fh		002Fh	003Fh		004Fh		005Fh	006Fh		0087h		Global timing
4025h	[7:0]															
4026h	[7:0]	THSEXIT	00B7h	0047h		004Fh	005Fh		007Fh		0097h	00B7h		00DFh		Global timing
4027h	[7:0]															
4028h	[7:0]	TLPX	005Fh	0027h		0027h	002Fh		003Fh		004Fh	005Fh		006Fh		Global timing
4029h	[7:0]															
4074h	[2:0]	INCKSEL7	0h	See “INCK Setting”.												

Address	bit	Register name	Initial value	CSI-2 serial 4-lane																		Remarks
				12	10	12	10	12	10	12	10	12	10	12	10	12	10	12	10	10		Bit width
				20	25	25	30.01	30		30	50	30.01	60.03	30	60	60		60		90.16		[frame/s]
				594		720		891		1188		1440		1485		1782		2079		2376		[Mbps/lane]
				22.3	17.8	17.8	14.9	14.9		14.9	8.9	14.9	7.5	10.2	7.5	7.5		7.5		5.0		1H period [μs]
3008h 3009h	[7:0] [1:0]	BCWAIT_TIME	0FFh	See “INCK Setting”.																		
300Ah 300Bh	[7:0] [1:0]	CPWAIT_TIME	0B6h																			
301Ch	[3:0]	WINMODE	0h	0h																		All-pixel mode
3022h	[1:0]	ADDMODE	0h	0h																		All-pixel mode
3024h 3025h 3026h	[7:0] [7:0] [3:0]	VMAX	8CAh	8CAh										CE4h	8CAh	8CAh						
3028h 3029h	[7:0] [7:0]	HMAX	226h	672h	528h	500h	42Ah	44Ch		44Ch	294h	42Ah	215h	2EEh	226h	226h		226h		16Eh		
3030h	[0]	HREVERSE	0h	0h or 1h																		0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h or 1h																		0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	0h		0: 10-bit, 1: 12-bit
3032h	[0]	MDBIT	1h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	1h	0h	0h		0: 10-bit, 1: 12-bit
3033h	[3:0]	SYS_MODE	4h	7h		9h		5h		6h		8h		8h		4h		2h		0h		
3115h	[7:0]	INCKSEL1	00h	See “INCK Setting”.																		
3116h	[7:0]	INCKSEL2	28h																			
3118h 3119h	[7:0] [2:0]	INCKSEL3	0C0h																			
311Ah 311Bh	[7:0] [2:0]	INCKSEL4	0E0h																			
311Eh	[7:0]	INCKSEL5	28h																			
3200h to 3BFFh	[7:0]	See “Register Map”.																				
4001h	[2:0]	LANEMODE	3h	3h																		4-lane
4004h 4005h	[7:0] [7:0]	TXCLKESC_FREQ	1290h	See “INCK Setting”.																		
400Ch	[0]	INCKSEL6	1h																			
4018h 4019h	[7:0] [7:0]	TCLKPOST	00B7h	0067h		006Fh		007Fh		008Fh		009Fh		00A7h		00B7h		00D7h		00E7h		Global timing
401Ah 401Bh	[7:0] [7:0]	TCLKPREPARE	0067h	0027h		002Fh		0037h		004Fh		0057h		0057h		0067h		007Fh		008Fh		Global timing
401Ch 401Dh	[7:0] [7:0]	TCLKTRAIL	006Fh	0027h		002Fh		0037h		0047h		0057h		005Fh		006Fh		007Fh		008Fh		Global timing
401Eh 401Fh	[7:0] [7:0]	TCLKZERO	01DFh	00B7h		00BFh		00F7h		0137h		0187h		0197h		01DFh		0237h		027Fh		Global timing
4020h 4021h	[7:0] [7:0]	THSPREPARE	006Fh	002Fh		002Fh		003Fh		004Fh		005Fh		005Fh		006Fh		0087h		0097h		Global timing
4022h 4023h	[7:0] [7:0]	THSZERO	00CFh	004Fh		0057h		006Fh		0087h		00A7h		00AFh		00CFh		00EFh		010Fh		Global timing
4024h 4025h	[7:0] [7:0]	THSTRAIL	006Fh	002Fh		002Fh		003Fh		004Fh		005Fh		005Fh		006Fh		0087h		0097h		Global timing
4026h 4027h	[7:0] [7:0]	THSEXIT	00B7h	0047h		004Fh		005Fh		007Fh		0097h		009Fh		00B7h		00DFh		00F7h		Global timing
4028h 4029h	[7:0] [7:0]	TLPX	005Fh	0027h		0027h		002Fh		003Fh		004Fh		004Fh		005Fh		006Fh		007Fh		Global timing
4074h	[2:0]	INCKSEL7	0h	See “INCK Setting”.																		



Pixel Array Image Drawing in All-pixel Mode



Drive Timing Chart for All-pixel Mode

Horizontal/Vertical 2/2-line Binning Mode

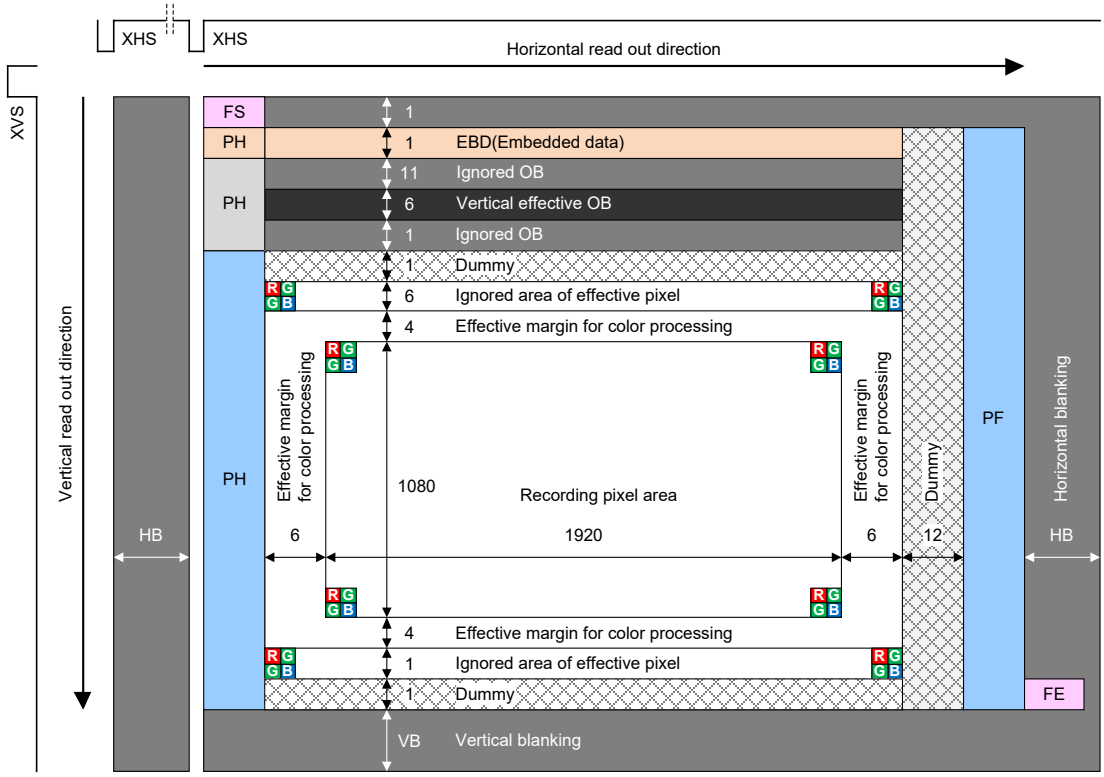
List of Setting Registers

Address	bit	Register name	Initial value	CSI-2 serial 2-lane				Remarks
				AD conversion 10-bit and sensor output 12-bit				Bit width
				10	15	30	30	[frame/s]
				594	891	1782	2079	[Mbps/lane]
				44.5	29.7	14.9	14.9	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	See “INCK Setting”.				
3009h	[1:0]							
300Ah	[7:0]	CPWAIT_TIME	0B6h					
300Bh	[1:0]							
301Ch	[3:0]	WINMODE	0h	0h				All-pixel mode
3020h	[0]	HADD	0h	1h				Horizontal 2 binning
3021h	[0]	VADD	0h	1h				Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h				H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh				
3025h	[7:0]							
3026h	[3:0]							
3028h	[7:0]	HMAX	226h	CE4h	898h	44Ch	44Ch	
3029h	[7:0]							
3030h	[0]	HREVERSE	0h	0h or 1h				0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h or 1h				0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h				10-bit
3032h	[0]	MDBIT	1h	1h				12-bit
3033h	[3:0]	SYS_MODE	4h	7h	5h	4h	2h	
30D9h	[4:0]	DIG_CLP_VSTART	06h	02h				H/V 2/2-line binning
30DAh	[1:0]	DIG_CLP_VNUM	2h	1h				H/V 2/2-line binning
3115h	[7:0]	INCKSEL1	00h	See “INCK Setting”.				
3116h	[7:0]	INCKSEL2	28h					
3118h	[7:0]	INCKSEL3	0C0h					
3119h	[2:0]							
311Ah	[7:0]	INCKSEL4	0E0h					
311Bh	[2:0]							
311Eh	[7:0]	INCKSEL5	28h					
3200h to 3BFFh	[7:0]	See “Register Map”.						
4001h	[2:0]	LANEMODE	3h	1h				2-lane
4004h	[7:0]	TXCLKESC_FREQ	1290h	See “INCK Setting”.				
4005h	[7:0]							
400Ch	[0]	INCKSEL6	1h					
4018h	[7:0]	TCLKPOST	00B7h	0067h	007Fh	00B7h	00D7h	Global timing
4019h	[7:0]							
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	0037h	0067h	007Fh	Global timing
401Bh	[7:0]							
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	0037h	006Fh	007Fh	Global timing
401Dh	[7:0]							
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00F7h	01DFh	0237h	Global timing
401Fh	[7:0]							
4020h	[7:0]	THSPREPARE	006Fh	002Fh	003Fh	006Fh	0087h	Global timing
4021h	[7:0]							
4022h	[7:0]	THSZERO	00CFh	004Fh	006Fh	00CFh	00EFh	Global timing
4023h	[7:0]							

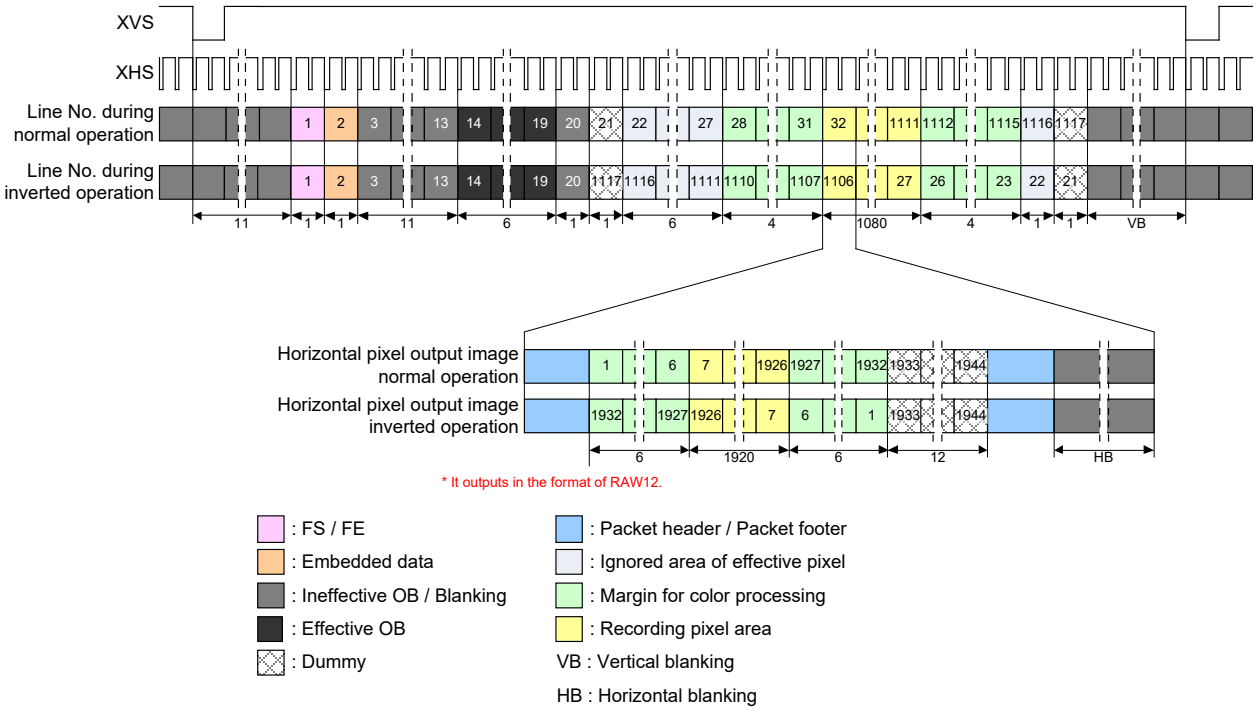
Address	bit	Register name	Initial value	CSI-2 serial 2-lane				Remarks
				AD conversion 10-bit and sensor output 12-bit				Bit width
				10	15	30	30	[frame/s]
				594	891	1782	2079	[Mbps/lane]
4024h	[7:0]	THSTRAIL	006Fh	002Fh	003Fh	006Fh	0087h	Global timing
4025h	[7:0]							
4026h	[7:0]	THSEXIT	00B7h	0047h	005Fh	00B7h	00DFh	Global timing
4027h	[7:0]							
4028h	[7:0]	TLPX	005Fh	0027h	002Fh	005Fh	006Fh	Global timing
4029h	[7:0]							
4074h	[2:0]	INCKSEL7	0h	See “INCK Setting”.				

Address	bit	Register name	Initial value	CSI-2 serial 4-lane						Remarks
				AD conversion 10-bit and sensor output 12-bit						Bit width
				20	25	30	30.01	60	60	[frame/s]
				594	720	891	1440	1782	2079	[Mbps/lane]
				22.3	17.8	14.9	14.9	7.5	7.5	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	See “INCK Setting”.						
3009h	[1:0]									
300Ah	[7:0]	CPWAIT_TIME	0B6h							
300Bh	[1:0]									
301Ch	[3:0]	WINMODE	0h	0h						All-pixel mode
3020h	[0]	HADD	0h	1h						Horizontal 2 binning
3021h	[0]	VADD	0h	1h						Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h						H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh						
3025h	[7:0]									
3026h	[3:0]									
3028h	[7:0]	HMAX	226h	672h	500h	44Ch	42Ah	226h	226h	
3029h	[7:0]									
3030h	[0]	HREVERSE	0h	0h or 1h						0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h or 1h						0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h						10-bit
3032h	[0]	MDBIT	1h	1h						12-bit
3033h	[3:0]	SYS_MODE	4h	7h	9h	5h	8h	4h	2h	
30D9h	[4:0]	DIG_CLP_VSTART	06h	02h						H/V 2/2-line binning
30DAh	[1:0]	DIG_CLP_VNUM	2h	1h						H/V 2/2-line binning
3115h	[7:0]	INCKSEL1	00h	See “INCK Setting”.						
3116h	[7:0]	INCKSEL2	28h							
3118h	[7:0]	INCKSEL3	0C0h							
3119h	[2:0]									
311Ah	[7:0]	INCKSEL4	0E0h							
311Bh	[2:0]									
311Eh	[7:0]	INCKSEL5	28h							
3200h to 3BFFh	[7:0]	See “Register Map”.								
4001h	[2:0]	LANEMODE	3h	3h						4-lane
4004h	[7:0]	TXCLKESC_FREQ	1290h	See “INCK Setting”.						
4005h	[7:0]									
400Ch	[0]	INCKSEL6	1h							
4018h	[7:0]	TCLKPOST	00B7h	0067h	006Fh	007Fh	009Fh	00B7h	00D7h	Global timing
4019h	[7:0]									
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	002Fh	0037h	0057h	0067h	007Fh	Global timing
401Bh	[7:0]									
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	002Fh	0037h	0057h	006Fh	007Fh	Global timing
401Dh	[7:0]									
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00BFh	00F7h	0187h	01DFh	0237h	Global timing
401Fh	[7:0]									
4020h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	003Fh	005Fh	006Fh	0087h	Global timing
4021h	[7:0]									
4022h	[7:0]	THSZERO	00CFh	004Fh	0057h	006Fh	00A7h	00CFh	00EFh	Global timing
4023h	[7:0]									

Address	bit	Register name	Initial value	CSI-2 serial 4-lane						Remarks
				AD conversion 10-bit and sensor output 12-bit						Bit width
				20	25	30	30.01	60	60	[frame/s]
				594	720	891	1440	1782	2079	[Mbps/lane]
4024h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	003Fh	005Fh	006Fh	0087h	Global timing
4025h	[7:0]									
4026h	[7:0]	THSEXIT	00B7h	0047h	004Fh	005Fh	0097h	00B7h	00DFh	Global timing
4027h	[7:0]									
4028h	[7:0]	TLPX	005Fh	0027h	0027h	002Fh	004Fh	005Fh	006Fh	Global timing
4029h	[7:0]									
4074h	[2:0]	INCKSEL7	0h	See “INCK Setting”.						



Pixel Array Image Drawing in Horizontal/Vertical 2/2-line Binning Mode



Drive Timing Chart for Horizontal/Vertical 2/2-line Binning Mode

Pixels that are binned in the inverted operation are pixels that are shifted by one pixel among the same color as compared to pixels that are binned in the normal operation. For example, for consecutive red pixels R1, R2, and R3, R1 and R2 are binned in the normal operation, while R2 and R3 are binned in the inverted operation.

Window Cropping Mode

In Window cropping mode, sensor signals are cropped and read out at an arbitrary position and width. This mode supports Horizontal / Vertical, normal / inverted readout mode for each of All-pixel mode, Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR and Digital overlap HDR.

The cropping area is designated by the cropping start position and width. The start position of the effective pixels including the dummy becomes the origin (0, 0) for specifying the cropping start position. The cropping start position is specified by the offset from the origin.
For the horizontal period after cropping, use the same value as the horizontal period for the drive mode before cropping. Pixels cropped by horizontal cropping are output left aligned. This extends the horizontal blanking period.
Use the cropping position and width fixed. (An invalid frame will be output when the cropping position or width is changed.)

Window cropping image is shown in the figure below.
When the setting values of cropping start position and width are the same, the same physical pixel area as All-pixel mode will be cropped in Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR, and Digital overlap HDR.
In the inverted mode, the readout operates so that it becomes the same “Recording pixel with Effective margin for color processing” area (green rectangle in the figure below) as in the normal mode.

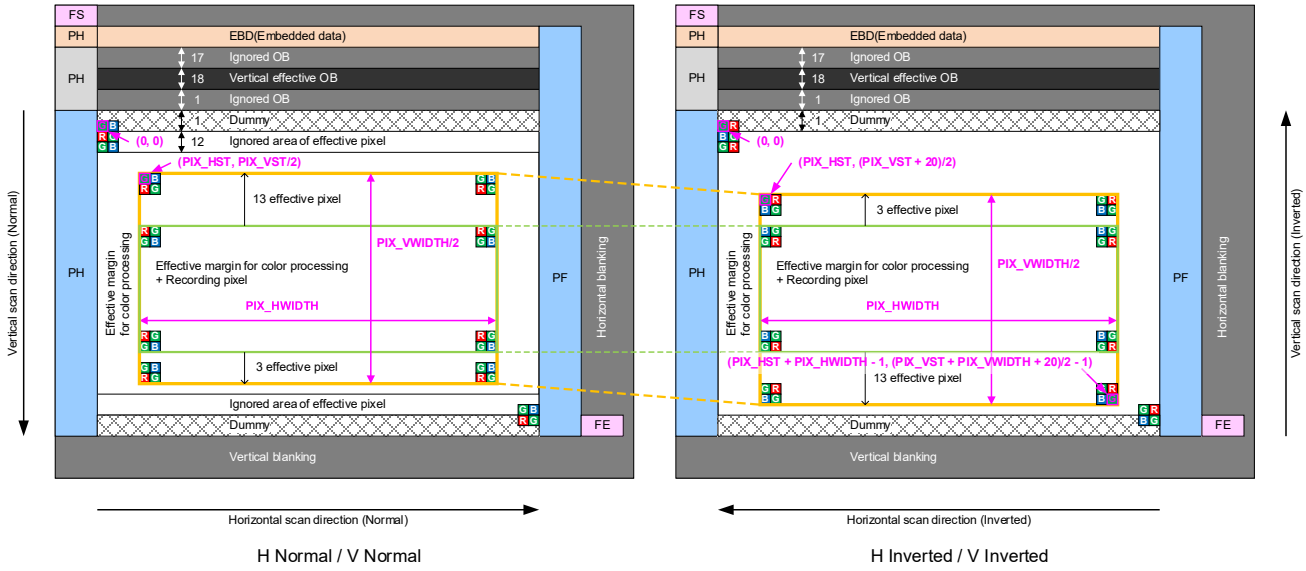


Image Drawing of Window Cropping Mode in Horizontal / Vertical, Normal / Inverted Direction

Supplement) In the inverted mode of the Window cropping mode, the first readout pixel color is “G”.

List of Setting Registers

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
WINMODE	301Ch	[3:0]	0h	4h: Window cropping mode	
PIX_HST	3040h	[7:0]	0000h	Effective pixel start position (Horizontal direction)	Set a multiple of 2.
	3041h	[4:0]			
PIX_HWIDTH	3042h	[7:0]	0F18h	Effective pixel cropping width (Horizontal direction)	Set a multiple of 24.
	3043h	[4:0]			
PIX_VST	3044h	[7:0]	0000h	Effective pixel start position (Vertical direction) Designated in V units (Line×2)	Set a multiple of 4.
	3045h	[4:0]			
PIX_VWIDTH	3046h	[7:0]	1120h	Effective pixel cropping width (Vertical direction) Designated in V units (Line×2)	Set a multiple of 4.
	3047h	[4:0]			

Restrictions on Window cropping mode
The register settings must satisfy the following conditions.

◆ WINMODE

Set WINMODE to 4h.

◆ PIX_VST, PIX_VWIDTH

Set PIX_VST and PIX_VWIDTH to multiples of 4.

$PIX\_VST = n_1 \times 4$
$PIX\_VWIDTH = n_2 \times 4$

Since the values of PIX_VST and PIX_VWIDTH are in units of internal V addresses, set PIX_VST and PIX_VWIDTH to twice the desired cropping start position and cropping width.

The range specified by PIX_VST and PIX_VWIDTH must include an extra 13 effective lines in the front and 3 effective lines in the rear in addition to the “Recording pixels with Effective margin for color processing” that you want to crop.

◆ PIX_HST, PIX_HWIDTH

Set PIX_HST to a multiple of 2.
Set PIX_HWIDTH to a multiple of 24.

$PIX\_HST = n_3 \times 2$
$PIX\_HWIDTH = n_4 \times 24$

Where n_1 to n_4 are integers greater than or equal to 0.

◆ V_{TTL}

V_{TTL} (length of one frame in line units or VMAX) ≥ (PIX_VWIDTH / 2) + 46

Set V_{TTL} to 1222 or higher.

$V_{TTL} \geq 1222$

◆ Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))
1H period (set in units [s]) : Set a value greater than or equal to the “1H period” of the mode before cropping in the “Operating Modes” table.

Description of Various Functions

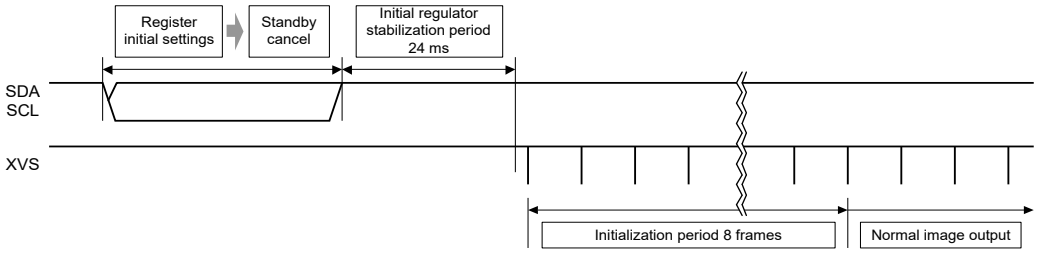
Standby Mode

This sensor stops its operation and goes into standby mode which reduces power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
STANDBY	3000h	[0]	1h	1h: Standby 0h: Operating	Register communication is possible even during standby.

The values of serial communication registers are retained even in standby mode, and the register values can be overwritten by serial communication. Therefore, standby mode can be canceled by setting the STANDBY register to “0”. After standby mode is canceled, it takes 24 ms for the internal regulator stabilization. After that, the frame output starts. Normal frames are output from the 9th frame.
For a detailed sequence of setting and canceling standby mode, see the section of “Sensor Setting Flow”.



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER register. Establish the XMASTER status before canceling standby mode. (Do not switch this register status during operation.)

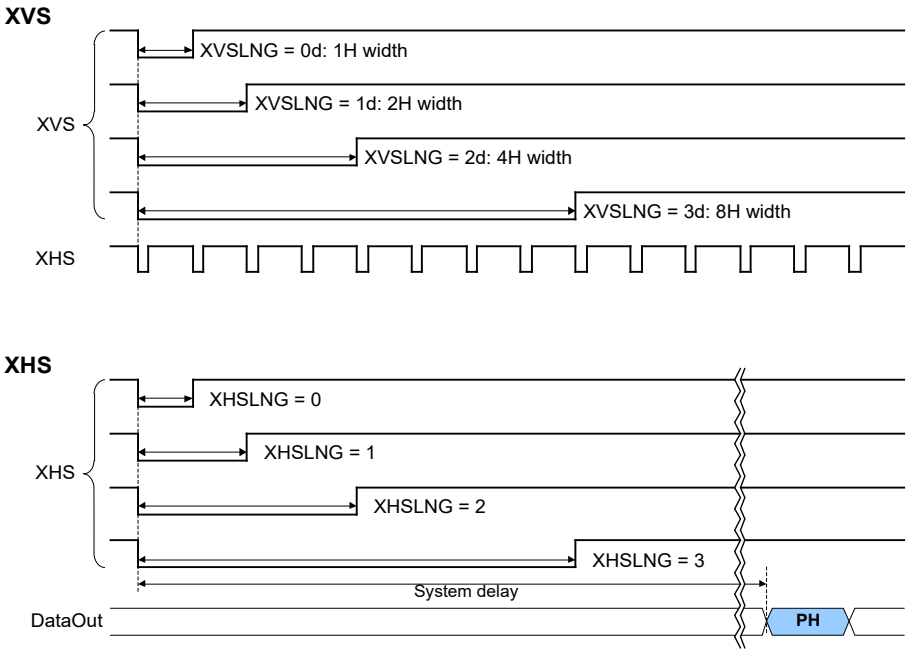
When the sensor is in slave mode, input the vertical sync signal to the XVS pin and the horizontal sync signal to the XHS pin. The vertical sync signal interval should be equal to the number of lines per frame, and the horizontal sync signal interval should be 1H period determined for each operating mode. See the section of “Details of Each Readout Drive Mode” for the number of lines per frame and 1H period.
After setting the master mode, set the register XMSTA to 0h to start the operation. In the master mode, the interval of the vertical sync signal to be generated is set in the VMAX [19:0] register in line units, and the interval of the horizontal sync signal is set in the HMAX [15:0] register in clock units. See the section of “Details of Each Readout Drive Mode” for details on setting each operating mode.

Register to Select Slave Mode or Master Mode

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMASTER	3003h	[0]	0h	0h: Master mode 1h: Slave mode	

List of Setting Registers in Master Mode

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMSTA	3002h	[0]	1h	1h: Master operation ready 0h: Master operation start	The master operation starts by setting 0.
VMAX [19:0]	3024h	[7:0]	008CAh	See the section of “Details of Each Readout Drive Mode”.	Number of lines per frame designated.
	3025h	[7:0]			
	3026h	[3:0]			
HMAX [15:0]	3028h	[7:0]	0226h	See the section of “Details of Each Readout Drive Mode”.	Number of clocks per line designated.
	3029h	[7:0]			
XVSOUTSEL [1:0]	30C0h	[1:0]	2h	0h: Fixed to Low 2h: VSYNC output	
XHSOUTSEL [1:0]		[3:2]	2h	0h: Fixed to Low 2h: HSYNC output	
XVS_DRV [1:0]	30C1h	[1:0]	3h	0h: XVS output (master mode) 3h: Hi-Z (slave mode)	
XHS_DRV [1:0]		[3:2]	3h	0h: XHS output (master mode) 3h: Hi-Z (slave mode)	
XVSLNG [1:0]	30CCh	[5:4]	0h	0h: 1H, 1h: 2H, 2h: 4H, 3h: 8H	XVS low level pulse width designated.
XHSLNG [1:0]	30CDh	[5:4]	0h	0h: 16 clocks, 1h: 32 clocks 2h: 64 clocks, 3h: 128 clocks See the next.	XHS low level pulse width designated.



XVS and XHS Output Waveforms in Sensor Master Mode

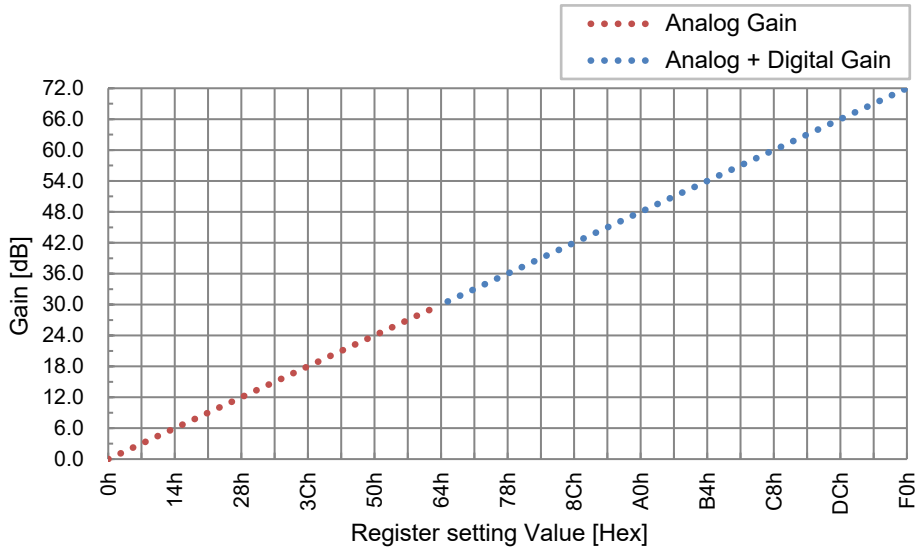
XVS and XHS are output when the register XMSTA is set to 0. If XMSTA is set to 0 during standby, XVS and XHS are output just after canceling standby. The XVS and XHS are output asynchronously with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync code output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this sensor consists of an analog part and a digital part. By setting the register GAIN_PGC_0 [8:0], it is possible to set a maximum of 72 dB in total of analog gain and digital gain. The setting is common to all colors.

Set the register to a value that is 10/3 times the desired gain value. (0.3 dB step)

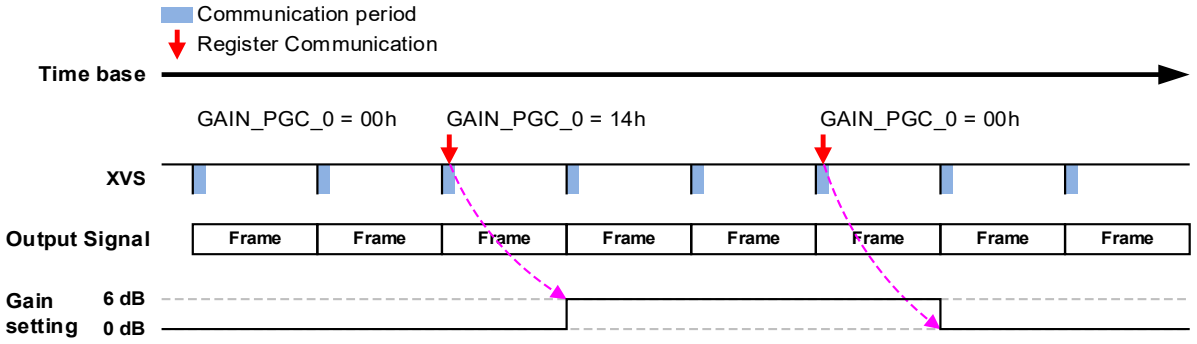
Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN_PGC_0 = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN_PGC_0 = 2Ah



List of PGC Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit		Setting range	
GAIN_PGC_0 [8:0]	3090h	[7:0]	000h	00h-F0h (0d-240d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	3091h	[0]			

As shown below, the gain setting is reflected in the frame that is delayed by one frame from the communication.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added to the data for which the digital gain modulation has been performed by the BLKLEVEL [9:0] register.
Note that the offset unit changes depending on the bit width of the pixel data output from the sensor.
When the bit width is 10-bit, increasing the register value by 1h increases the black level by 1 LSB.
When the bit width is 12-bit, increasing the register value by 1h increases the black level by 4 LSB.

* Recommended setting
  10-bit output: 032h (50d in LSB units)
  12-bit output: 032h (200d in LSB units)

List of Black Level Adjustment Register

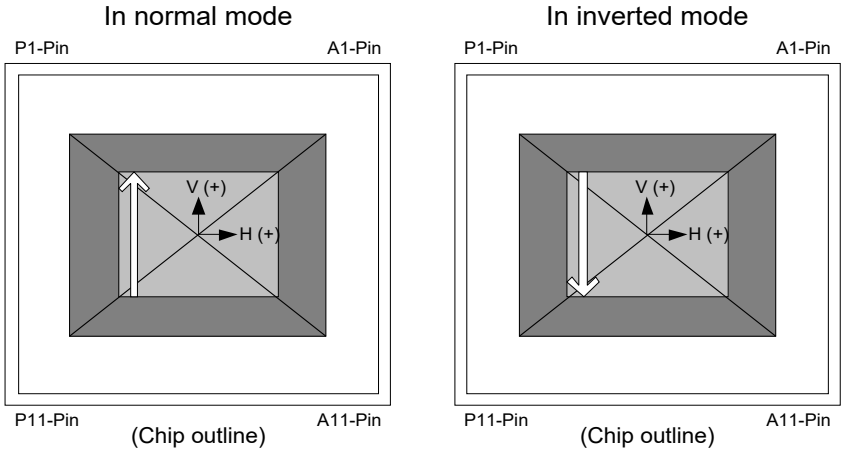
Register	Register details		Initial value	Setting value
	Address	bit		
BLKLEVEL [9:0]	30E2h	[7:0]	032h	000h to 3FFh
	30E3h	[1:0]		

Normal Operation and Inverted Operation

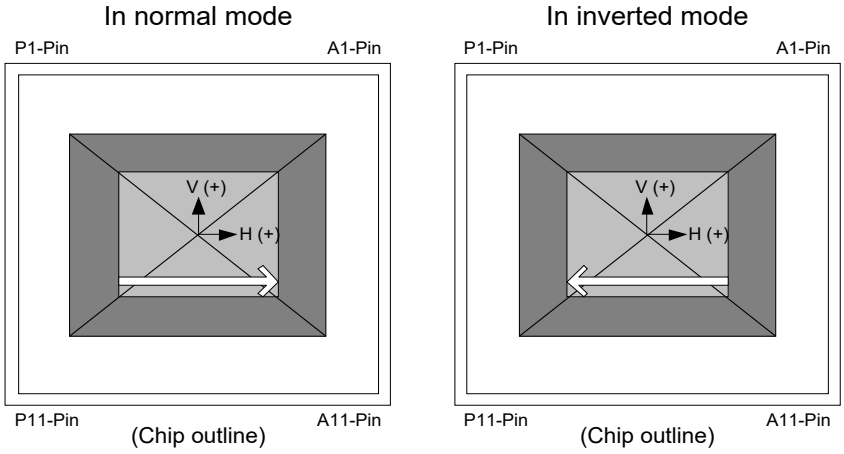
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register and in horizontal direction can be switched by HREVERSE register. See the section of “Details of Each Readout Drive Mode” for the order of readout lines in normal and inverted modes, and for other register settings.
If the vertical readout direction is switched during streaming, one invalid frame occurs, while regarding the horizontal readout direction switching, no invalid frame occurs.

List of Drive Direction Setting Registers

Register	Register details		Initial value	Setting value
	Address	bit		
HREVERSE	3030h	[0]	0h	0h: Normal 1h: Inverted
VREVERSE		[1]	0h	0h: Normal 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Setting

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) The frame that reflects the change in the integration time is output with a delay of one frame from the change.

Calculation of Integration Time

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period – SHR0 × (1H period) + T_{offset}

Where T_{offset} is 1.79 [µs] in AD 10-bit mode and 2.68 [µs] in AD 12-bit mode.

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode and by the register VMAX when the sensor is in master mode. Since the frame period is designated in 1H units, it can be converted into time units using the formula (Number of lines × 1H period).
*2 See the section of “Details of Each Readout Drive Mode” for the 1H period.

In the following pages, the shutter operation and integration time are shown as in the figure below with the time sequence on the horizontal axis and the vertical addresses on the vertical axis. In the figures on the following pages, the shutter and readout operations are depicted as lines for simplicity.

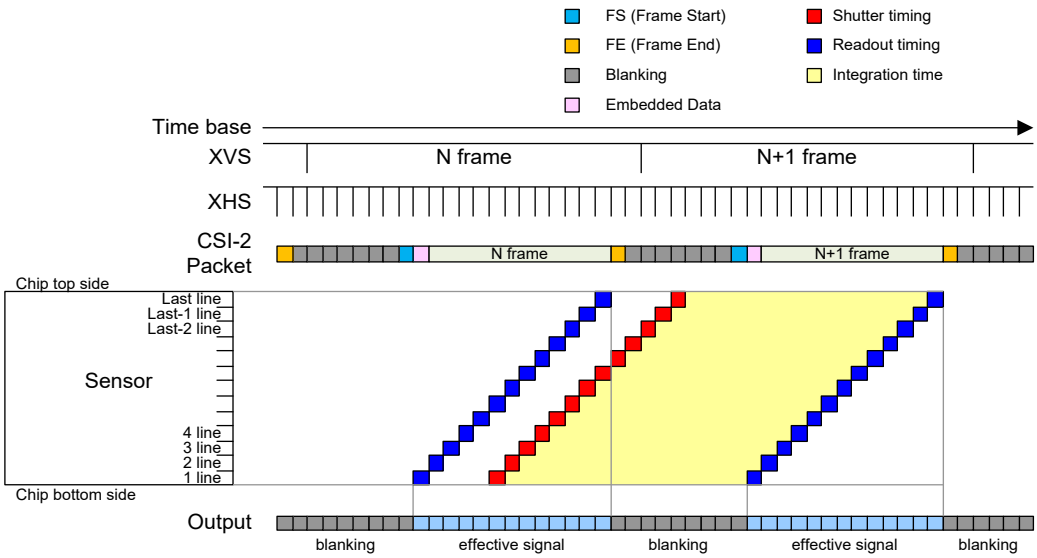


Image Drawing of Shutter Operation

Normal Exposure Operation

The integration time can be controlled by changing the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 8 and (Number of lines per frame – 4). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), with the input XHS interval being one line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [19:0] register.
The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time

Register	Register details		Initial value	Setting value
	Address	bit		
SHR0 [19:0]	3050h	[7:0]	00066h	Shutter sweep time. 8 to (Number of lines per frame – 4). * Others: Setting prohibited.
	3051h	[7:0]		
	3052h	[3:0]		
VMAX [19:0]	3024h	[7:0]	008CAh	Number of lines per frame. Valid only in master mode. See section “Details of Each Readout Drive Mode” for the setting value of each mode.
	3025h	[7:0]		
	3026h	[3:0]		

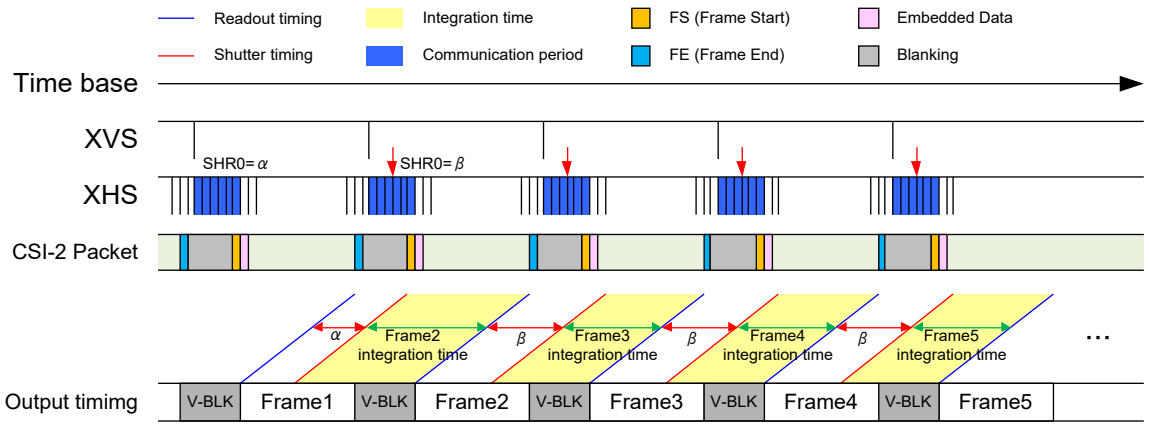


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, this is done by setting register VMAX [19:0] to a value greater than in normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

The maximum exposure time in long exposure operation varies depending on the mode, but it is approximately 1 s. If a value that exceeds the number of V lines for each operating mode described in the “Details of Each Readout Drive Mode” section is set, the imaging characteristics are not guaranteed during long exposure operation.

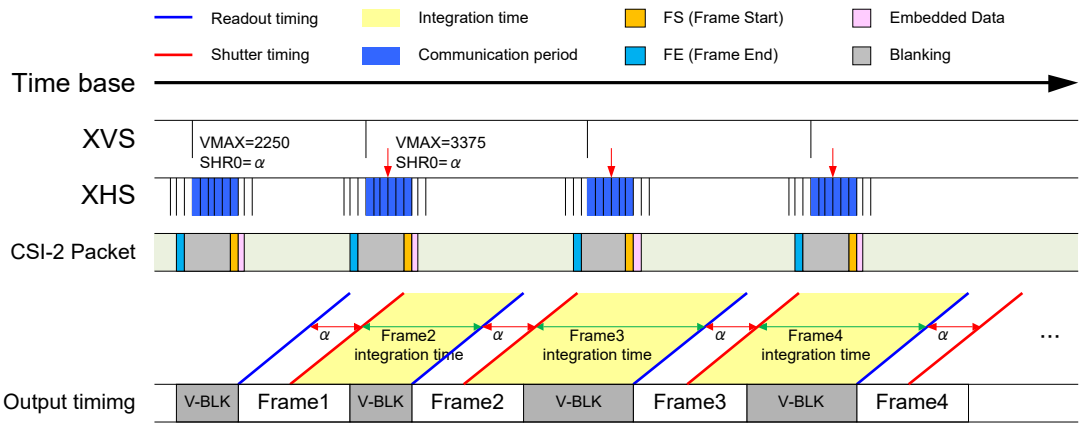


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register settings for controlling the integration time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time
	VMAX*	SHR0**	
All-pixel scan mode	2250	2246	$4H + T_{offset}$
		⋮	⋮
		N	$(2250 – N) H + T_{offset}$
		⋮	⋮
		8	$2242H + T_{offset}$

Where T_{offset} is 1.79 [µs] in AD 10-bit mode and 2.68 [µs] in AD 12-bit mode.

* VMAX is valid only in master mode. In slave mode, XVS input interval is used instead of VMAX.
** The range of SHR0 (N) is “8” to “VMAX (M) – 4”.

CSI-2 Output

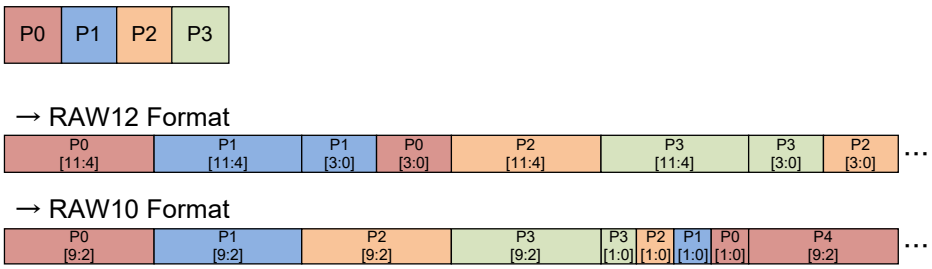
This sensor supports the following output modes and output formats.

CSI-2 serial 2-lane / 4-lane, RAW10 / RAW12

The following describes the 2-lane / 4-lane serial signal output method of this sensor.
The image data of this sensor is output according to the CSI-2 interface. There is a total of 4 pairs of pins for the CSI-2 data signal output. The name of each pair is as follows. The DMO1P / DMO1N pair is called “Lane1”. The DMO2P / DMO2N pair is called “Lane2”. The DMO3P / DMO3N pair is called “Lane3”. And the DMO4P / DMO4N pair is called “Lane4”. In addition, the CSI-2 clock signal is output from the DCKP / DCKN pair. This pair is called “Clock Lane”.
In 2-lane mode, data is output from Lane1 and Lane2. In 4-lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The maximum bit rate is 2376 Mbps/lane in 4-lane mode and 2079 Mbps/lane in 2-lane mode.
RAW10 / RAW12 is selectable by register MDBIT [0]. The number of data lanes used can be set by register LANEMODE [2:0].
Unused lanes output according to the MIPI standard.

Register	Register details		Initial value	Setting value
	Address	bit		
MDBIT	3032h	[0]	1h	0h: RAW10 1h: RAW12
LANEMODE [2:0]	4001h	[2:0]	3h	1h: 2-lane 3h: 4-lane

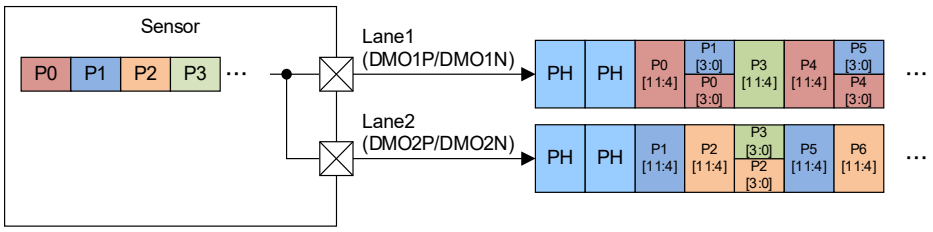
The formats of RAW12 and RAW10 are shown below.



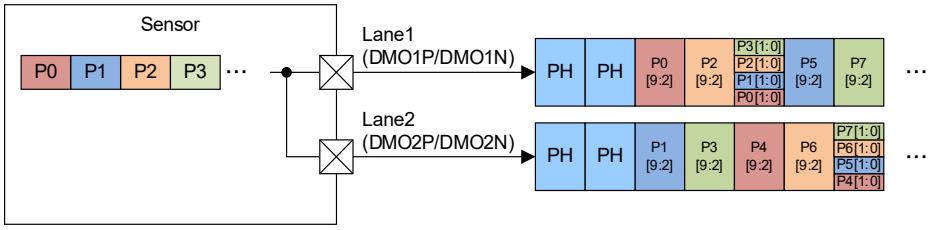
RAW12 / RAW10 Format Example

The output formats of 2-lane and 4-lane are shown below.

a) 2-Lane RAW12

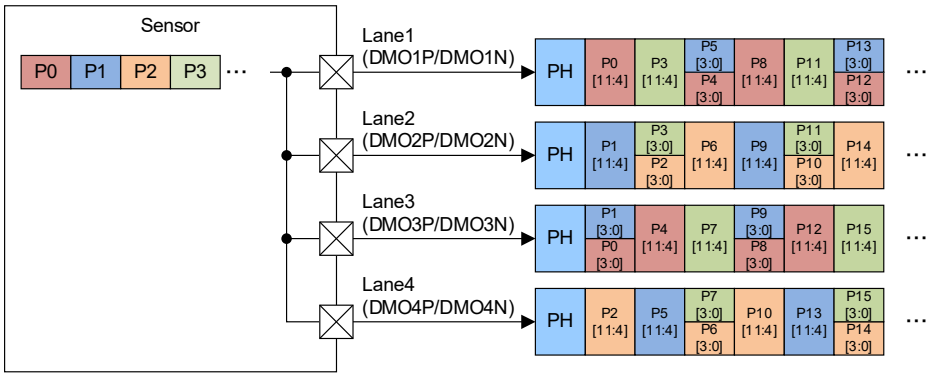


b) 2-Lane RAW10

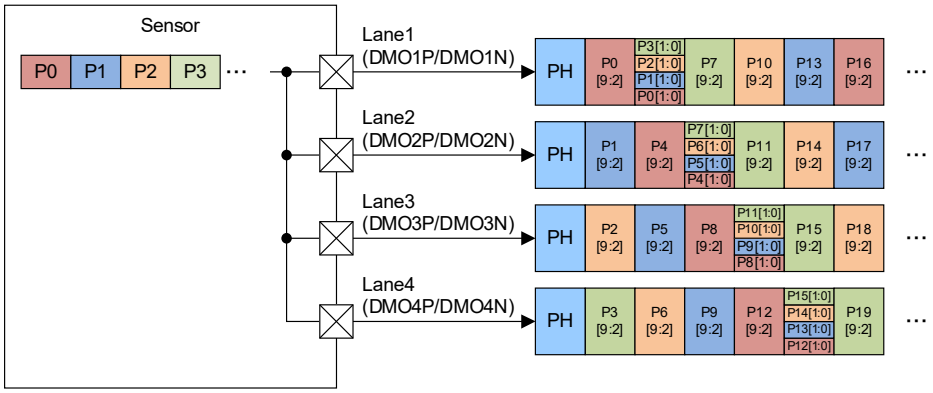


2-Lane Output Format

c) 4-Lane RAW12



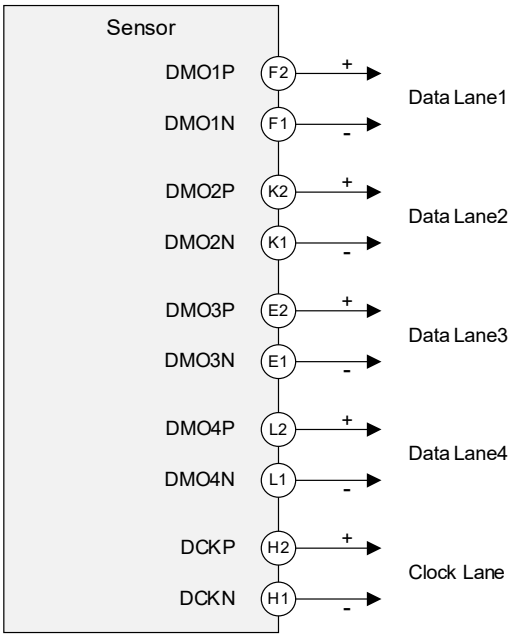
d) 4-Lane RAW10



4-Lane Output Format

MIPI Transmitter

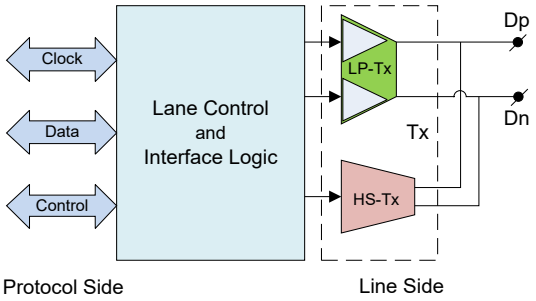
The CSI-2 output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DCKP, DCKN) are described in this page.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-Speed serial interface.
Refer to the MIPI Standard:
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2
・MIPI Alliance Specification for D-PHY Version 1.2

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, place it as close as possible to the Receiver. To avoid malfunction, the spacing between signal lines of a differential pair shall be kept constant, the wiring length difference between signal lines of a differential pair shall be minimum, and usage of meander wiring shall be kept to a minimum. The maximum bit rate of each lane is 2376 Mbps/lane.



Universal Lane Module Functions

Analog-to-Digital Conversion Bit Width Setting

The output bit width of the sensor internal ADC (analog-to-digital converter) can be set to 10-bit or 12-bit by register ADBIT [1:0]. Depending on the operating mode, it may be limited to 10-bit only. See the section of “Readout Drive Modes” for the bit width supported by each operating mode.

List of Analog-to-Digital Conversion Bit Width Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
ADBIT	3031h	[1:0]	1h	0h: 10-bit 1h: 12-bit

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10-bit or 12-bit gradation, and the maximum output value is 3FFh for 10-bit output and FFFh for 12-bit output.
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10-bit	000h	3FFh
12-bit	000h	FFFh

INCK Setting

The available operating modes vary according to the INCK frequency. Use 24 MHz, 27 MHz, 37.125 MHz, 72 MHz, or 74.25 MHz for INCK frequency. The INCK setting registers and the list of INCK settings are shown in the tables below.

In the MIPI Alliance Specification for D-PHY Version 1.2,
when operating above 1500 Mbps, an initial deskew sequence shall be transmitted before High-Speed Data Transmission. When operating at or below 1500 Mbps, the transmission of the initial deskew sequence is optional. When operating at or above 1440 Mbps, this sensor transmits the initial deskew burst.

INCK Setting Registers

Data rate: 2376 Mbps/lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	0h	0h	0h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	108h	100h	100h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 2079 Mbps/lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	2h	2h	2h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0E7h	0E0h	0E0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1782 Mbps/lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	4h	4h	4h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0C6h	0C0h	0C0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1485 Mbps/lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	8h	8h	8h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0A5h	0A0h	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1440 Mbps/lane

Register	Register details		Initial value	INCK	
	Address	bit		24 [MHz]	72 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	054h	0F8h
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	03Bh	0B0h
SYS_MODE	3033h	[3:0]	4h	8h	8h
INCKSEL1	3115h	[7:0]	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0B4h	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0FCh	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	0600h	1200h
INCKSEL6	400Ch	[0]	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h

Data rate: 1188 Mbps/lane

Register	Register details		Initial value	INCK				
	Address	bit		24 [MHz]	27 [MHz]	37.125 [MHz]	72 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	054h	05Dh	07Fh	0F8h	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	03Bh	042h	05Bh	0B0h	0B6h
SYS_MODE	3033h	[3:0]	4h	6h	6h	6h	6h	6h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	24h	23h	24h	28h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0C6h	084h	080h	084h	080h
INCKSEL4	311B-1Ah	[10:0]	0E0h	15Ah	0E7h	0E0h	0E7h	0E0h
INCKSEL5	311Eh	[7:0]	28h	24h	23h	24h	28h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	0600h	06C0h	0948h	1200h	1290h
INCKSEL6	400Ch	[0]	1h	0h	0h	0h	0h	0h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h	0h	0h

Data rate: 891 Mbps/lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	5h	5h	5h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0C6h	0C0h	0C0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	0h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h	1h

Data rate: 720 Mbps/lane

Register	Register details		Initial value	INCK	
	Address	bit		24 [MHz]	72 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	054h	0F8h
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	03Bh	0B0h
SYS_MODE	3033h	[3:0]	4h	9h	9h
INCKSEL1	3115h	[7:0]	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0B4h	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0FCh	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	0600h	1200h
INCKSEL6	400Ch	[0]	1h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h

Data rate: 594 Mbps/lane

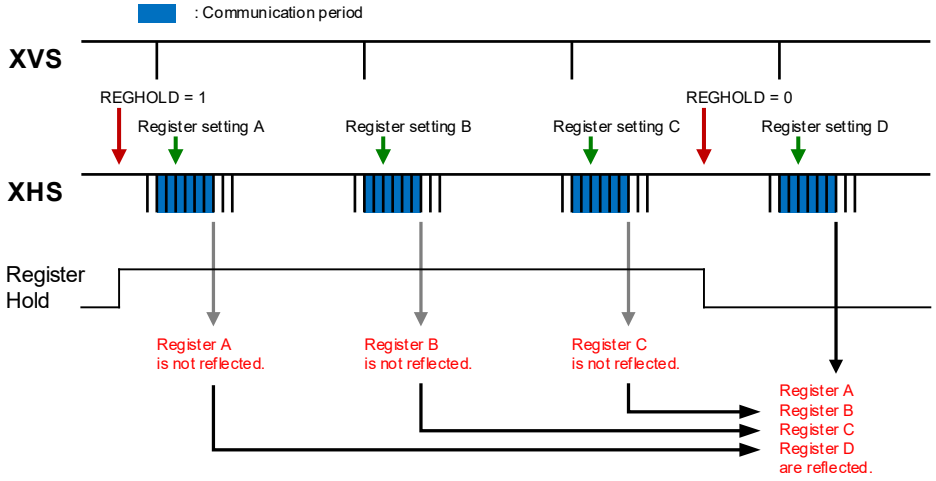
Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3033h	[3:0]	4h	7h	7h	7h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	084h	080h	080h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	0h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h	1h

Register Hold Setting

By using the register REGHOLD, the settings of the frame reflection registers (registers whose reflection timing is “V” in the Register Map) can be transmitted in several frames and reflected in a certain frame at once. Registers set while REGHOLD is 1 are not reflected at the “Frame reflection register reflection timing”. By setting REGHOLD to 0 in the frame where you want to reflect the registers, the registers set while REGHOLD is 1 are reflected at once.

Register Hold Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
REGHOLD	3001h	[0]	0h	0: Invalid 1: Valid (register hold)



Register Hold Setting

Mode Transitions

The transitions between operation modes are shown below. These examples are when setting is completed in one communication period.

List of Mode Transitions

Transition			State
Horizontal direction normal	→	Horizontal direction inverted	Via the standby mode is unnecessary.
Horizontal direction inverted	→	Horizontal direction normal	
All-pixel scan mode	→	Window cropping mode	Via the standby mode is unnecessary. One invalid frame will occur.
Window cropping mode	→	All-pixel scan mode	
Vertical direction normal	→	Vertical direction inverted	
Vertical direction inverted	→	Vertical direction normal	
Vertical direction the number of lines change (Master mode: VMAX change; slave mode: XVS interval change)			
Horizontal direction 1H period change (Master mode: HMAX change; slave mode: XHS interval change)			
- Transitions between modes other than the above - Change the input frequency of INCK *1 - Change the register setting noted “S” in the reflection timing column of the Register Map			Via the standby mode is necessary.

*1 When changing the input INCK frequency, be careful not to input a pulse shorter than the high / low level widths of the preceding and following INCK at the frequency switching. If the above pulse may occur at the INCK switching point, set the XCLR pin to Low level and change the INCK frequency during system reset. Then, set the XCLR pin to High level and perform system clear following the “Power-on Sequence” in the section of “Power-on and Power-off Sequence”. Execute the initial settings again because registers are initialized by system clear.

Other Functions

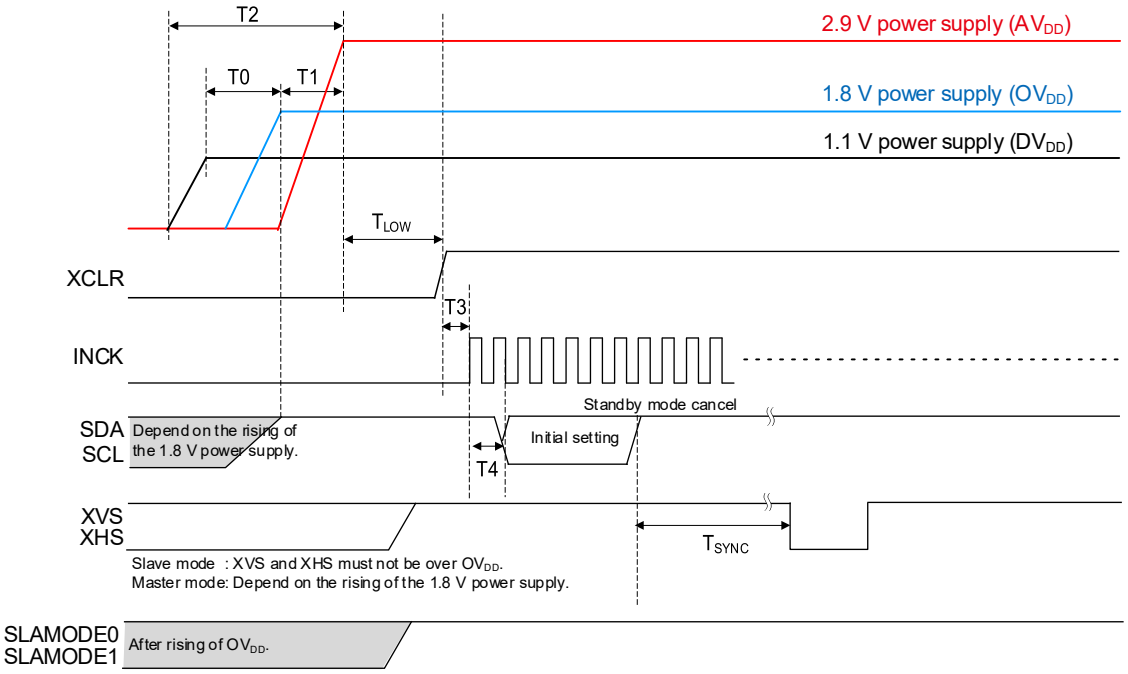
This sensor has the following functions. For details, refer to each application note.

- Digital overlap HDR (2 / 3 frame)
- Multiple exposure HDR (2 / 4 frame)
- Additional Function of Synchronizing Sensors

Power-on and Power-off Sequence

Power-on Sequence

1. Turn on the power supplies so that the power supplies rise in order of 1.1 V power supply (DV_{DD}) → 1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD}). In addition, all the power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
3. The system clear is applied by setting XCLR to High level. Input the master clock after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

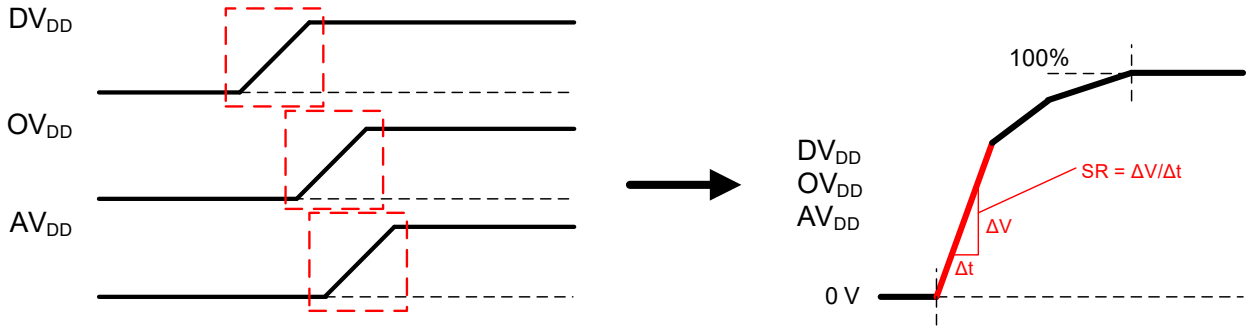


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.1 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supplies	T2	—	200	ms
2.9 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	1	—	µs
Clear OFF → Communication start	T4	20	—	µs
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	24	—	ms

Slew Rate Limitation of Power-on Sequence

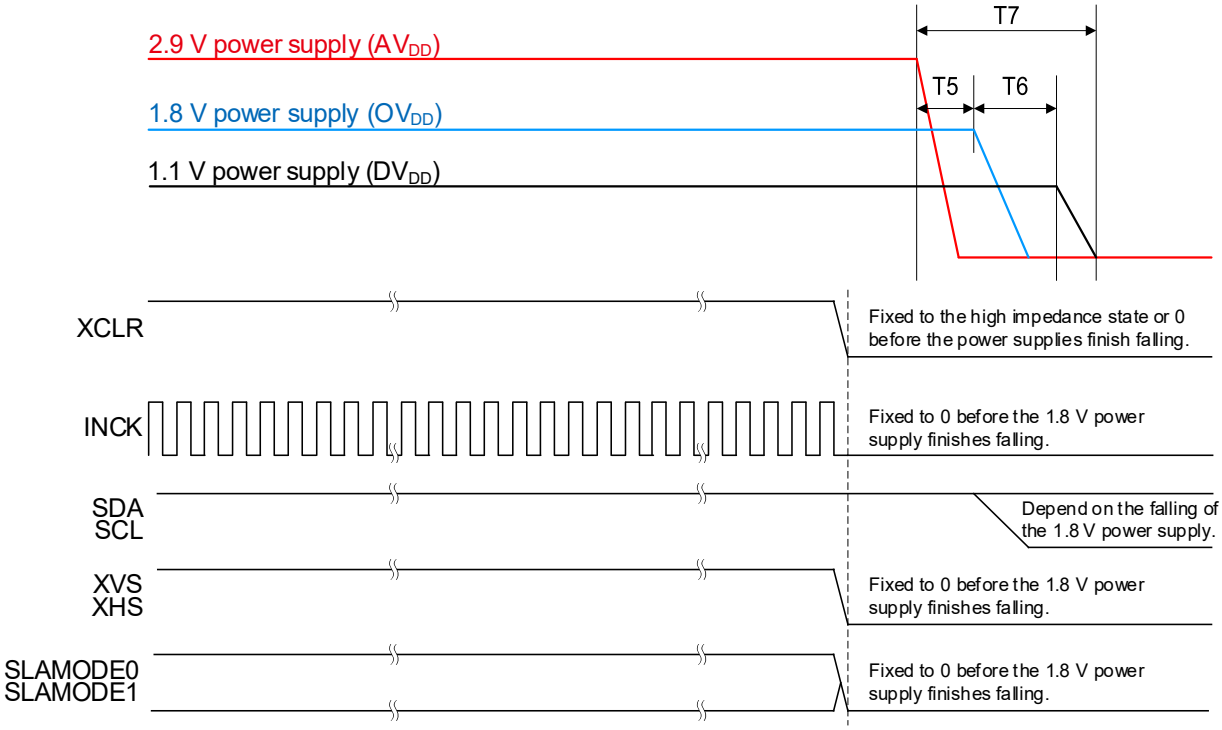
Conform the slew rate limitation shown below while a power supply ramps up from 0 V to 100 % of its voltage in the power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.1 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		AV_{DD} (2.9 V)	—	25	mV/μs	

Power-off Sequence

Turn off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.1 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



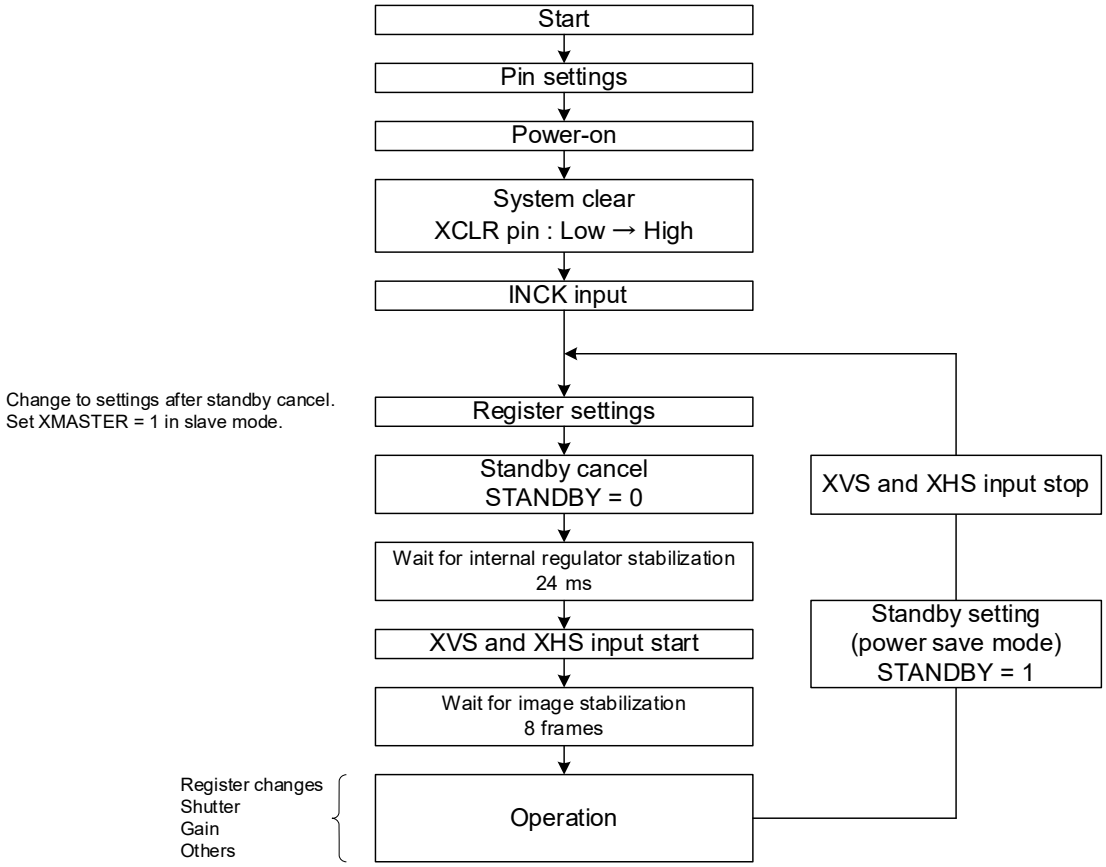
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
2.9 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.1 V power shut down	T6	0	—	ns
Shut down time of all power supplies	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

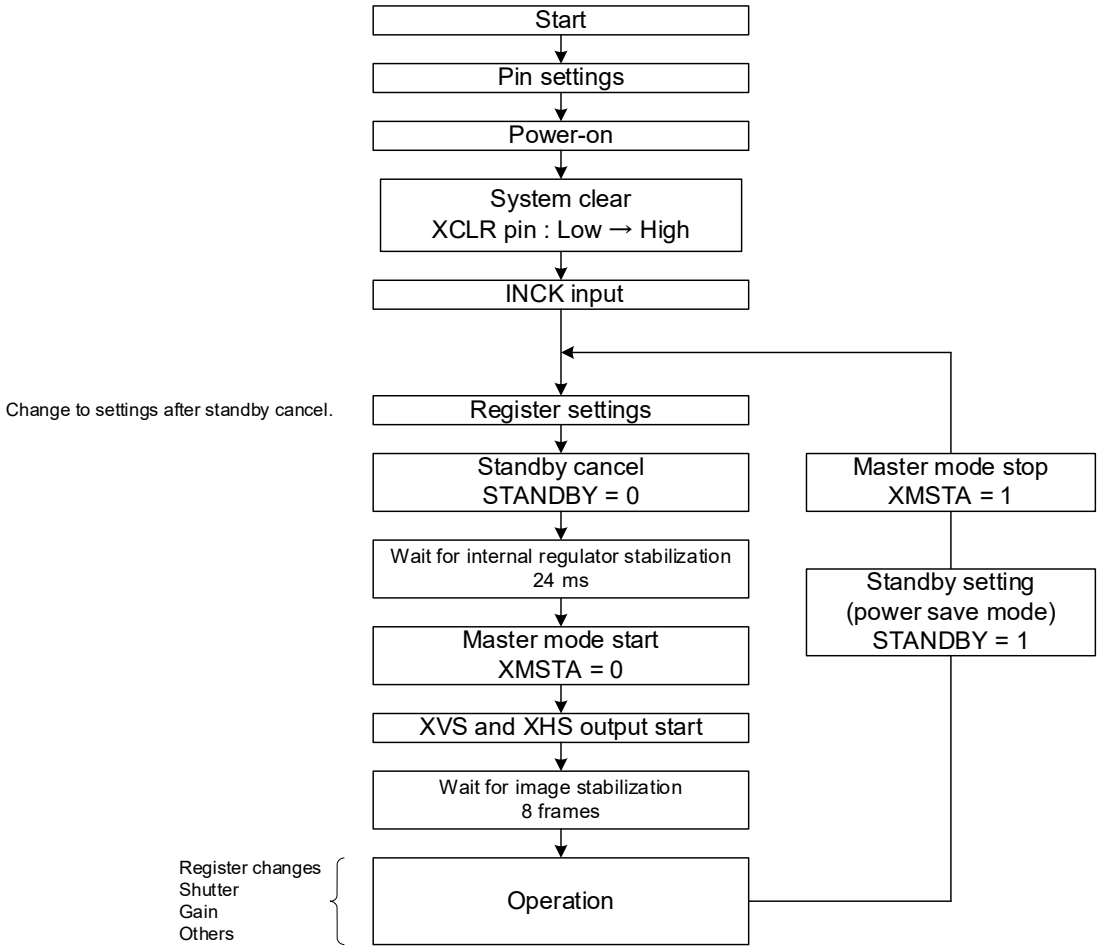
The figure below shows the operating flow in sensor slave mode.
For details from “Power-on” to “System clear”, see the item of “Power-on Sequence” in the section of “Power-on and Power-off Sequence”.
For details from “Standby cancel” to “Wait for image stabilization”, see the item of “Standby Mode” in the section of “Description of Various Functions”.
“Standby setting (power save mode)” can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

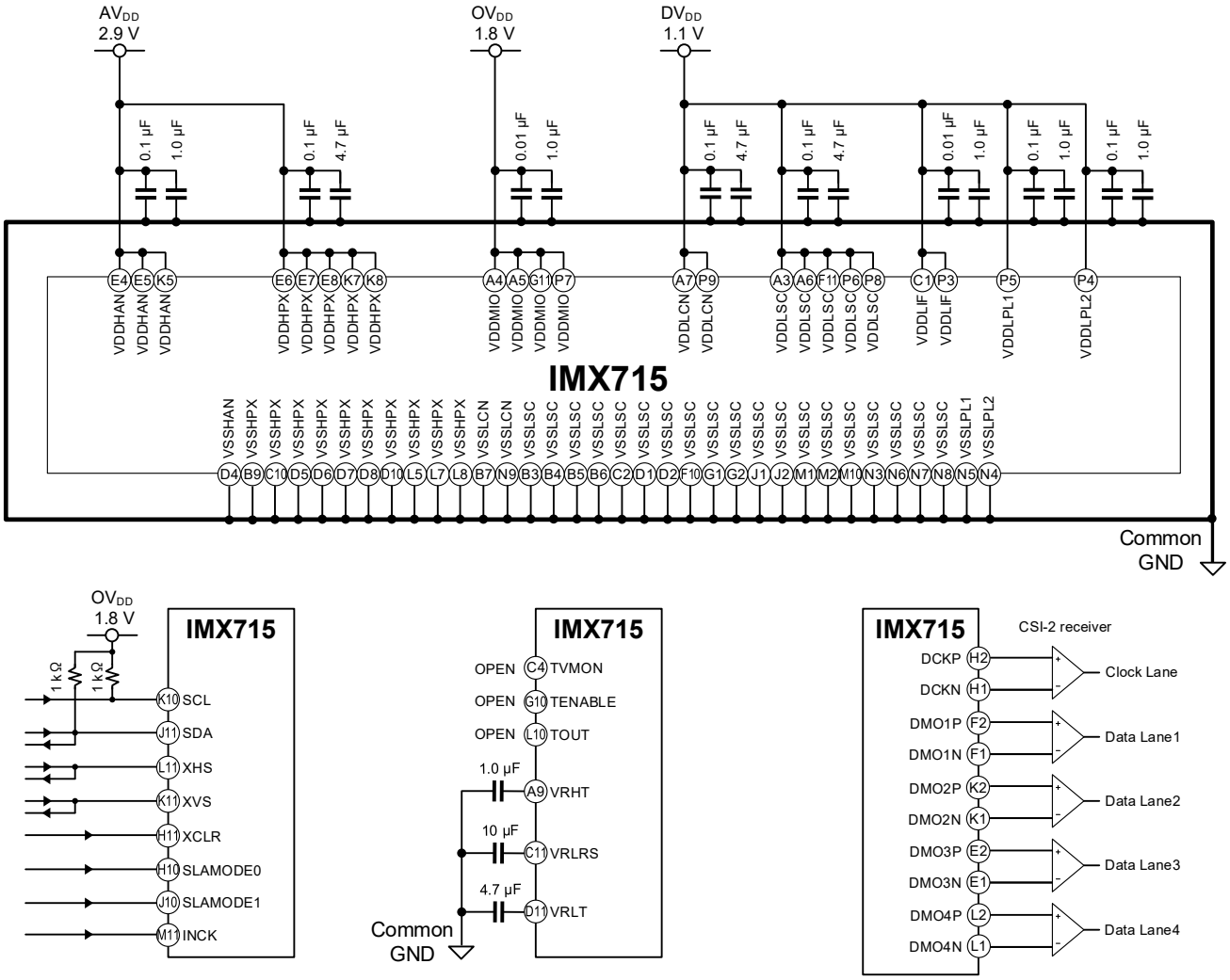
Setting Flow in Sensor Master Mode

The figure below shows the operating flow in sensor master mode.
For details from “Power-on” to “System clear”, see the item of “Power-on Sequence” in the section of “Power-on and Power-off Sequence”.
For details from “Standby cancel” to “Wait for image stabilization”, see the item of “Standby Mode” in the section of “Description of Various Functions”.
In master mode, “Master mode starts” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”.
“Standby setting (power save mode)” can be made by setting the STANDBY register to “1” during “Operation”.
At this time, set “Master mode stop” by setting XMSTA to “1”.



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

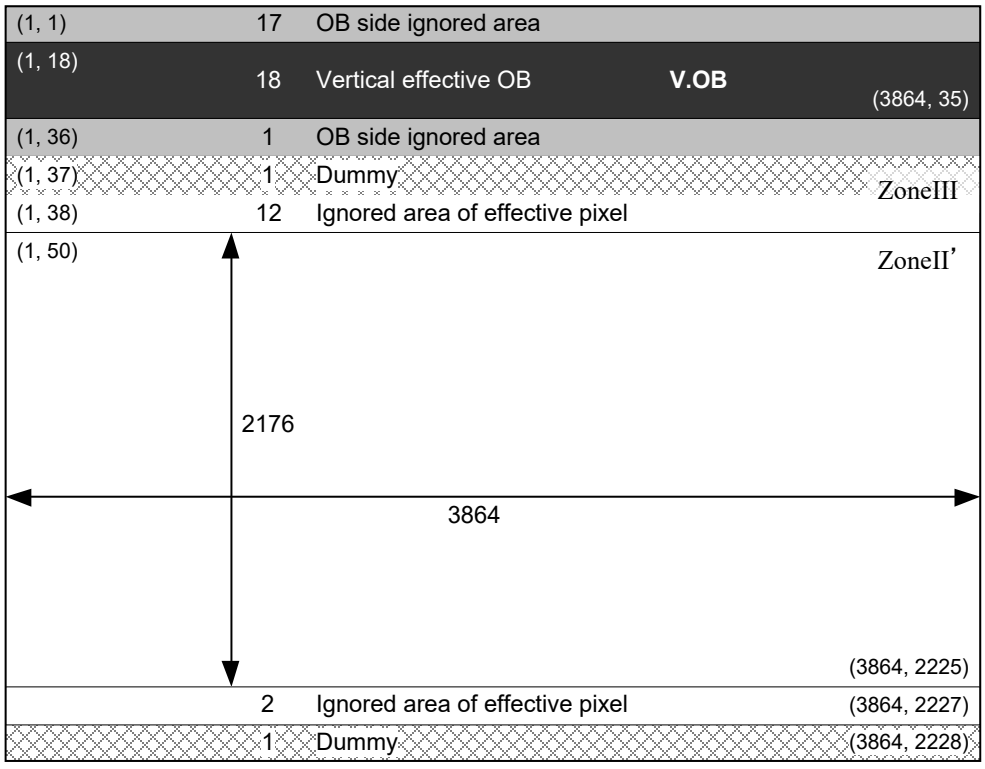
Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	90	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	800		No evaluation criteria applied		2	1/30 s storage

Note) 1. Zone is specified based on the All-pixel drive mode.
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the use of spot pixels that are close to each other.

Zone Definition



Notice on White Pixel Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	27 pcs
10.0 mV or higher	15 pcs
24.0 mV or higher	6 pcs
50.0 mV or higher	3 pcs
72.0 mV or higher	2 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

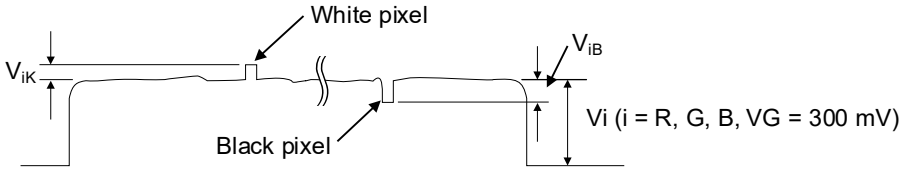
Material_No.03-0.0.10

Measurement Methods for Spot Pixels

After setting to the standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb and Gr signal outputs is 300 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



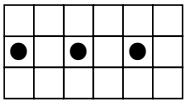
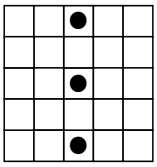
Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

Spot Pixel Pattern Specifications

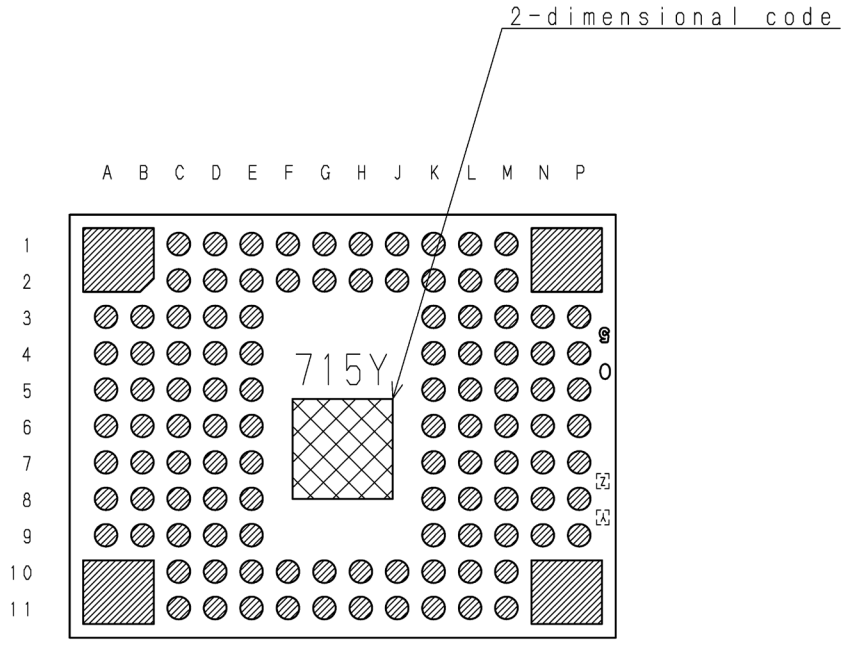
White pixels, black pixels, and bright pixels are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel, and Bright Pixel Patterns

No.	Pattern (R G / G B)	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1. "●" shows the position of white pixel, black pixel, or bright pixel.
Each pattern is defined by three white pixels, three black pixels, or three bright pixels.
(Example: If one black pixel and two white pixels are located like pattern No.1, they are not judged to be rejected.)
2. Products that have one or more rejected patterns are filtered out.
3. All spot pixels are subject to the "Maximum distorted pixels in each zone" judgment in the section of "Spot Pixel Specifications" even if they do not correspond to the patterns in the table above.

Marking



Y:In English upper case character,One character
Z:Number,single number

DRAWING No. AM-C715AAQR1(2D)

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

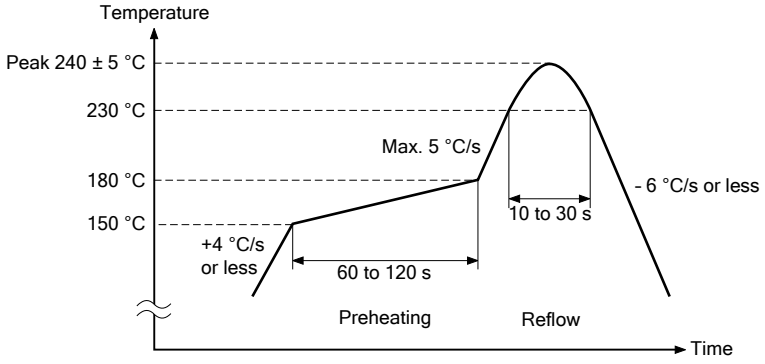
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Recommended temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.
(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

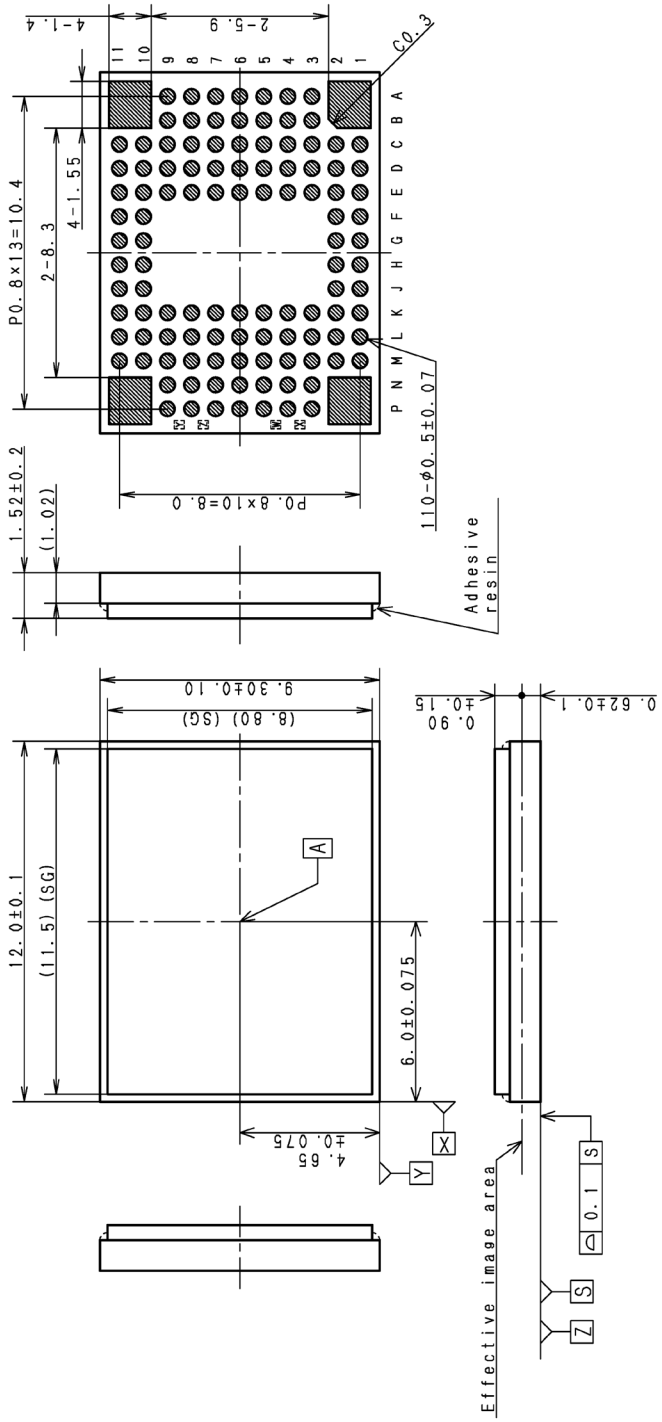
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.
(6) Please perform the tilt adjustment for the optical axis in your company as required.

Package Outline

(Unit:mm)



1) " A " is the center of the effective image area
2) Datum surface " S " is a virtual flat surface calculated at three points (A11 , P1 , P11) of back side terminal
3) The rotation angle of the effective image area relative to " X " and " Y " is ± 1 °
4) The tilt of the effective image area relative to the bottom " Z " is less than 0.05 mm
5) The thickness of the cover glass is 0.5 mm , and the refractive index is 1.5
6) Cover glass:Both is sides AR coat.
7) As for standard for resin overflow in package outside, it shall be accepted up to outermost line tolerance of package.
8) One character of alphabet or number shall be placed from W to Z part.(Plating option)

PACKAGE STRUCTURE

CLASSIFICATION	LGA
LEAD TREATMENT	GOLD PLATING
PIN NUMBER	114pin
PACKAGE WEIGHT(Typ.)	0.44g
DRAWING NUMBER	AS-C110(E)

List of Trademark Logos and Definition Statements

STARVIS

* STARVIS is a registered trademark or trademark of Sony Group Corporation or its affiliates. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for security camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date (Y / M / D)	Rev.	Page	Description
2021 / 05 / 13	0.1	—	First Edition
2021 / 08 / 23	E21804	—	First Edition (Official Edition)
		24	Added: [Old measurement conditions] to standard imaging condition I
		25	Modified: Description of “2. Sensitivity ratio” sensitivity measurement -> sensitivity measurement under the new measurement conditions
		37	Modified: Description of register MDBIT Number of output bits setting -> Bit width setting for pixel data output from the sensor
		48	Corrected: 1H period in mode “All-pixel 2-lane 2079 Mbps/lane 12-bit” 887 -> 884 Added: Mode “All-pixel 4-lane 1485 Mbps/lane 12-bit”
		53	Modified: Section title Image Data Output Format -> Details of Each Readout Drive Mode
		55	Added: Mode “All-pixel 4-lane 1485 Mbps/lane 12-bit”
		70	Corrected: Item title Example of Integration Time Setting -> Calculation of Integration Time Corrected: Description of figures For simplicity, shutter and readout operations are noted in line units. -> In the figures on the following pages, the shutter and readout operations are depicted as lines for simplicity.
		77	Modified: Item title Internal A/D Conversion Bit Width Setting -> Analog-to-Digital Conversion Bit Width Setting Modified: Description of the A/D conversion bit width setting internal A/D conversion bit width -> output bit width of the sensor internal ADC (analog-to-digital converter)
		83	Corrected: Unification of terminologies standby state -> standby mode
		90	Modified: Peripheral Circuit AVDD -> AV_{DD}; OVDD -> OV_{DD}; DVDD -> DV_{DD}; MIPI Rx -> CSI-2 receiver; MIPI Lane -> Data Lane
		95	Update: TBD Marking diagram
		98	Update: TBD Package Outline diagram
2022 / 10 / 31	E21804A2X	1	Deleted: Applications FA cameras, Industrial cameras Added: Features AR coating on cover glass (both sides) Added: Copyright 2022
		23	Deleted: “F5.6” in the Remarks column of G sensitivity (New measurement conditions)
		24	Deleted: Standard imaging condition III
		25	Corrected: Symbol in “1. Sensitivity” Sg -> S Modified: 4. Video signal shading standard imaging condition III -> standard imaging condition II

Date (Y / M / D)	Rev.	Page	Description
		37	Added: Description of register SYS_MODE 6: 1188 Mbps
		48	Added: Operating modes with a data rate of 1188 Mbps/lane
		54 to 55, 57 to 60	Modified: List of Setting Registers table Bit widths were added to table headers, and each column in the table was subdivided by bit width as needed. By doing this, the bit width associated with each frame rate became clearer.
		54 to 55	Added: Register setting examples for a data rate of 1188 Mbps/lane
		54, 55, 57, 59	Corrected: Register name TXCLCKES_FREQ -> TXCLKESC_FREQ
		80	Added: INCK settings for a data rate of 1188 Mbps/lane