

Diagonal 7.857 mm (Type 1/2.3) 12.3Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

**Tentative**

## IMX577-AACK-C

For the latest data sheet, please visit [www.sunnywale.com](http://www.sunnywale.com)

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### Description

IMX577-AACK-C is a diagonal 7.857 mm (Type 1/2.3) 12.3 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.8 V, digital 1.05 V and 1.8 V for input/output interface and achieves low power consumption.

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### Features

- ◆ Back-illuminated and stacked CMOS image sensor Exmor RS
- ◆ Digital Overlap High Dynamic Range (DOL-HDR) mode with raw data output.
- ◆ High signal to noise ratio (SNR).
- ◆ Full resolution @60 frame/s (Normal), 4K2K @60 frame/s (Normal), 1080p @240 frame/s  
Full resolution @40 frame/s (12 bit Normal), Full resolution @30 frame/s (DOL-HDR, 2 frame)
- ◆ Output video format of RAW12/10/8, COMP8.
- ◆ Power Save Mode with MIPI ULPS operation
- ◆ Pixel binning readout and V sub-sampling function.
- ◆ Independent flipping and mirroring.
- ◆ Input clock frequency 6 to 27 MHz
- ◆ CSI-2 serial data output (MIPI 2lane/4lane, Max. 2.1 Gbps/lane, D-PHY spec. ver. 1.2 compliant)
- ◆ 2-wire serial communication.
- ◆ Two PLLs for independent clock generation for pixel control and data output interface.
- ◆ Ambient Light Sensor (ALS)
- ◆ Fast mode transition. (on the fly)
- ◆ Dual sensor synchronization operation (Multi camera compatible)
- ◆ 7 K bit of OTP ROM for users.
- ◆ Built-in temperature sensor
- ◆ 10-bit/12-bit A/D conversion on chip
- ◆ Horizontal Low Power analog Cropping
- ◆ Window Scanning mode
- ◆ 92-pin high-precision ceramic package

## Exmor RS

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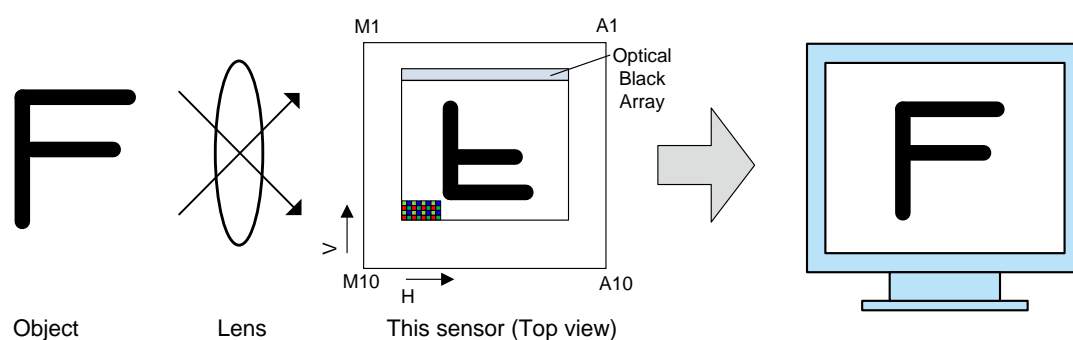
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## Device Structure

◆ CMOS image sensor	
◆ Image size	: Diagonal 7.857 mm (Type 1/2.3)
◆ Total number of pixels	: 4072 (H) × 3176 (V) approx. 12.93 M pixels
◆ Number of effective pixels	: 4072 (H) × 3064 (V) approx. 12.47 M pixels
◆ Number of active pixels	: 4056 (H) × 3040 (V) approx. 12.33 M pixels
◆ Chip size	: 7.564 mm (H) × 5.476 mm (V)
◆ Unit cell size	: 1.55 μm (H) × 1.55 μm (V)
◆ Substrate material	: Silicon

## Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during default readout in the vertical direction and the horizontal direction.

**Figure 1 Optical Black Array and Readout Scan Direction**

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	$V_{ANA}$	-0.3 to +3.3	V	refer to $V_{SS}$ level
Supply voltage (digital)	$V_{DIG}$	-0.3 to +1.8	V	
Supply voltage (interface)	$V_{IF}$	-0.3 to +3.3	V	
Input voltage (digital)	$V_I$	-0.3 to +3.3	V	
Output voltage (digital)	$V_O$	-0.3 to +3.3	V	
Guaranteed operating temperature	$T_{OPR}$	-20 to +75	°C	
Guaranteed storage temperature	$T_{STG}$	-30 to +80	°C	
Guaranteed performance temperature	$T_{SPEC}$	-20 to +60	°C	

## Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	$V_{ANA}^{*1}$	$2.8 \pm 0.1$	V	refer to $V_{SS}$ level
Supply voltage (digital)	$V_{DIG}^{*2}$	$1.05 \pm 0.1$	V	
Supply voltage (interface)	$V_{IF}^{*3}$	$1.8 \pm 0.1$	V	

\*1  $V_{ANA}$ :  $V_{DDSUB}$ ,  $V_{DDHAN}$ ,  $V_{DDHCM1}$  to 2,  $V_{DDHSN1}$  to 4 (2.8 V power supply)

\*2  $V_{DIG}$ :  $V_{DDLSC1}$  to 4,  $V_{DDL CN1}$  to 2,  $V_{DDLPL1}$  to 2,  $V_{DDLIF}$  (1.05 V power supply)

\*3  $V_{IF}$ :  $V_{DDMIO1}$  to 2,  $V_{DDMIF}$  (1.8 V power supply)

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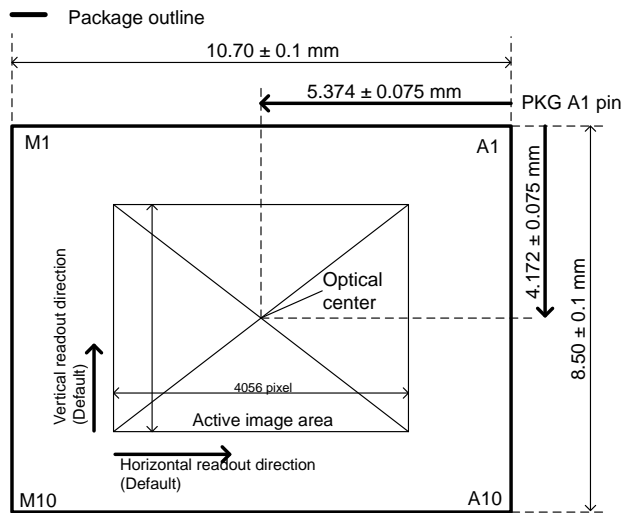
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1. Optical Center

(Top View)



Note) The optical center is the center of the active image area 4056 (H) × 3040 (V) pixel.  
Please refer to “Figure 12 Physical alignment of the imaging pixel array (Top View)” for active image area.

Figure 2 Optical Center

2. Pin Configuration

(Bottom View)

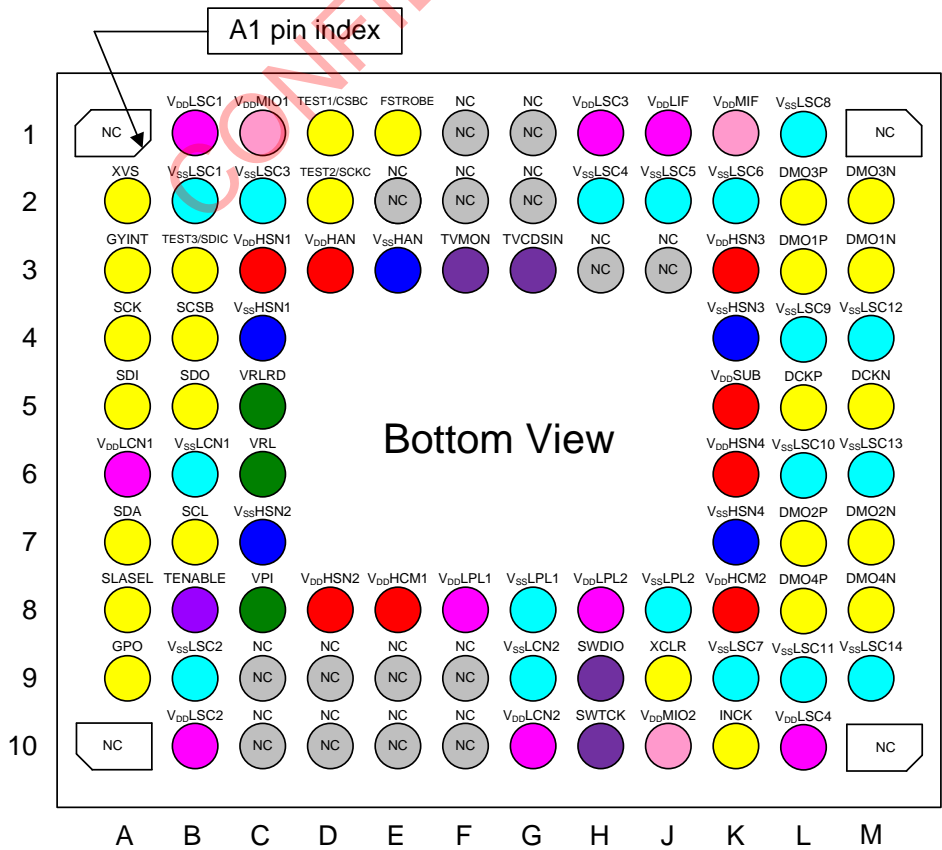


Figure 3 Pin Configuration



### 3. Pin Description

**Table 1 Pin Description**

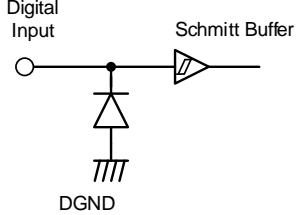
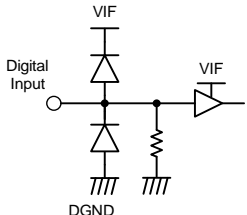
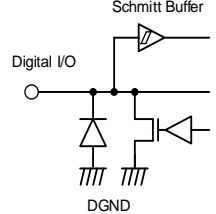
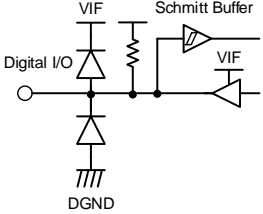
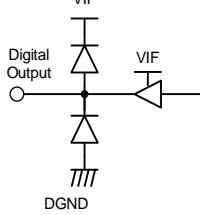
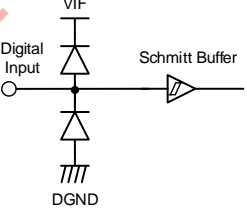
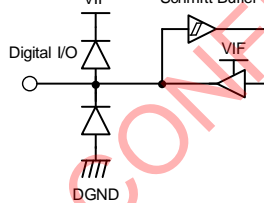
Pin No.	Symbol	I/O	A/D	Pin description	Remarks
A2	XVS	I/O	D	Digital I/O (Vertical sync signal)	Used as a vertical synchronizing signal of dual sensor application
A3	GYINT	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the Gyro interrupt)
A4	SCK	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro control clock)
A5	SDI	I/O	D	Digital I/O	Digital GND (When using OIS combined system, this pin has the function of the Gyro data input)
A6	V <sub>DD</sub> LCN1	Power	D	V <sub>DIG</sub> power supply	
A7	SDA	I/O	D	Digital I/O	I <sup>2</sup> C communication data input/output
A8	SLASEL	I	D	Digital input	I <sup>2</sup> C slave address select (Pull-down)
A9	GPO	O	D	Digital output	
B1	V <sub>DD</sub> LSC1	Power	D	V <sub>DIG</sub> power supply	
B2	V <sub>SS</sub> LSC1	GND	D	V <sub>DIG</sub> GND	
B3	TEST3/SDIC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
B4	SCSB	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro chip select)
B5	SDO	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro data output)
B6	V <sub>SS</sub> LCN1	GND	D	V <sub>DIG</sub> GND	
B7	SCL	I/O	D	Digital I/O	I <sup>2</sup> C communication clock input
B8	TENABLE	I	D	Digital input	NC (Pull-down)
B9	V <sub>SS</sub> LSC2	GND	D	V <sub>DIG</sub> GND	
B10	V <sub>DD</sub> LSC2	Power	D	V <sub>DIG</sub> power supply	
C1	V <sub>DD</sub> MIO1	Power	D	V <sub>IF</sub> power supply	
C2	V <sub>SS</sub> LSC3	GND	D	V <sub>DIG</sub> GND	
C3	V <sub>DD</sub> HSN1	Power	A	V <sub>ANA</sub> power supply	
C4	V <sub>SS</sub> HSN1	GND	A	V <sub>ANA</sub> GND	
C5	VRLRD	Minus	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)
C6	VRL	Minus	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)
C7	V <sub>SS</sub> HSN2	GND	A	V <sub>ANA</sub> GND	
C8	VPI	Power	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)

Pin No.	Symbol	I/O	A/D	Pin description	Remarks
D1	TEST1/CSBC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
D2	TEST2/SCKC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
D3	V <sub>DD</sub> HAN	Power	A	V <sub>ANA</sub> power supply	
D8	V <sub>DD</sub> HSN2	Power	A	V <sub>ANA</sub> power supply	
E1	FSTROBE	O	D	Digital output	Flash strobe
E3	V <sub>SS</sub> HAN	GND	A	V <sub>ANA</sub> GND	
E8	V <sub>DD</sub> HCM1	Power	A	V <sub>ANA</sub> power supply	
F3	TVMON	O	A	Analog output	NC
F8	V <sub>DD</sub> LPL1	Power	D	V <sub>DIG</sub> power supply	
G3	TVCD SIN	I	A	Analog input	NC
G8	V <sub>SS</sub> LPL1	GND	D	V <sub>DIG</sub> GND	
G9	V <sub>SS</sub> LCN2	GND	D	V <sub>DIG</sub> GND	
G10	V <sub>DD</sub> LCN2	Power	D	V <sub>DIG</sub> power supply	
H1	V <sub>DD</sub> LSC3	Power	D	V <sub>DIG</sub> power supply	
H2	V <sub>SS</sub> LSC4	GND	D	V <sub>DIG</sub> GND	
H8	V <sub>DD</sub> LPL2	Power	D	V <sub>DIG</sub> power supply	
H9	SWDIO	I/O	D	Digital I/O	NC (Pull-up)
H10	SWTCK	I	D	Digital input	NC (Pull-down)
J1	V <sub>DD</sub> LIF	Power	D	V <sub>DIG</sub> power supply	
J2	V <sub>SS</sub> LSC5	GND	D	V <sub>DIG</sub> GND	
J8	V <sub>SS</sub> LPL2	GND	D	V <sub>DIG</sub> GND	
J9	XCLR	I	D	Digital input	Chip clear (Pull-down)
J10	V <sub>DD</sub> MIO2	Power	D	V <sub>IF</sub> power supply	
K1	V <sub>DD</sub> MIF	Power	D	V <sub>IF</sub> power supply	
K2	V <sub>SS</sub> LSC6	GND	D	V <sub>DIG</sub> GND	
K3	V <sub>DD</sub> HSN3	Power	A	V <sub>ANA</sub> power supply	
K4	V <sub>SS</sub> HSN3	GND	A	V <sub>ANA</sub> GND	
K5	V <sub>DD</sub> SUB	Power	A	V <sub>ANA</sub> power supply	
K6	V <sub>DD</sub> HSN4	Power	A	V <sub>ANA</sub> power supply	
K7	V <sub>SS</sub> HSN4	GND	A	V <sub>ANA</sub> GND	
K8	V <sub>DD</sub> HCM2	Power	A	V <sub>ANA</sub> power supply	
K9	V <sub>SS</sub> LSC7	GND	D	V <sub>DIG</sub> GND	
K10	INCK	I	D	Digital input	
L1	V <sub>SS</sub> LSC8	GND	D	V <sub>DIG</sub> GND	
L2	DMO3P	O	D	Digital output	MIPI output (DATA+)
L3	DMO1P	O	D	Digital output	MIPI output (DATA+)
L4	V <sub>SS</sub> LSC9	GND	D	V <sub>DIG</sub> GND	
L5	DCKP	O	D	Digital output	MIPI output (CLK+)
L6	V <sub>SS</sub> LSC10	GND	D	V <sub>DIG</sub> GND	
L7	DMO2P	O	D	Digital output	MIPI output (DATA+)
L8	DMO4P	O	D	Digital output	MIPI output (DATA+)
L9	V <sub>SS</sub> LSC11	GND	D	V <sub>DIG</sub> GND	

Pin No.	Symbol	I/O	A/D	Pin description	Remarks
L10	V <sub>DD</sub> LSC4	Power	D	V <sub>DIG</sub> power supply	
M2	DMO3N	O	D	Digital output	MIPI output (DATA-)
M3	DMO1N	O	D	Digital output	MIPI output (DATA-)
M4	V <sub>SS</sub> LSC12	GND	D	V <sub>DIG</sub> GND	
M5	DCKN	O	D	Digital output	MIPI output (CLK-)
M6	V <sub>SS</sub> LSC13	GND	D	V <sub>DIG</sub> GND	
M7	DMO2N	O	D	Digital output	MIPI output (DATA-)
M8	DMO4N	O	D	Digital output	MIPI output (DATA-)
M9	V <sub>SS</sub> LSC14	GND	D	V <sub>DIG</sub> GND	

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#### 4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR, SLASEL	
SCL, SDA		XVS	
GPO, FSTROBE, SDO, SCK, SCSB		GYINT	
SDI			

$V_{IF}$ : 1.8 V power supply

DGND:  $V_{DIG}$  GND

$V_{DD}LSC1$ ,  $V_{DD}LSC2$ ,  $V_{DD}LSC3$  and  $V_{DD}LSC4$  are internally connected.

$V_{SSLSC1}$  to 14 are internally connected.

$V_{DD}MIO1$  and  $V_{DD}MIO2$  are internally connected.

$V_{DD}HCM1$  and  $V_{DD}HCM2$  are internally connected.

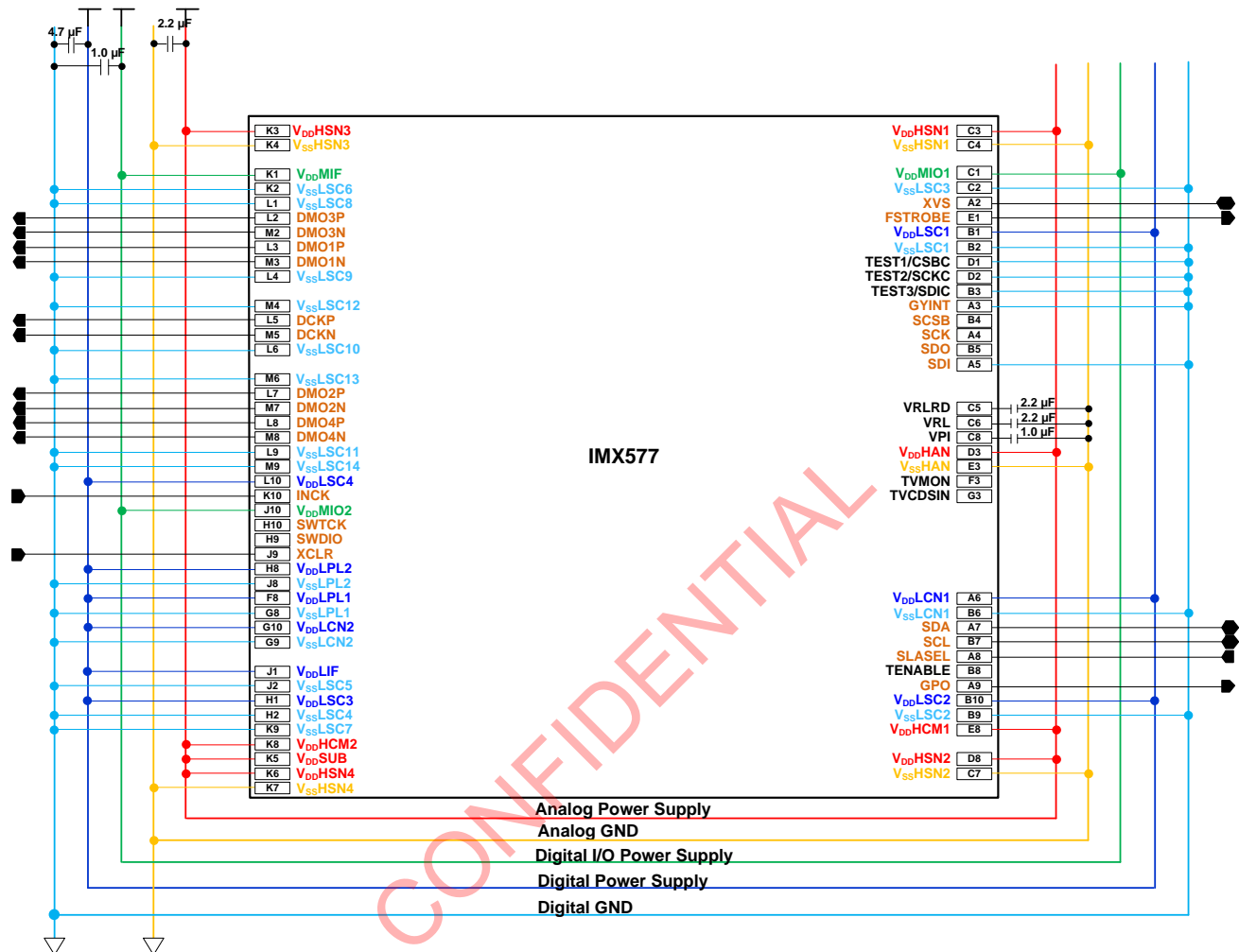
$V_{DD}HSN1$ ,  $V_{DD}HSN2$ ,  $V_{DD}HSN3$  and  $V_{DD}HSN4$  are internally connected.

$V_{SSLSC1}$ ,  $V_{SSLSC2}$ ,  $V_{SSLSC3}$  and  $V_{SSLSC4}$  are internally connected.

**Figure 4 Input / Output Equivalent Circuit**

## 5. Peripheral Circuit Diagram

### 5-1 Standard peripheral circuit diagram



- Note) The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with SSS's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.
- Note) If you need combined with the OIS, There is a need to change the connection of the next pin. TEST1/CSBC, TEST2/SCKC, TEST3/SDIC, GYINT, SCSB, SCK, SDO, SDI  
See software reference manual for details.

Figure 5 Peripheral Circuit Diagram (Recommended schematics)

## 5-2 Connecting for OIS compatible system

IMX577-AACK-C can connect with OIS controller using SPI bypass function. When the bypass mode set to enable, OIS controller can get the gyro data through IMX577-AACK-C. Each terminal also requires 1.8 V I/O voltage level when connect with OIS controller and gyro LSI. See software reference manual for details.

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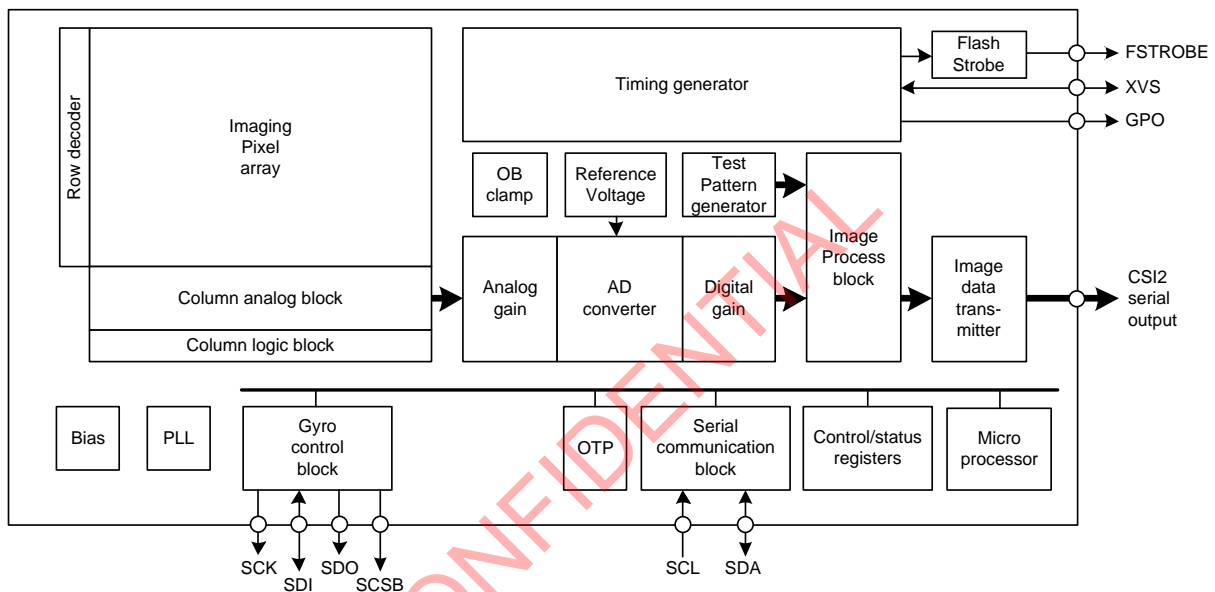
## 6. Functional Description

## 6-1 System Outline

IMX577-AACK-C is a CMOS active pixel type image sensor which adopts the Exmor RS technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. When Gyro function is enabled, Gyro control block in IMX577-AACK-C is processed based on the input data from Gyro IC.

Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.

A onetime programmable memory is embedded in the chip for storing the user data. It has 7 K-bit for users, 16 K-bit as a whole.



**Figure 6 Overview of functional block diagram**

## 6-2 Control register setting by the serial communication

The IMX577-AACK-C can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Software reference manual for more details of each function beyond the following description.

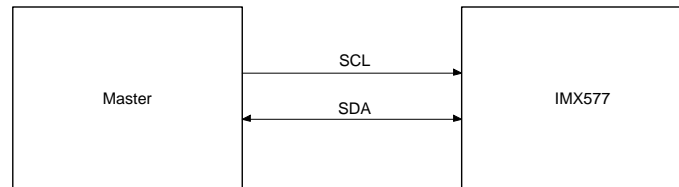


Figure 7 2-wire serial communication

### 6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I<sup>2</sup>C fast-mode compatible interface, and the data transfer protocol is I<sup>2</sup>C standard.

This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX577-AACK-C.

Table 2 Description of 2-wire Serial Communication Pins

Pin name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX577-AACK-C are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 3 Specification of register address map for 2-wire serial communication

I <sup>2</sup> C register	Address range	Description
	0000h to 0FFFh	Configuration register Read Only and Read/Write Dynamic register
	1000h to 1FFFh	Reserved
	2000h to 2FFFh	Reserved
	3000h to FFFFh	Manufacture specific register



6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

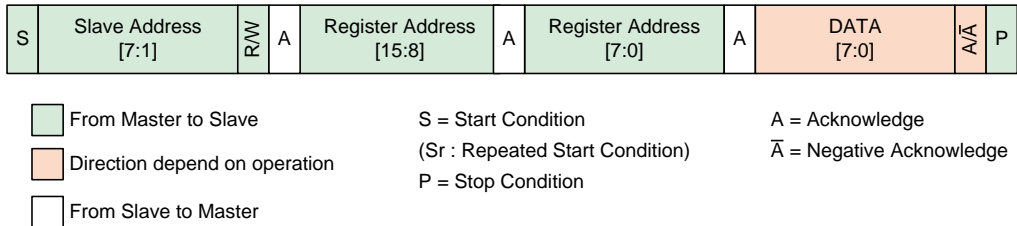
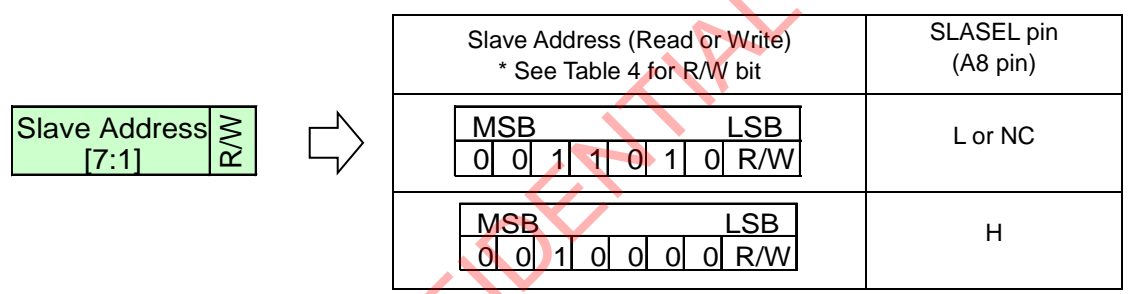


Figure 8 2-wire serial communication protocol

IMX577-AACK-C has a default slave address shown as below.  
The slave address is selectable by pin connection of SLASEL pin (A8 pin).  
When called by the selected slave address, serial communication interface is activated.  
Duplication of the address on the same bus must be prevented.  
\*For other slave address options, refer to Software reference manual.



R/W shows the direction of communication.

Figure 9 Slave address

Table 4 R/W bit

R/W bit	Direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

### 6-3 Clock generation and PLL

IMX577-AACK-C equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Software reference manual for more details of each function.

### 6-3-1 Clock System Diagram

IMX577-AACK-C is equipped with two PLL, One outputs IVTCK for image processing, the other is IOPCK for MIPI output.

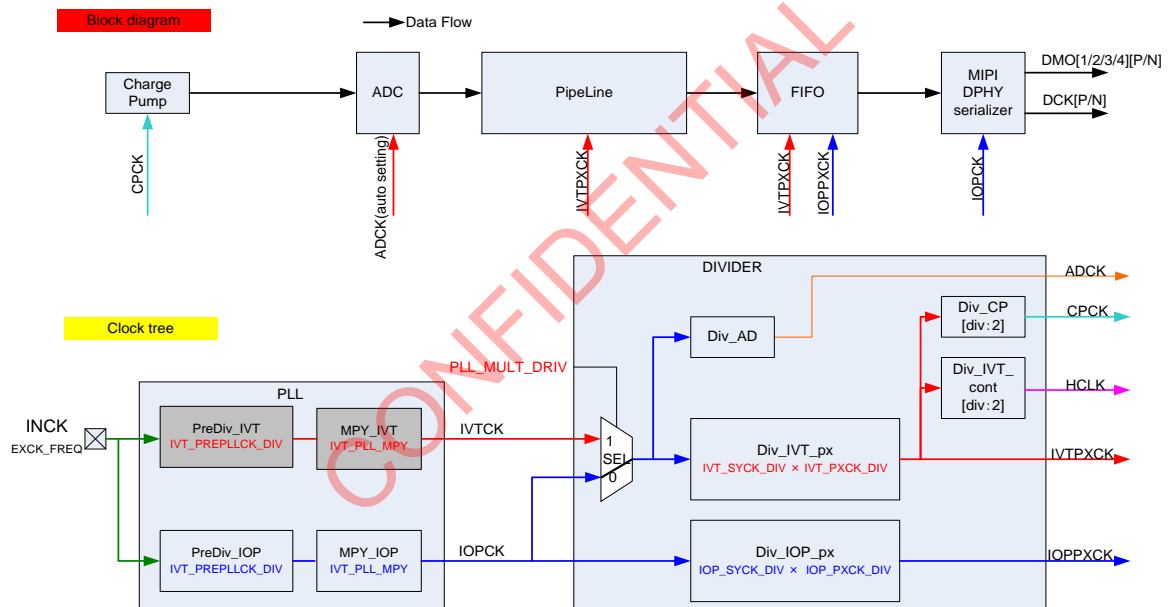
Based on the clock that is input in the range of 6 to 27 MHz, output of 1800 to 2100 MHz can be of the PLL for IVTCK, PLL of IOPCK for is capable of outputting 1200 to 2100 MHz.

It is possible to divide the range of 1/1 to 1/4 of the PLL IVTCK, and to multiply in the range of 150 to 350.

It is possible to divide the range of 1/1 to 1/4 of the PLL IOPCK, and to multiply in the range of 100 to 350.

Typically, IMX577-AACK-C can be driven from the dual PLL mode to operate the both of PLLs, but it also supports single PLL mode to move only one side of the PLL.

In PLL single mode, IOP\_PREPLLCK\_DIV and IOP\_PLL\_MPY are ignored.



**Figure 10 Clock System Diagram (PLL single mode)**

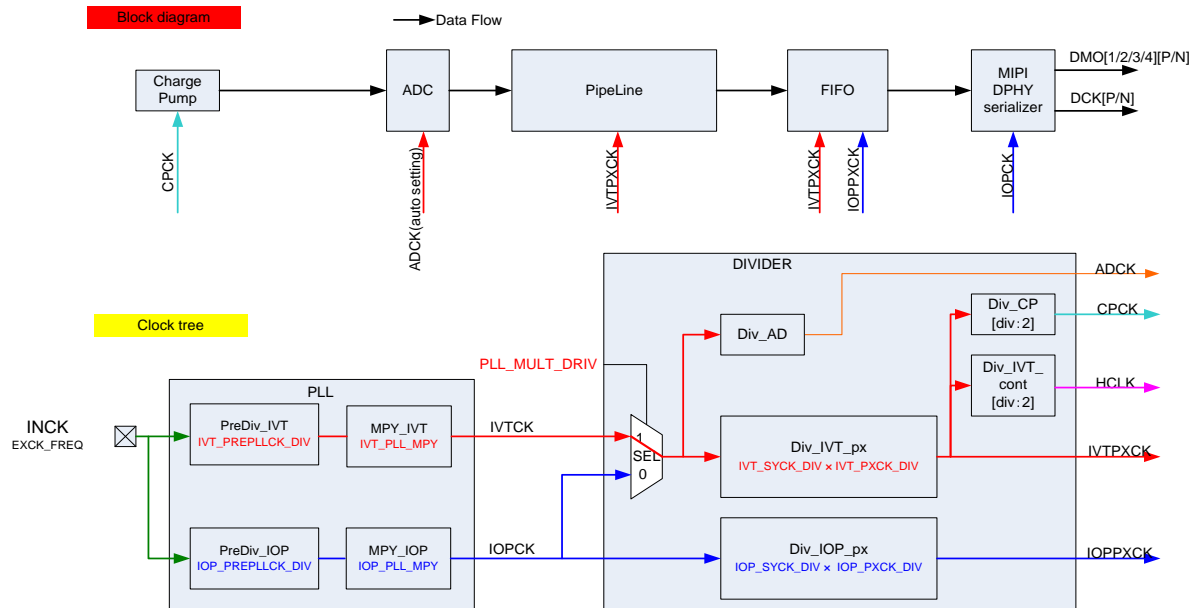


Figure 11 Clock System Diagram (PLL dual mode)

## 6-4 Description of operation clocks

The following are general descriptions for each clock. See “Clock generation and PLL” of Software reference manual for more detail.

### 6-4-1 INCK

INCK is an external input clock (6 to 27 MHz). See “AC characteristics” for electrical requirements to INCK.

### 6-4-2 ITPCK, IOPCK (PLL output)

These clocks are the root of all the operation clocks in IMX577-AACK-C and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2, 1/4 or 1/8 frequency since the interface is operated in double data rate format.

### 6-4-3 ITPXCK Clock

The clock for internal image processing is used as the base of integration time, frame rate, and etc.

### 6-4-4 IOPPXCK Clock

The clock for internal image processing is designating the pixel rate and etc.

## 6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX577-AACK-C outputs the image data.

See Software reference manual for more details of each function.

### 6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with A1 pin located at the upper right corner.

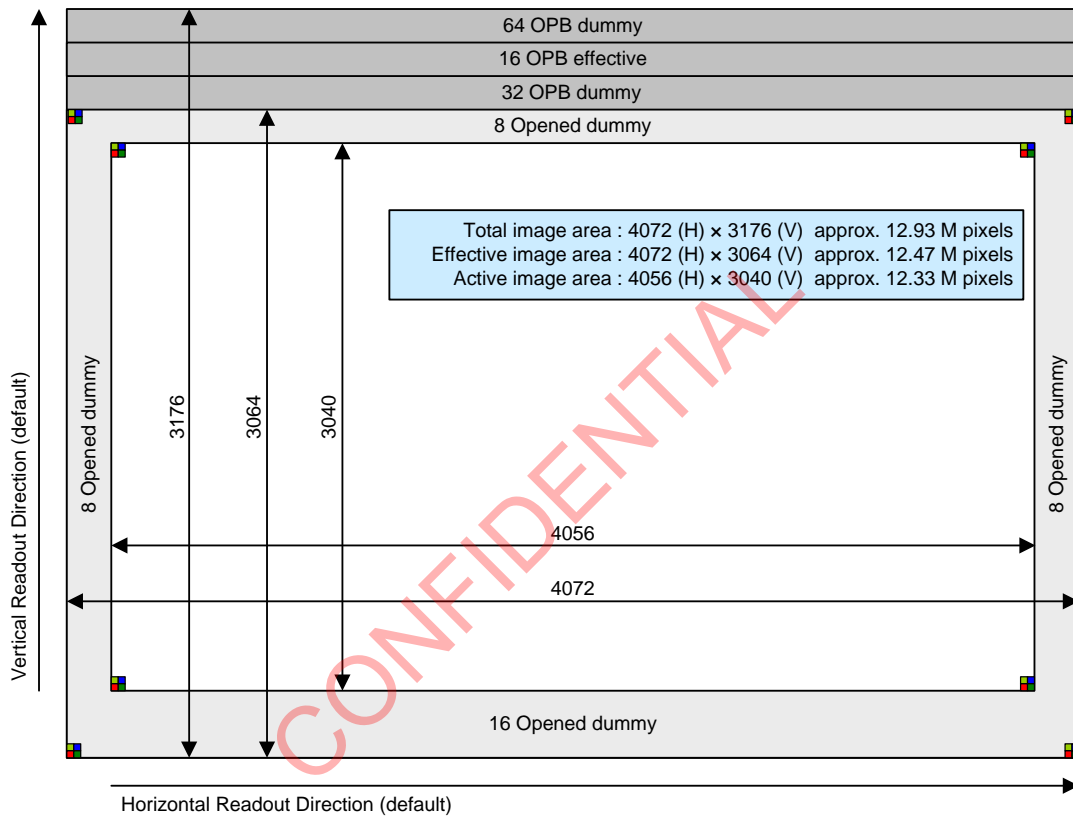


Figure 12 Physical alignment of the imaging pixel array (Top View)

### 6-5-2 Color coding and order of reading image data

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively.

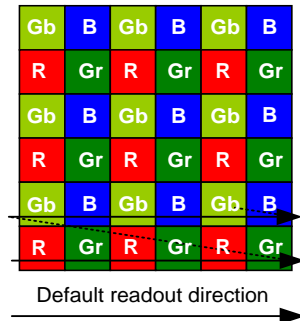


Figure 13 Color coding alignment

### 6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

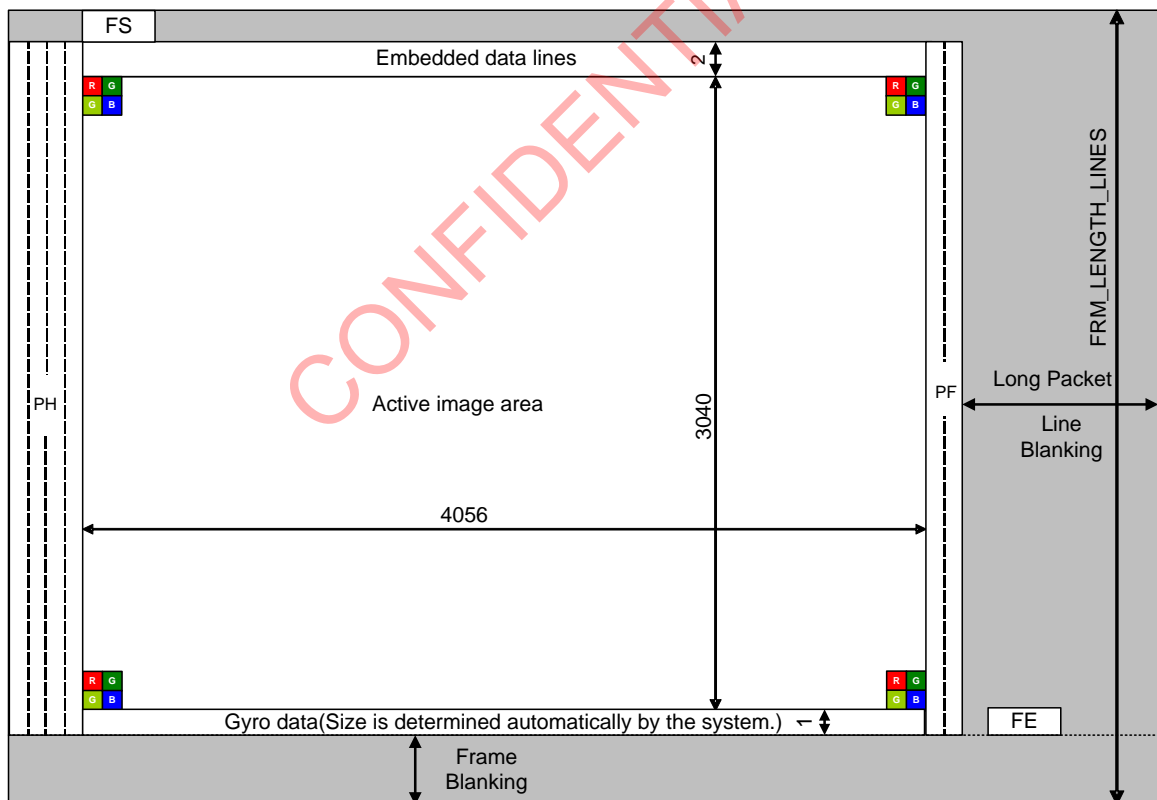


Figure 14 Full pixel output mode data structure

### 6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map. An unfixed value is output when not outputting embedded data.

See Software reference manual for contents and output sequence of Embedded Data Lines.

### 6-6-2 Image size of mode

IMX577-AACK-C can capture and output full size, cropped/scaled image in combination with the normal mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

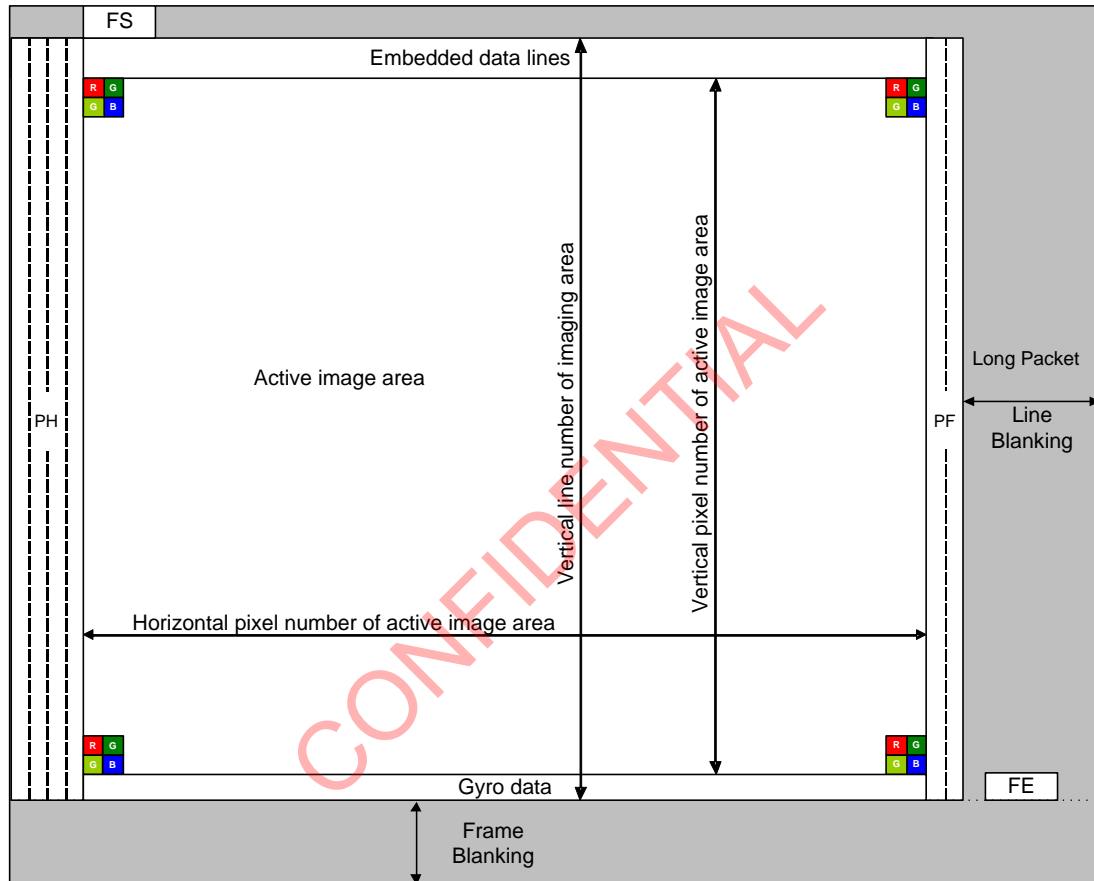


Figure 15 Image size parameter definition

Table 5 Typical image output of main capture mode

		Modes					
		Normal Operation Full resolution 10 bit / 12 bit		Normal Operation 2 Binning (V:1/2, H:1/2) 10 bit		DOL-HDR Full resolution 10 bit / 12 bit	
Number of vertical lines in imaging area		3044		1524		*1	
Number of horizontal pixels in active area		4056		2028			
Number of lines and start position		Start position	Number of lines	Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	-	1	-	*1	
	Embedded data lines	1	2	1	2		
	Number of vertical pixels in active area	3	3040	3	1520		
	Gyro Data	3043	1	1523	1		
	Frame end	3043	-	1523	-		

\*1 See DOL-HDR manual for details.

### 6-6-3 Description about operation mode

IMX577-AACK-C has following mode that Full resolution, Full resolution (DOL-HDR), 2 Binning (V:1/2, H:1/2).

See "Description of mode operation" of Software reference manual for details.

#### 6-6-4 Image area control capabilities

As control function for image's viewing area and /or image size, IMX577-AACK-C has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the register is shown below.

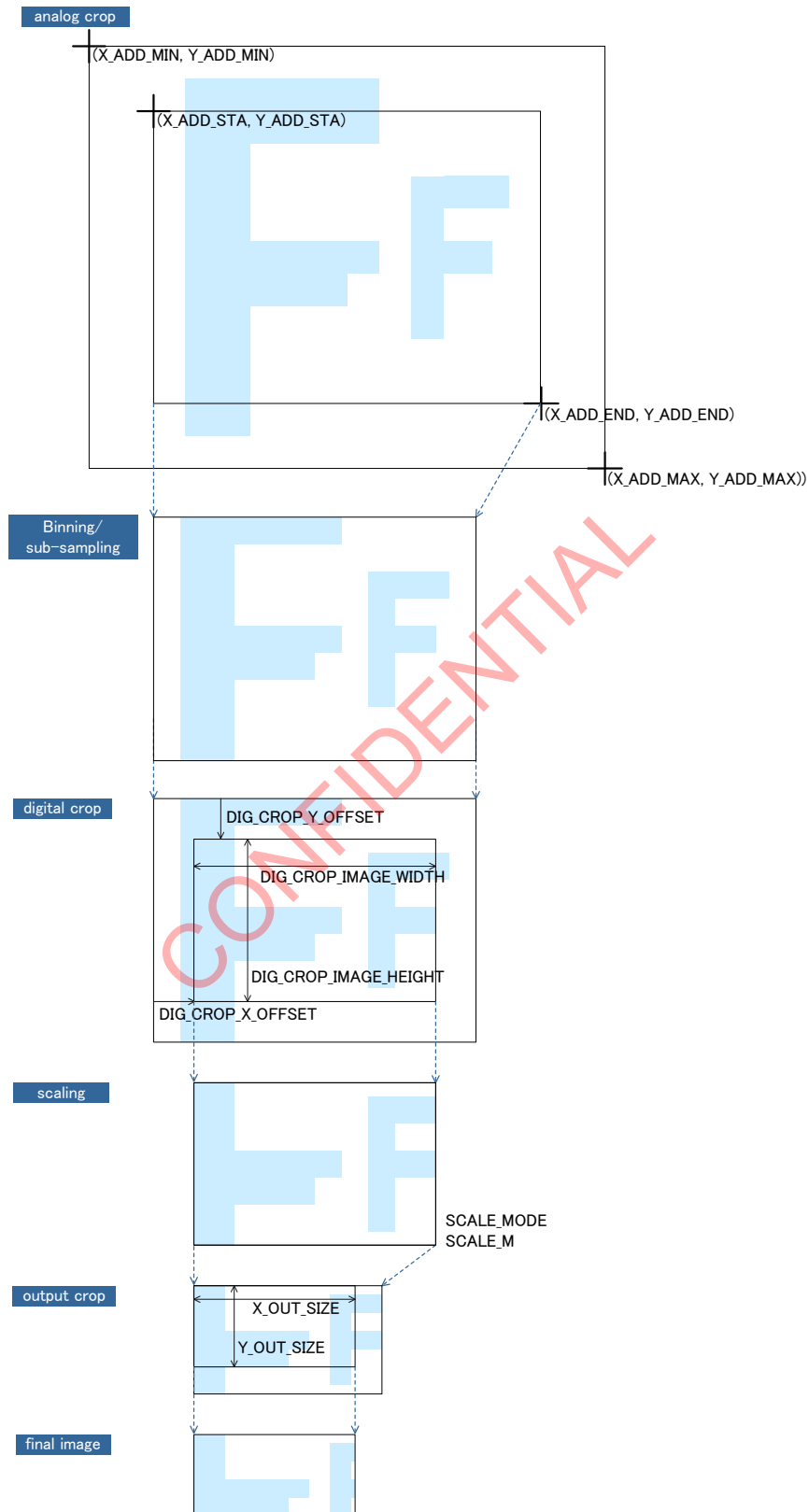


Figure 16 Image area control capabilities



6-6-5 Readout Scan Direction

Default readout position of IMX577-AACK-C starts from the lower left when pin A1 pin is placed at the upper right corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when A1 pin is placed at the upper right corner.

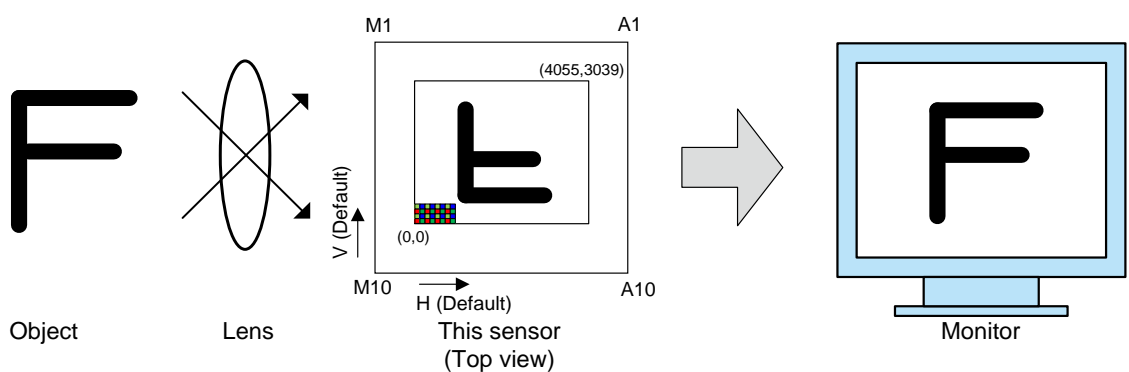


Figure 17 Readout Scan Direction

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, the color of first readout pixel (R/Gr/Gb/B) also changes with it. See Software reference manual for details.

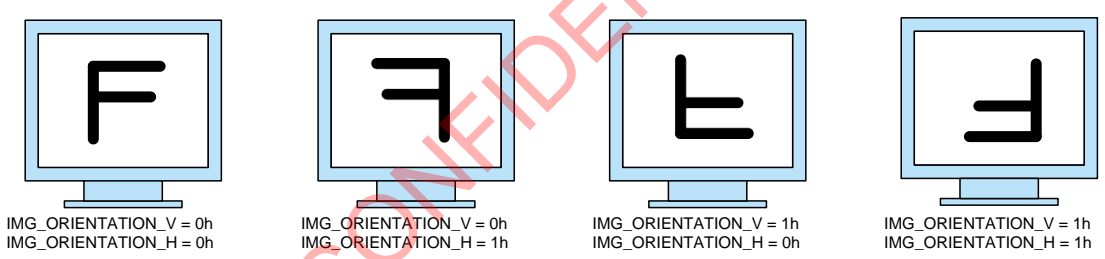


Figure 18 Read out image for each combination of flip and mirror

## 6-7 Gain setting

IMX577-AACK-C can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

**Table 6 Range of Gains**

	Max.	Note
Analog Gain	27 dB	
Digital Gain	24 dB	

## 6-8 Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Software reference manual for more details of each function.

### 6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There is one area for SSS's factory area.

The dynamic defect correction eliminates any critical defects detected on RGB pixel array by estimating from surrounding adjacent pixels value.

## 6-9 Miscellaneous functions

IMX577-AACK-C has the following additional functions to be used for various final products' features.  
See Application Notes for more details of each function.

### 6-9-1 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I<sup>2</sup>C or EBD data. See "Thermal meter" of Software reference manual for details.

### 6-9-2 Test pattern output and type of test pattern

IMX577-AACK-C can output the following test pattern by build-in pattern generator.  
Test patterns of Solid Color, 100 % Color Bar, Fade to Gray Color Bar, PN9 are available.  
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.  
See "Test pattern output (types of test patterns)" of Software reference manual for details.

### 6-9-3 Long Exposure Setting

IMX577-AACK-C can achieve a very long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting. See "Long exposure" of Software reference manual for details.

### 6-9-4 OTP (One Time Programmable Read Only Memory)

Total of 7 K bit of OTP is available for users. The area available for the user totals 14 pages. Among these pages, total 896 Byte (address: 0 to 895) can be used at the user's discretion.  
It is also possible to configure most of 14 pages to be usable at the user's discretion, if LSC data, ALS data and model ID function are not necessary to storage in OTP. See OTP manual for details.

### 6-9-5 Dual sensor synchronization operation (Multi camera compatible)

IMX577-AACK-C supports synchronized shooting operation of two or more image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method. See "Dual Camera" of Software reference manual for details.

### 6-9-6 Flash light control sequence

IMX577-AACK-C can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE). See "Flash light control sequence" of Software reference manual for details.

### 6-9-7 Monitor terminal settings

IMX577-AACK-C can output 4 internal signals (H Sync/V Sync/Flash strobe/OIS pulse) via monitor terminals. The monitor terminals mean the following three terminals, such as FSTROBE (E1 pin), GPO (A9 pin) and XVS (A2 pin). See "Monitor terminal settings" of Software reference manual for details.

### 6-9-8 Pulse for OIS driver

IMX577-AACK-C can output the pulse for OIS driver. See Software reference manual for details.

### 6-9-9 Low power streaming mode

IMX577-AACK-C supports the Low Power Streaming Mode. This function can reduce the power consumption at low frame rate. See Software reference manual for more detail.

### 6-9-10 Horizontal Low Power analog Cropping

IMX577-AACK-C supports to terminate column ADCs of unnecessary area regarding Horizontal crop setting. See Software reference manual for more detail.

### 6-9-11 Window scanning mode

IMX577-AACK-C has a mode which is able to change analog cropping area dynamically without corrupted frame. See Software reference manual for more detail.

### 6-9-12 Digital Overlap High Dynamic Range (DOL-HDR)

This sensor outputs to overlap several images that have different exposure time. In DOL 2 frame, the 1st frame and the 2nd frame are output as HDR set (Frame set) among 2 frames period of normal operation. In DOL 3 frame, the 1st frame, the 2nd frame and the 3rd frame are output as HDR set (Frame set) among 4 frames period of normal operation. See DOL-HDR manual for details.

\*DOL-HDR function is not available on slave mode in dual or multi sensor synchronization operation.

### 6-9-13 Ambient Light Sensor (ALS)

This function is to measure the illuminance. Measurement results could be read via I<sup>2</sup>C. See ALS manual for details.

## 6-10 Image signal interface

### 6-10-1 MIPI transmitter

IMX577-AACK-C outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details.

Because signal is transmitted by differential pair, impedance (generally 100  $\Omega$ ) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

7. How to operate

7-1 Power on Reset

IMX577-AACK-C does not have the built in “Power On Reset” function.  
The XCLR pin is set to “Low” and the power supplies are brought up. Then the XCLR pin should be set to “High” after INCK supplied.

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/μs) is specified for each power supply to avoid oscillation during power on.

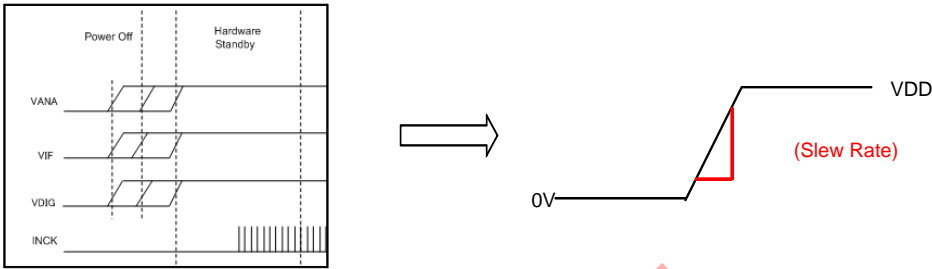


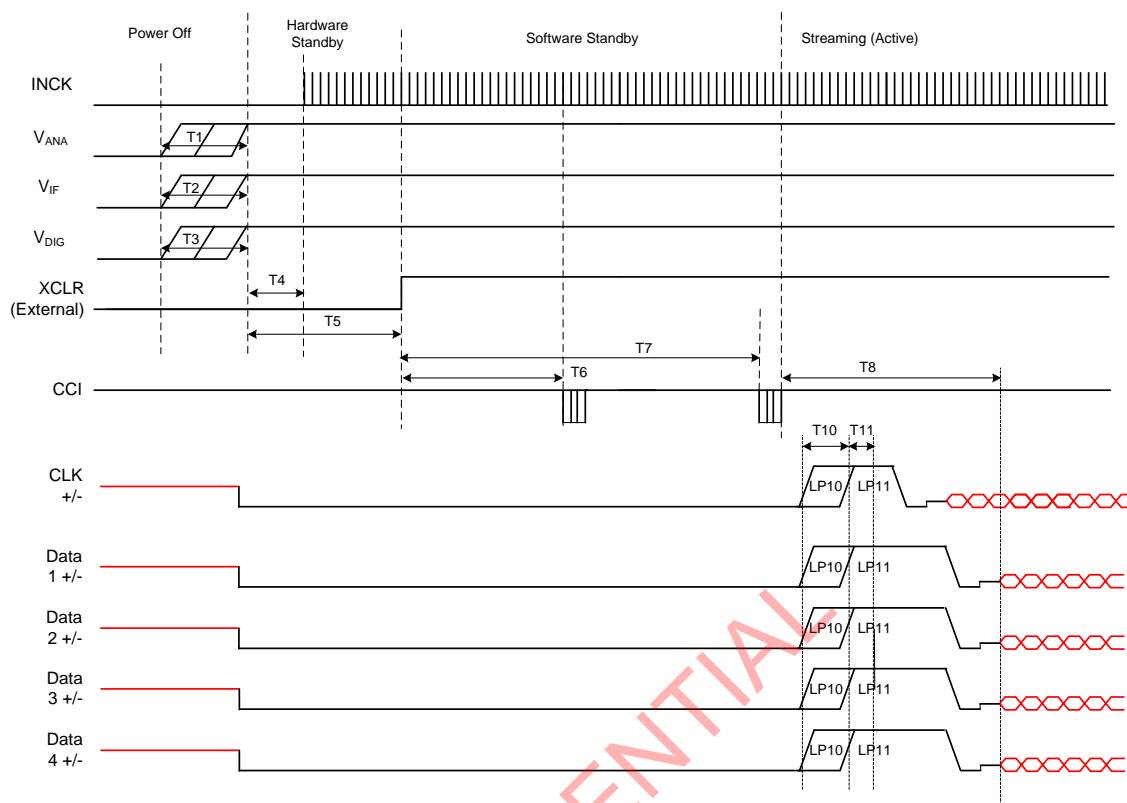
Figure 19 Power on slew rate

Table 7 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min.	Max.	Unit	
V <sub>ANA</sub> , V <sub>IF</sub> , V <sub>DIG</sub>		50	mV/μs	

### 7-2-2 Startup sequence with 2-wire serial communication (external reset)

Follow the power supply start up sequence as below.



**Figure 20 Startup sequence with 2-wire serial communication (external reset)**

\* Presence of INCK during Power Off is acceptable despite of above chart.

**Table 8 Startup sequence timing constraints (2-wire serial communication mode with external reset)**

Item	Label	Min.	Max.	Unit	Comment
$V_{ANA}$ rising – $V_{ANA}$ ON	T1	$V_{ANA}$ and $V_{IF}$ and $V_{DIG}$ may rise in any order.		$\mu s$	Slew rate of $V_{ANA}$ , $V_{IF}$ and $V_{DIG}$ (0 % - 100 %): Max. 50 mV/ $\mu s$
$V_{IF}$ rising – $V_{IF}$ ON	T2			$\mu s$	
$V_{DIG}$ rising – $V_{DIG}$ ON	T3			$\mu s$	
$V_{ANA}$ and $V_{IF}$ and $V_{DIG}$ rising - INCK start	T4	0		$\mu s$	Presence of INCK during Power off is acceptable
$V_{ANA}$ and $V_{IF}$ and $V_{DIG}$ rising - XCLR rising	T5	0		ms	After T1, T2 and T3
INCK start and XCLR rising till CCI Read version ID register wait time	T6	0.6		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	8		ms	
Start of first streaming from Sending Streaming Command.	T8		4.0 ms + The delay of the coarse integration time value		
D-PHY power up	T10	1	1.1	ms	
D-PHY init.	T11	100	110	$\mu s$	

Note) XCLR needs to be Low until all power supplies complete power-on

### 7-3 Power down sequence

#### 7-3-1 Power down sequence with 2-wire serial communication (external reset)

Follow the power down sequence below.

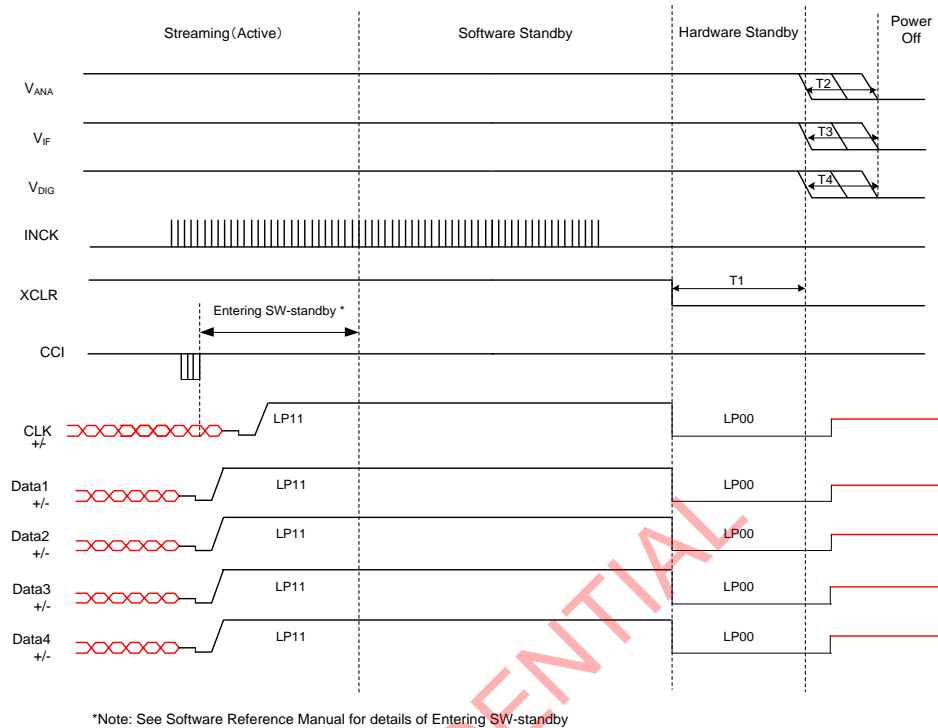


Figure 21 Power down sequence with 2-wire serial communication (external reset)

Table 9 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge - $V_{ANA}$ ( $V_{IF}$ or $V_{DIG}$ ) fall	T1	0		$\mu s$	Presence of INCK during Power Off is acceptable.
Sequence free of $V_{ANA}$ falling and $V_{IF}$ falling and $V_{DIG}$ falling	T2,T3,T4	$V_{ANA}$ and $V_{IF}$ and $V_{DIG}$ may fall in any order.		$\mu s$	

### 7-4 Register Map

See Register Map.



## 8. Electrical Characteristics

The Electrical Characteristics of the IMX577-AACK-C is shown below

### 8-1 DC characteristics

Table 10 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub> SUB, V <sub>DD</sub> HCM1 to 2, V <sub>DD</sub> HSN1 to 4, V <sub>DD</sub> HAN	V <sub>ANA</sub>		2.7	2.8	2.9	V
	V <sub>DD</sub> LCN1 to 2, V <sub>DD</sub> LSC1 to 4, V <sub>DD</sub> LIF, V <sub>DD</sub> LPL1 to 2	V <sub>DIG</sub>		0.95	1.05	1.15	V
	V <sub>DD</sub> MIO1 to 2, V <sub>DD</sub> MIF	V <sub>IF</sub>		1.7	1.8	1.9	V
Digital input voltage	SDA, SCL	V <sub>IH</sub>		0.7 V <sub>IF</sub>		2.9	V
		V <sub>IL</sub>		- 0.3		0.3 V <sub>IF</sub>	V
Digital input voltage	XCLR, INCK, GYINT, SDI,SLASEL	V <sub>IH</sub>		0.65 V <sub>IF</sub>		V <sub>IF</sub> + 0.3	V
		V <sub>IL</sub>		- 0.3		0.35 V <sub>IF</sub>	V
Digital output voltage	SDA	V <sub>OH</sub>		V <sub>IF</sub> - 0.4			V
		V <sub>OL</sub>				0.4	V
Digital output voltage	GPO,SDO, SCSB, FSTROBE	V <sub>OH</sub>		V <sub>IF</sub> - 0.4			V
		V <sub>OL</sub>				0.4	V

## 8-2 AC Characteristics

### 8-2-1 Master Clock Waveform Diagram

#### 8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

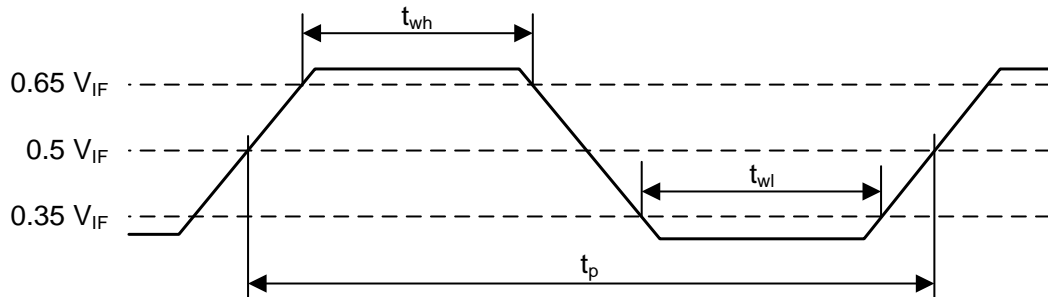


Figure 22 Master Clock Square Waveform Input Diagram

Table 11 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	$f_{\text{sck}}$	6		27	MHz
INCK clock period	$t_p$	37.0		166.7	ns
INCK low level width	$t_{wl}$	$0.4 t_p$		$0.6 t_p$	ns
INCK high level width	$t_{wh}$	$0.4 t_p$		$0.6 t_p$	ns
INCK jitter	$T_{\text{jitter}}$			600	ps

#### 8-2-1-2 INCK Sine Waveform Input Specifications

IMX577-AACK-C does not support the "AC coupled connection".

Therefore, there is no description of AC characteristics

### 8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 12 PLL block characteristics (VT system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	1800		2100.0	MHz	
Output frequency range	1800		2100.0	MHz	
Settling time			1000	$\mu\text{s}$	

**Table 13 PLL block characteristics (OP system)**

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	1200		2100.0	MHz	
Output frequency range	1200		2100.0	MHz	
Settling time			1000	μs	

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### 8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

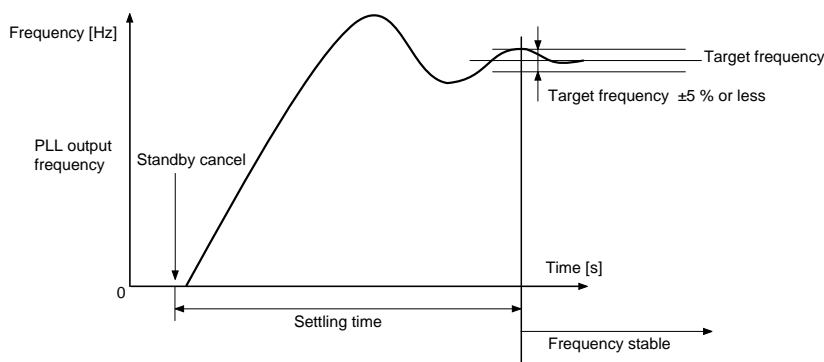


Figure 23 Definition of settling time

### 8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

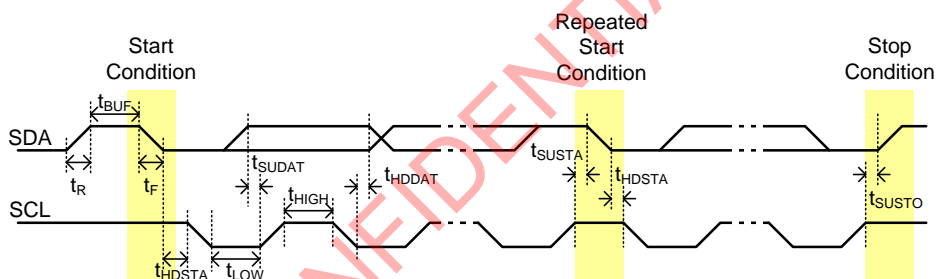


Figure 24 2-wire serial communication block specification

Table 14 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
Low level input voltage	$V_{IL}$		-0.5	$0.3 V_{IF}$	V
High level input voltage	$V_{IH}$		$0.7 V_{IF}$	2.9	V
Low level output voltage	$V_{OL1}$	$V_{IF} > 2$ V, Sink 3 mA	0	0.4	V
	$V_{OL2}$	$V_{IF} < 2$ V, Sink 3 mA	0	$0.2 V_{IF}$	V
Output fall time	$t_{of}$	Load 10 pF – 400 pF, $0.7 V_{IF} \rightarrow 0.3 V_{IF}$		250 (120)	ns
Input current	$I_I$	$0.1 V_{IF} \rightarrow 0.9 V_{IF}$	-10	10	$\mu$ A
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	$C_I$			10	pF

Table 15 2-wire serial communication block AC specification

Parameter	Symbol	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
SCL clock frequency	$f_{SCL}$	0	400 (1000)	kHz
Rise time (SDA and SCL)	$t_R$	—	300 (120)	ns
Fall time (SDA and SCL)	$t_F$	—	300 (120)	ns
Hold time (start condition)	$t_{HDSTA}$	0.6 (0.26)	—	$\mu s$
Setup time (rep.-start condition)	$t_{SUSTA}$	0.6 (0.26)	—	$\mu s$
Setup time (stop condition)	$t_{SUSTO}$	0.6 (0.26)	—	$\mu s$
Data setup time	$t_{SUDAT}$	100 (50)	—	ns
Data hold time	$t_{HDDAT}$	0	—	$\mu s$
Bus free time between Stop and Start condition	$t_{BUF}$	1.3 (0.5)	—	$\mu s$
Low period of the SCL clock	$t_{LOW}$	1.3 (0.5)	—	$\mu s$
High period of the SCL clock	$t_{HIGH}$	0.6 (0.26)	—	$\mu s$

Note) Fast-mode Plus supports only available with INCK  $\geq$  8.0 MHz

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### 8-2-5 Gyro Control Interface

Gyro Control Interface supports Serial Peripheral Interface (SPI).  
Gyro Control Interface characteristics are shown below.

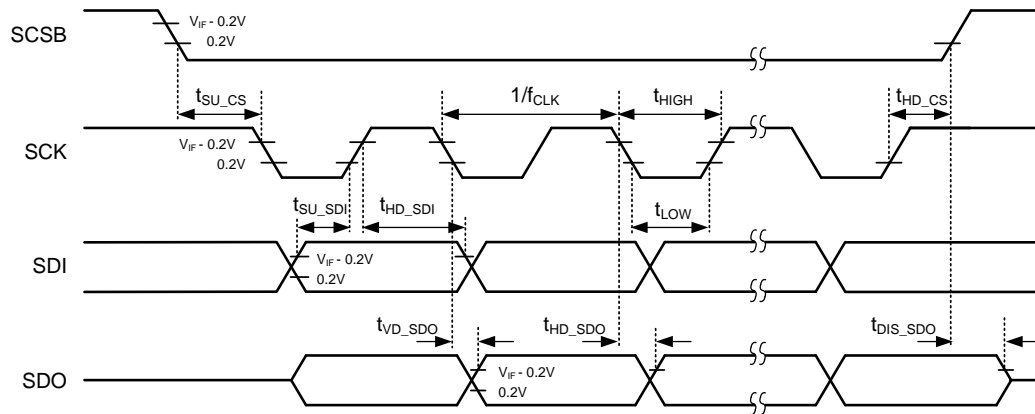


Figure 25 2-wire serial communication block specification

Table 16 2-wire serial communication block AC specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK Clock Frequency	$f_{CLK}$	—	—	1	MHz	
SCLK Low Period	$t_{LOW}$	500	—	—	ns	
SCLK High Period	$t_{HIGH}$	500	—	—	ns	
CS Setup Time	$t_{SU\_CS}$	500	—	—	ns	
CS Hold Time	$t_{HD\_CS}$	500	—	—	ns	
SDI Setup Time	$t_{SU\_SDI}$	11	—	—	ns	
SDI Hold Time	$t_{HD\_SDI}$	7	—	—	ns	
SDO Valid Time	$t_{VD\_SDO}$	—	—	100	ns	
SDO Hold Time	$t_{HD\_SDO}$	4	—	—	ns	
SDO Output Disable Time	$t_{DIS\_SDO}$	—	—	50	ns	
CS high time between transactions	$t_{BUF}$	—	940	—	$\mu s$	

### 8-2-6 Current consumption and standby current

**Table 17 Current consumption and standby current**

(30 frame/s,  $V_{ANA} = 2.8\text{ V}$ ,  $V_{DIG} = 1.05\text{ V}$ ,  $V_{IF} = 1.8\text{ V}$ ,  $T_j = 60\text{ }^{\circ}\text{C}$ )

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	$I_{ANA}$		TBD	TBD	mA	
Current consumption (digital)	$I_{DIG}$		TBD	TBD	mA	Full-resolution, function off
Current consumption (IF)	$I_{IF}$		TBD	TBD	mA	
Standby current (analog)	$I_{STBANA}$			TBD	$\mu\text{A}$	XCLR : Low fixed INCK : stop
Standby current (digital)	$I_{STBDIG}$			TBD	mA	XCLR : Low fixed INCK : stop
Standby current (IF)	$I_{STBIF}$			TBD	$\mu\text{A}$	XCLR : Low fixed INCK : stop

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9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

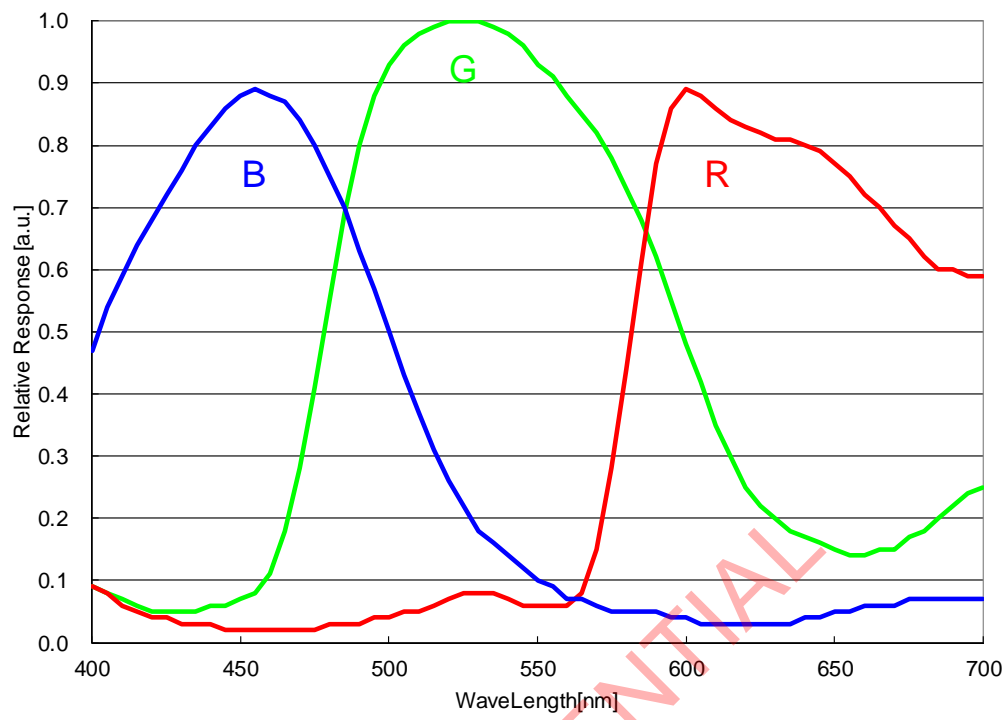


Figure 26 Spectral sensitivity characteristics



## 10. Image Sensor Characteristics

### 10-1 Image Sensor Characteristics

**Table 18 Image Sensor Characteristics**

(30 frame/s,  $V_{ANA} = 2.8\text{ V}$ ,  $V_{DIG} = 1.05\text{ V}$ ,  $V_{IF} = 1.8\text{ V}$ ,  $T_j = 60\text{ }^{\circ}\text{C}$ )

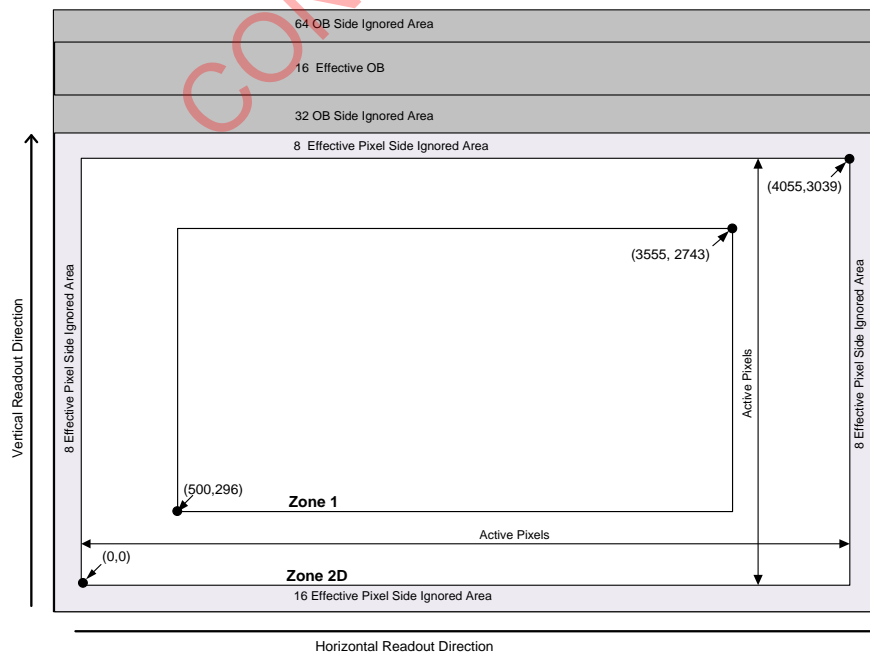
Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	250			LSB	Center	1 <sup>*1</sup>	1/120 s storage
Sensitivity ratio	R	RG	0.40	0.46	0.52	Center	2 <sup>*1</sup>	
	B	BG	0.33	0.39	0.45			
Saturation signal	Vsat	1023			LSB	Zone1	3 <sup>*1</sup>	Include OB level <sup>*2</sup>
Video signal shading	SH			95	%	Zone2D	4 <sup>*1</sup>	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	5 <sup>*1</sup>	When operation at 15 frame/s

The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Note 1) These refer to the descriptions of the section "11-4 Measurement Method".

Note 2) LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value).

### 10-2 Zone Definition used for specifying image sensor characteristics



**Figure 27 Zone Definition Diagram for Image Sensor Characteristics**

## 11. Measurement Method for Image Sensor Characteristics

### 11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

**Table 19 Measurement Conditions**

Supply voltage	Analog 2.8 V, Digital 1.05 V, IF 1.8 V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.

As an example of 1 LSB, the typical value is  $1 \text{ LSB} \approx 0.509 \text{ mV}$  in all-pixel output 10-bit operation mode.

### 11-2 Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

All pixel signals are output successively in a  $1/15 \text{ s}$  period.



**Figure 28 Color coding alignment**

### 11-3 Definition of Standard Imaging Conditions

#### 11-3-1 Standard imaging condition I

Use a pattern box (luminance:  $706 \text{ cd/m}^2$ , color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S ( $t = 1.0 \text{ mm}$ ) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

#### 11-3-2 Standard imaging condition II

A testing lens with CM500S ( $t = 1.0 \text{ mm}$ ) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

#### 11-3-3 Standard imaging condition III

A recommended testing lens with CM500S ( $t = 1.0 \text{ mm}$ ) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

## 11-4 Measurement Method

### 11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After the electronic shutter mode with a shutter speed of 1/150 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of imaging area, and substitute the values into the following formula.

$$S = (VGr + VGb) / 2 \times (150 / 120) \text{ [LSB]}$$

### 11-4-2 Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 341 LSB, measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

$$\begin{aligned} VG &= (VGr + VGb) / 2 \\ RG &= VR / VG \\ RB &= VB / VG \end{aligned}$$

### 11-4-3 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr, Gb signal outputs, 341 [LSB], measure the average value of the Gr, Gb, R and B signal outputs.

### 11-4-4 Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 341 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

$$SH = ((Gmax - Gmin) / Gmax) \times 100 \text{ [%]}$$

### 11-4-5 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 °C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

$$Vdt = (Va - Vb) \times (1/15) / (1/15) - (1/15000) \approx (Va - Vb) \text{ [LSB]}$$

## 12. Spot Pixel Specification

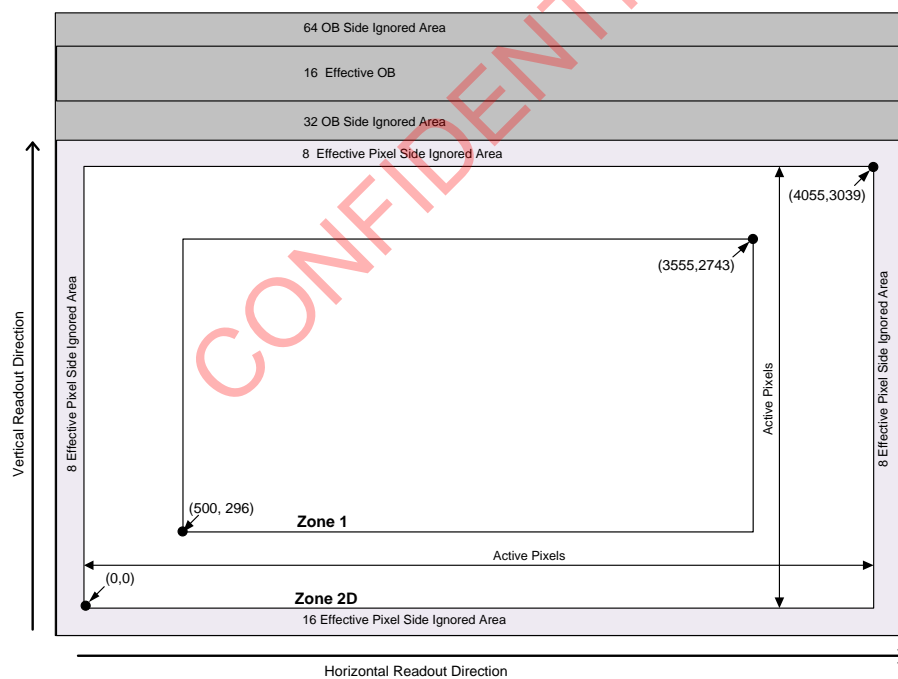
**Table 20 Spot Pixel Specifications**

(15 frame/s,  $V_{ANA} = 2.8\text{ V}$ ,  $V_{DIG} = 1.05\text{ V}$ ,  $V_{IF} = 1.8\text{ V}$ ,  $T_j = 60\text{ }^{\circ}\text{C}$ )

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone		Measurement method	Remarks
		Zone2D	Other		
Black or white pixels at high light	$30\% \leq D$	60	No evaluation criteria applied	12-4-1	
White pixels in the dark	$28\text{ (LSB)} \leq D$	900	No evaluation criteria applied	12-4-2	1/30 storage Note 2)

- Note) 1. D...Spot pixel level.  
 2. Continuous same color pixels in the horizontal or vertical direction are NG.  
 3. Defect pixels are measured with all optional image processing features (DPC) disabled.  
 4. The maximum quantity pixel counts of 60 for Bright Pixels and 900 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any color channels.  
 5. The analog gain for both the Illuminated and Dark defect conditions is 0 dB.

### 12-1 Zone Definition for spot pixel specification



**Figure 29 Zone Definition Diagram for Spot Pixel Specification**

## 12-2 Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards. Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.

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### [For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.

The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

#### Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (T <sub>J</sub> = 60 °C)	Annual number of occurrence
2.9 LSB or higher	13.0 pcs
5.1 LSB or higher	7.3 pcs
12.2 LSB or higher	3.0 pcs
25.5 LSB or higher	1.4 pcs
36.6 LSB or higher	1.0 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

#### For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

### 12-3 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

### 12-4 Spot Pixel Pattern Specifications

#### 12-4-1 Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 341 LSB, measure the local dip point (black pixel at high light,  $V_{XB}$ ) and peak point (white pixel at high light,  $V_{XK}$ ) in the Gr/Gb/R/B signal output  $V_X$  ( $x = \text{Gr/Gb/R/B}$ ), and substitute the values into the following formula.

The 341 LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

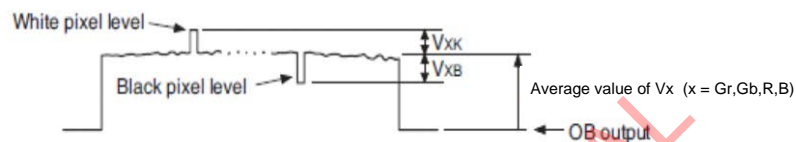
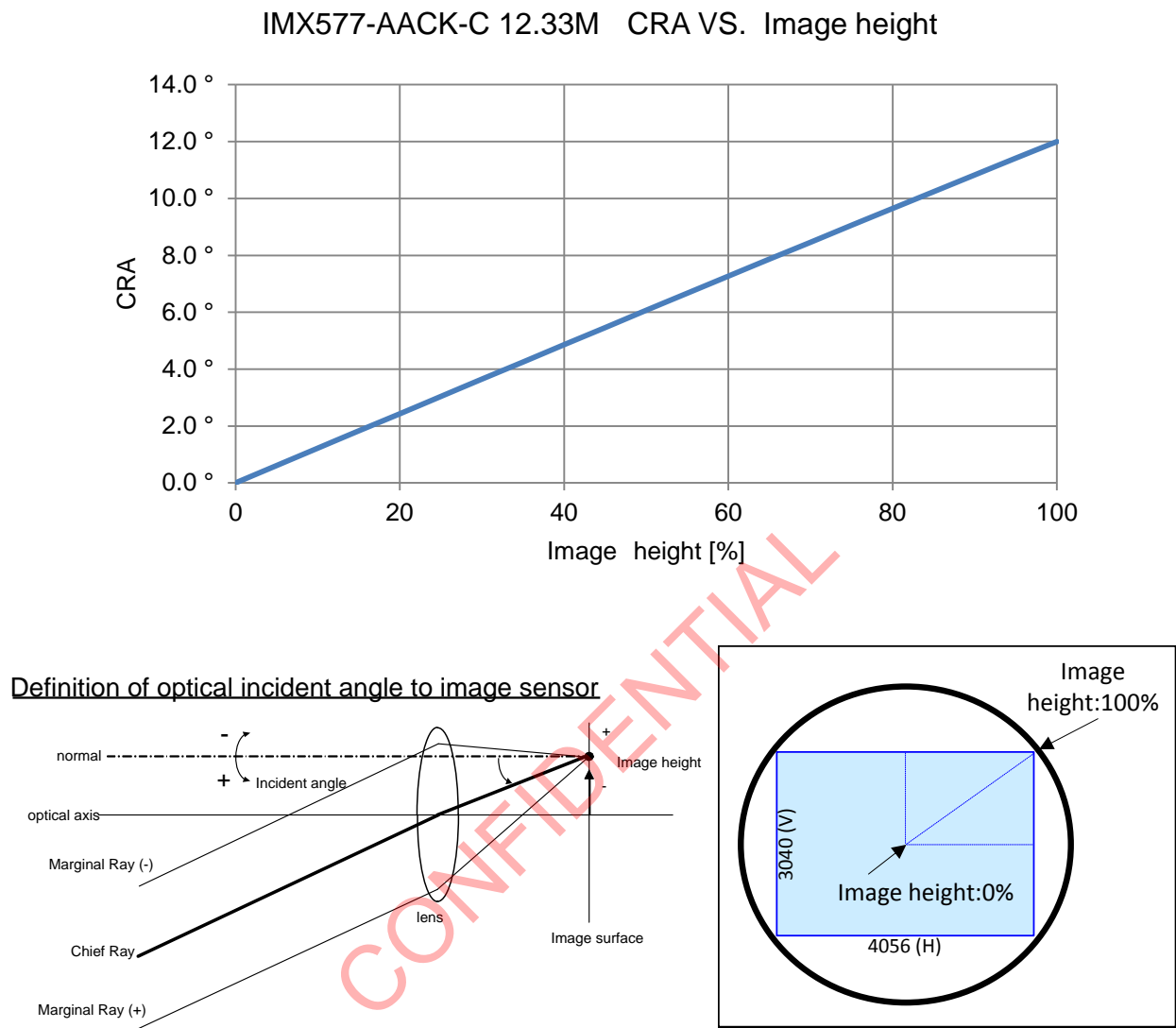


Figure 30 Measurement Method for Spot Pixels

#### 12-4-2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens



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**14. Marking**

TBD

**Figure 32 Marking**

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## 15. Notes on Handling

### 1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- (1) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- (2) Use a wrist strap when handling directly.
- (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
- (4) Ionized air is recommended for discharge when handling image sensors.
- (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

### 2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

- (1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
- (2) Do not touch the glass surface with hand and make any object contact with it.  
If dust or other is stuck to a glass surface, blow it off with an air blower.  
(For dust stuck through static electricity, ionized air is recommended.)
- (3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
- (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

### 3. Installing (attaching)

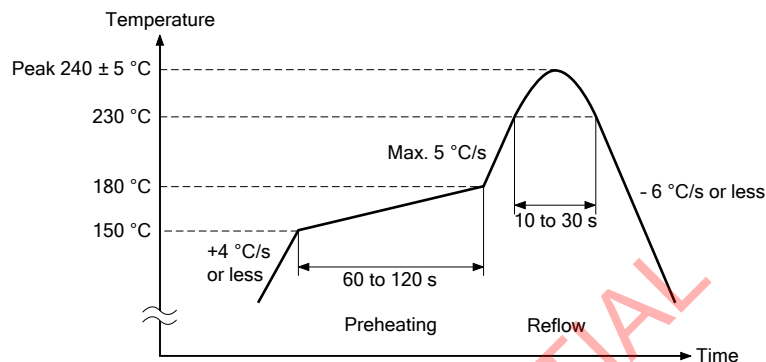
- (1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.  
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
- (2) The adhesive may cause the marking on the rear surface to disappear.
- (3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
- (4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
- (5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

#### 4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

##### (1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



##### (2) Reflow conditions

- Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
- Perform the reflow soldering only one time.
- Finish reflow soldering within 24 h after unsealing the degassed packing.  
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
- Perform re-baking only one time under the condition at 125 °C for 24 h.

##### (3) Others

- Carry out evaluation for the solder joint reliability in your company.
- After the reflow, the paste residue of protective tape may remain around the seal glass.  
(The paste residue of protective tape should be ignored except remarkable one.)
- Note that X-ray inspection may damage characteristics of the sensor.

#### 5. Others

- Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
- Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
- This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
- Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
- Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.



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## 17. List of Trademark Logos and Definition Statements

The logo for Exmor RS, featuring the word "Exmor" in a stylized, italicized font followed by "RS" in a bold, blocky font.

\* Exmor RS is a trademark of Sony Corporation. The Exmor RS is a Sony's CMOS image sensor with high-resolution, high-performance and compact size by replacing a supporting substrate in Exmor R™ which changed fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type, with layered chips formed signal processing circuits.

Sales: Shenzhen Sunnywale Inc, [www.sunnywale.com](http://www.sunnywale.com) , [awin@sunnywale.com](mailto:awin@sunnywale.com) , Wechat: 9308762

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```

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 *
 * $Date:    17. January 2013
 * $Revision: V1.4.1
 *
 * Project:   CMSIS DSP Library
 * Title:    arm_common_tables.h
 *
 * Description: This file has extern declaration for common tables like Bitreverse, reciprocal etc which are used
 across different functions
 *
 * Target Processor: Cortex-M4/Cortex-M3
 *
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 *
 * $Date:    17. January 2013
 * $Revision: V1.4.1
 *
 * Project:   CMSIS DSP Library
 * Title:    arm_const_structs.h
 *
 * Description: This file has constant structs that are initialized for
 *   user convenience. For example, some can be given as
 *   arguments to the arm_cfft_f32() function.
 *
 * Target Processor: Cortex-M4/Cortex-M3
 *
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* $Date:    17. January 2013
* $Revision: V1.4.1
*
* Project:   CMSIS DSP Library
* Title:     arm_math.h
*
* Description: Public header file for CMSIS DSP Library
*
* Target Processor: Cortex-M4/Cortex-M3/Cortex-M0
*
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/\*\*\*\*\*//\*\*

\* @file core\_cm0.h  
 \* @brief CMSIS Cortex-M0 Core Peripheral Access Layer Header File  
 \* @version V3.20  
 \* @date 25. February 2013  
 \*  
 \* @note  
 \*

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\* @file core\_cm0plus.h  
 \* @brief CMSIS Cortex-M0+ Core Peripheral Access Layer Header File  
 \* @version V3.20  
 \* @date 25. February 2013  
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 \* @note  
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/\*\*\*\*\*

\* @file core\_cmFunc.h

\* @brief CMSIS Cortex-M Core Function Access Header File

\* @version V3.20

\* @date 25. February 2013

\*

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\*

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/\*\*\*\*\*

\* @file core\_cmInstr.h

\* @brief CMSIS Cortex-M Core Instruction Access Header File

\* @version V3.20

\* @date 05. March 2013

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\* @note

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\* @version V3.10

\* @date 19. August, 2014

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\* @note

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