SONY

Diagonal 6.08mm (Type 1/3) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX035LQZ-C

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Description

The IMX035LQZ-C is a diagonal 6.08mm (Type 1/3) CMOS active pixel type solid-state image sensor with a square pixel array and 1.39M effective pixels. This chip operates with analog 3.0V and 1.8V, and digital 1.8V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-storage time.
(Applications: Surveillance cameras)

Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Input frequency: 54MHz
- Number of recommended recording pixels: 1280 (H) × 1024 (V) approx. 1.31M pixels
- Supports the following drive modes
  - All-pixel scan mode
  - Horizontal/vertical 2 × 2 addition readout mode
  - Windows cut-out Mode
    Min.: CIF size 352 (H) × 288 (V)
    Max.: VGA size 640 (H) × 480 (V)
  - Vertical 1/2 elimination readout mode
- Variable-speed shutter function (minimum 1H units)
- CDS/PDA function
  - Digital Max. +18dB (6.0dB STEP)
  - Analog Max. +18dB (0.3dB STEP)
- 10/12-bit A/D converter
  - CMOS logic 1 port SDR output
- Recommended lens: F number: 2.8 or more
- Recommended exit pupil distance: –30mm to –∞

E09513B98

Element Structure

- ◆ CMOS image sensor
- ◆ Image size
  Type 1/3
- ◆ Total number of pixels
  1384 (H) × 1076 (V) approx. 1.49M pixels
- ◆ Number of effective pixels
  1329 (H) × 1049 (V) approx. 1.39M pixels
- ◆ Number of active pixels
  1313 (H) × 1041 (V) approx. 1.36M pixels
- ◆ Number of recommended recording pixels
  1280 (H) × 1024 (V) approx. 1.31M pixels
- ◆ Chip size
  7.64mm × 7.64mm
- ◆ Unit cell size
  3.63μm (H) × 3.63μm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 44 pixels, rear 7 pixels
  Vertical (V) direction: Front 24 pixels, rear 3 pixels
- ◆ Number of dummy bits
  Horizontal (H) direction: Front 4 pixels, rear 0 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage (analog 3.0V)	$AV_{DD}0$	–0.3	+3.5	V
Supply voltage (analog 1.8V)	$AV_{DD}1$	–0.3	+2.5	V
Supply voltage (digital)	DV_{DD}, OV_{DD}	–0.3	+2.5	V
Input voltage	V_I	–0.3	DV_{DD} + 0.3	V
Output voltage	V_O	–0.3	OV_{DD} + 0.3	V
Operating temperature	Topr	–10	+60	˚C
Storage temperature	Tstg	–30	+80	˚C
Performance guarantee temperature	Tspec	–10	+60	˚C

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.0V)	$AV_{DD}0$	2.85	3.00	3.15	V
Supply voltage (analog 1.8V)	$AV_{DD}1$	1.70	1.80	1.90	V
Supply voltage (diagital 1.8V)	DV_{DD}, OV_{DD}	1.70	1.80	1.90	V

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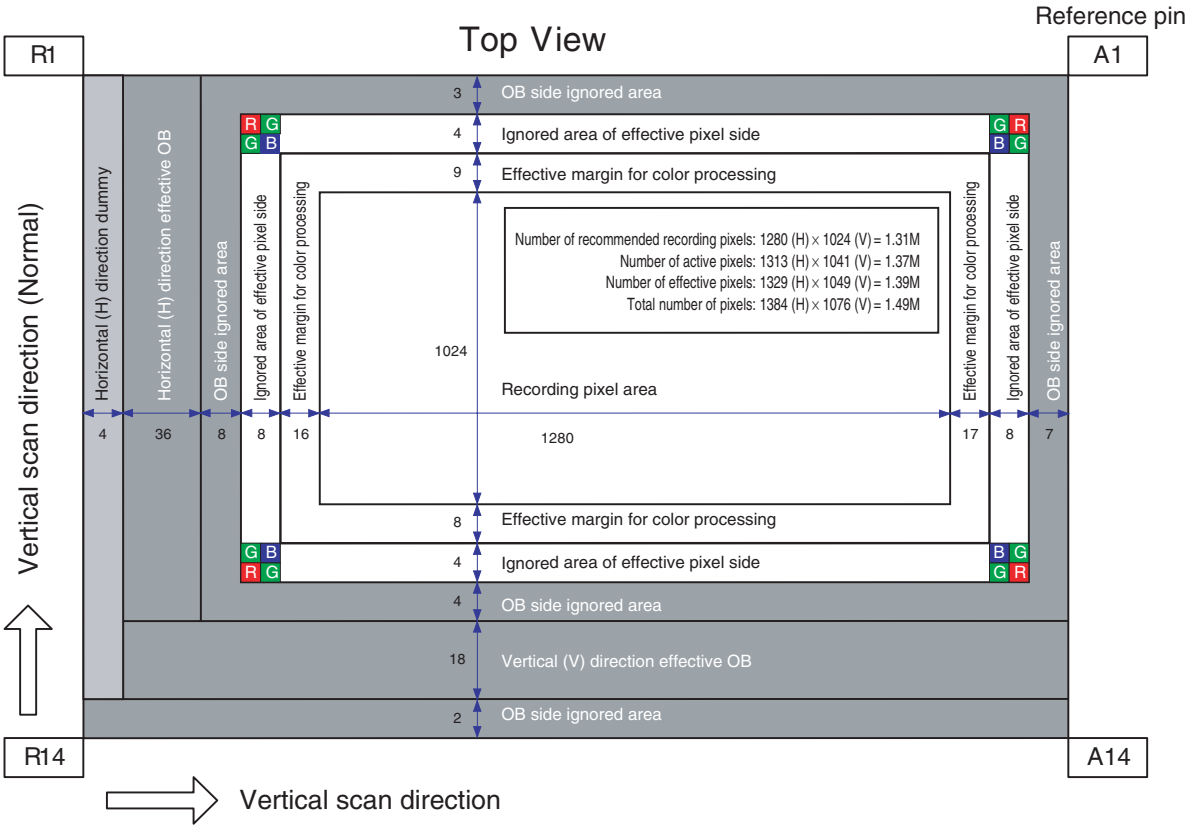
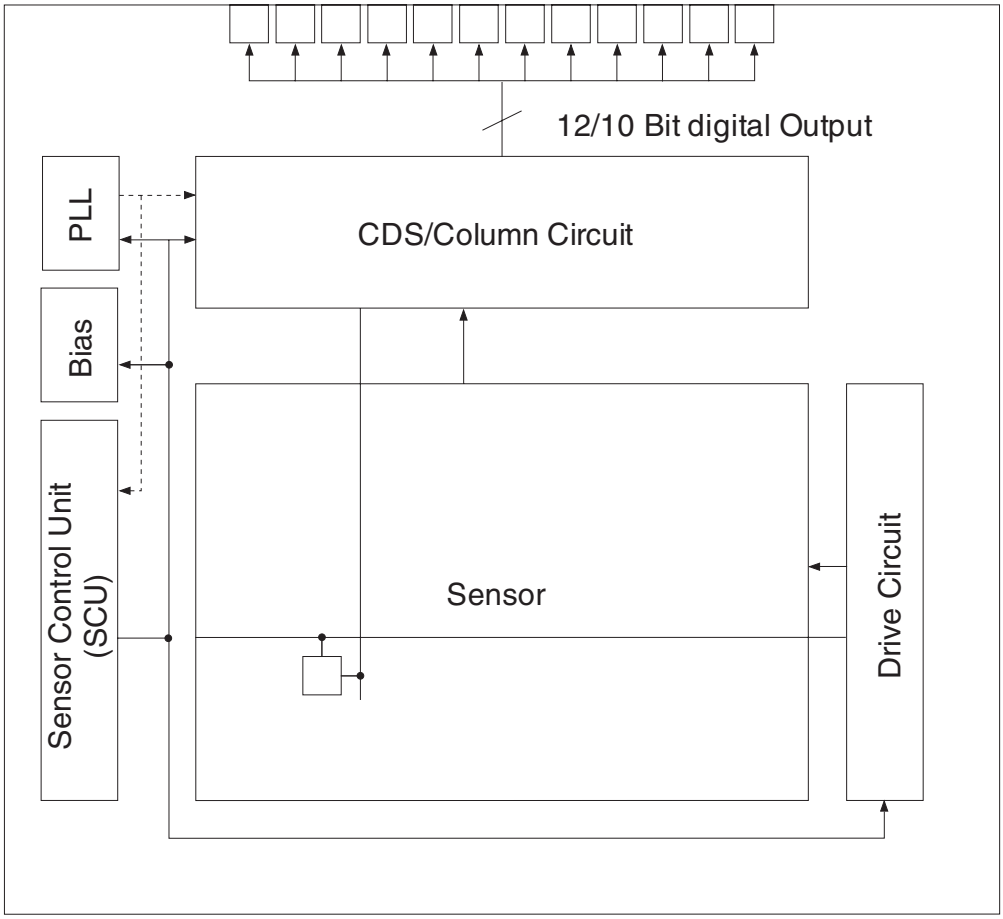
Product structure

1. Pixel Array (Physical Image)

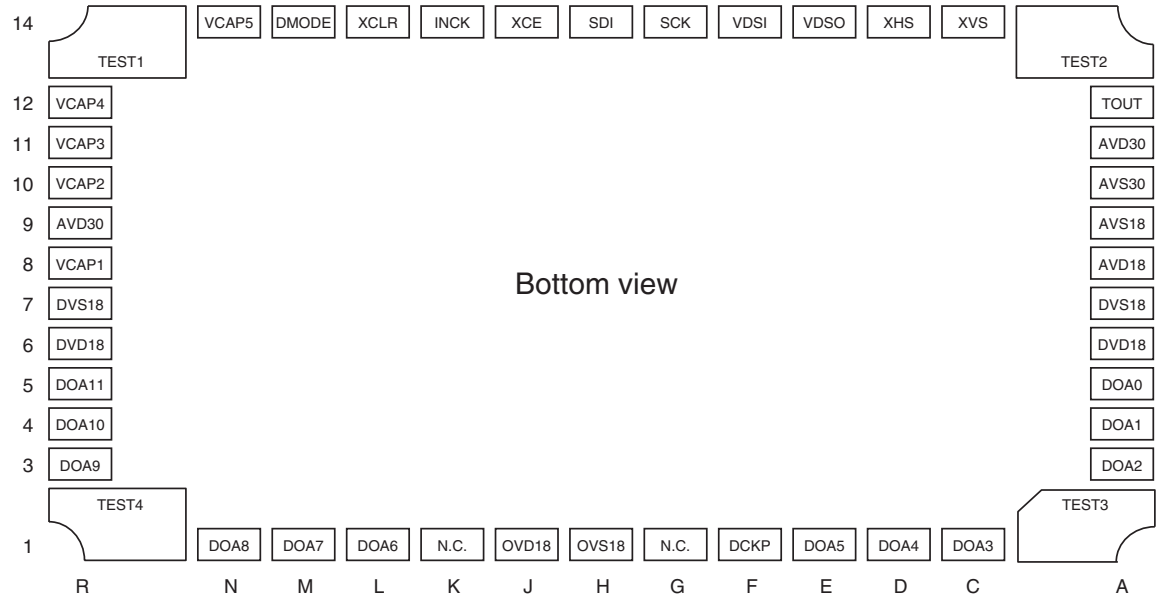


* Reference pin number is consecutive numbering of package pin array. See the Pin Configuration for the number of each pin.

2. Block Diagram



3. Pin Configuration



Pin Description

No.	Pin.No.	I/O	Analog/ Digital	Symbol	Description	Remarks
1	A5	O	D	DOA0	Digital output (DO0)	
2	A4	O	D	DOA1	Digital output (DO1)	
3	A3	O	D	DOA2	Digital output (DO2)	
4	C1	O	D	DOA3	Digital output (DO3)	
5	D1	O	D	DOA4	Digital output (DO4)	
6	E1	O	D	DOA5	Digital output (DO5)	
7	F1	O	D	DCKP	Digital output timing clock (DCK)	
8	G1	O	D	N.C.	No connection	OPEN
9	H1	GND	D	OVS18	GND for output buffer (digital 1.8V)	
10	J1	Power	D	OVD18	Power supply for output buffer (digital 1.8V)	
11	K1	O	D	N.C.	No connection	OPEN
12	L1	O	D	DOA6	Digital output (DO6)	
13	M1	O	D	DOA7	Digital output (DO7)	
14	N1	O	D	DOA8	Digital output (DO8)	
15	R3	O	D	DOA9	Digital output (DO9)	
16	R4	O	D	DOA10	Digital output (DO10)	
17	R5	O	D	DOA11	Digital output (DO11)	
18	F14	GND	A	VDSI	Connect to VDSO pin	
19	E14	GND	A	VDSO	Connect to VDSI pin	
20	R8	TEST	A	VCAP1	Reference pin	Connect an external capacitor.
21	R10	TEST	A	VCAP2	Reference pin	Connect an external capacitor.
22	R11	TEST	A	VCAP3	Reference pin	Connect an external capacitor.
23	R12	TEST	A	VCAP4	Reference pin	Connect an external capacitor.
24	N14	TEST	A	VCAP5	Reference pin	Connect an external capacitor.
25	L14	I	D	XCLR	System clear	
26	K14	I	D	INCK	Master clock	
27	J14	I	D	XCE	Serial interface (Communication enable)	
28	H14	I	D	SDI	Serial interface (Register value input)	
29	G14	I	D	SCK	Serial interface (Communication clock input)	
30	D14	I/O	D	XHS	Horizontal sync pulse	
31	C14	I/O	D	XVS	Vertical sync pulse	
32	R9	Power	A	AVD30	Analog 3.0V power supply	
33	A11	Power	A	AVD30	Analog 3.0V power supply	

No.	Pin.No.	I/O	Analog/ Digital	Symbol	Description	Remarks
34	A10	GND	A	AVS30	Analog 3.0V GND	
35	A8	Power	A	AVD18	Analog 1.8V power supply	
36	A9	GND	A	AVS18	Analog 1.8V GND	
37	A6	Power	D	DVD18	Digital 1.8V power supply	
38	R6	Power	D	DVD18	Digital 1.8V power supply	
39	A7	GND	D	DVS18	Digital 1.8V GND	
40	R7	GND	D	DVS18	Digital 1.8V GND	
41	A12	TEST	D	TOUT	Serial interface (Register value output)	
42	R14	TEST	A	TEST1	Test pin	OPEN
43	A14	TEST	D	TEST2	Test pin	OPEN
44	A1	TEST	D	TEST3	Test pin	10kΩ Pull Down
45	R1	TEST	D	TEST4	Test pin	10kΩ Pull Down
46	M14	TEST	D	DMODE	In slave mode: High/In master mode: Low	High: 1.8V/Low: GND

Electrical Characteristics

1. DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VAD30	$AV_{DD}0$		2.85	3.00	3.15	V
		VAD18	$AV_{DD}1$		1.70	1.80	1.90	V
	Digital	DVD18	DV_{DD}		1.70	1.80	1.90	V
		OVD18	OV_{DD}		1.70	1.80	1.90	V
Digital input voltage		XCLR INCK SCK SDI XCE XHS XVS DMODE	V_{IH}		0.8DV_{DD}			V
			V_{IL}				0.2DV_{DD}	V
Digital output voltage		DOA [11:0] DCKP	V_{OH}	IOH = –6mA	OV_{DD} – 0.4			V
			V_{OL}	IOL = 6mA			0.4	V
		XHS XVS TOUT	V_{OH}	In master mode	DV_{DD} – 0.4			V
			V_{OL}	In master mode			0.4	V

2. Current Consumption

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Operating current	Analog	VAD30	$I_{AVDD}0$	—	57	67	mA
		VAD18	$I_{AVDD}1$	—	0.1	0.1	mA
	Digital	DVD18 OVD18	I_{DVDD}	—	64	87	mA
Standby current	Analog	VAD30	$I_{AVDD}0\_STB$	—	—	21	μA
		VAD18	$I_{AVDD}1\_STB$	—	—	1	μA
	Digital	DVD18 OVD18	I_{DVDD_STB}	—	—	1900	μA

*1 INCK = 54MHz, CMOS logic, all-pixel 30fps, 12-bit output

Maximum value condition: $AV_{DD}0$ = 3.15V, $AV_{DD}1$ = DV_{DD} = OV_{DD} = 1.9V, Ta = 60℃, Standard imaging condition I

Typical value condition: $AV_{DD}0$ = 3.00V, $AV_{DD}1$ = DV_{DD} = OV_{DD} = 1.8V, Ta = 25℃, Standard imaging condition I

3. Power consumption

Item	Pins	Symbol	Min.	Typ.	Max.	Unit
Analog power consumption	VAD30	P_{AVDD0}	—	171	211	mW
	AVD18	P_{AVDD1}	—	0.3	0.3	mW
Digital power consumption	DVD18	P_{DVDD}	—	115	165	mW
	OVD18					
Total			—	287	377	mW

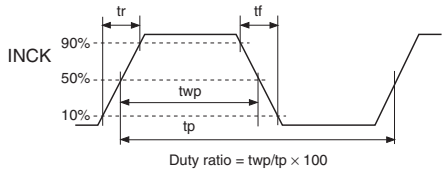
*1 INCK = 54MHz, CMOS logic, all-pixel 30fps, 12-bit output

Maximum value condition: $AV_{DD}0$ = 3.15V, $AV_{DD}1$ = DV_{DD} = OV_{DD} = 1.9V, Ta = 60℃, Standard imaging condition I

Typical value condition: $AV_{DD}0$ = 3.00V, $AV_{DD}1$ = DV_{DD} = OV_{DD} = 1.8V, Ta = 25℃, Standard imaging condition I

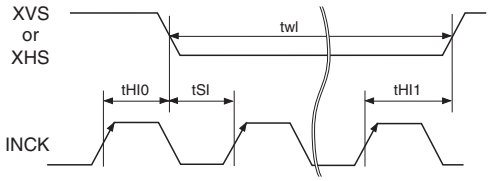
4. AC Characteristics

a). Master Clock Waveform Diagram



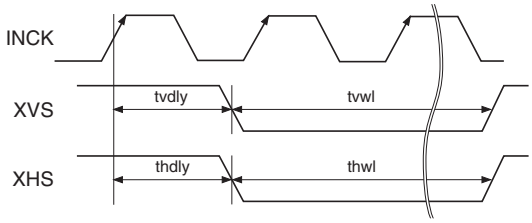
Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{inck}	53.0	54.0	55.0	MHz
INCK clock period	tp	1000/55	1000/54	1000/53	ns
Rise, fall time	tr, tf			2.0	ns
Duty ratio	Duty	45.0	50.0	55.0	%

b). Input characteristics in slave mode (DMODE pin = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XVS Low level width	twl	2		100	INCK
XVS input setup time	tSI	5			ns
XVS input hold time	tHI0, tHI1	0			ns
XHS Low level width	twl	2		100	INCK
XHS input setup time	tSI	5			ns
XHS input hold time	tHI0, tHI1	0			ns

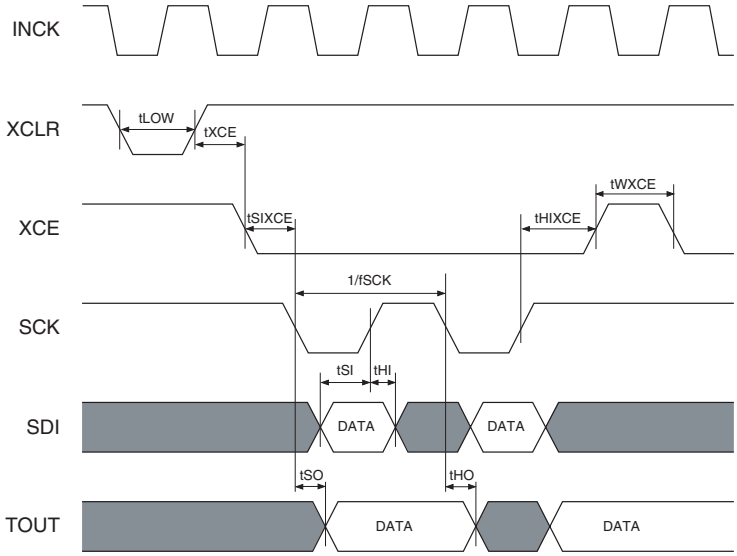
c). Output characteristics in master mode (DMODE pin = Low)



(Output load capacitance: 20pF)

Item	Symbol	Min.	Typ.	Max.	Unit
XVS Low level width	tvwl	1	6	7	H
XVS output delay	tvdly			17	ns
XHS Low level width	thwl	1	6	7	INCK
XHS output delay	thdly			17	ns

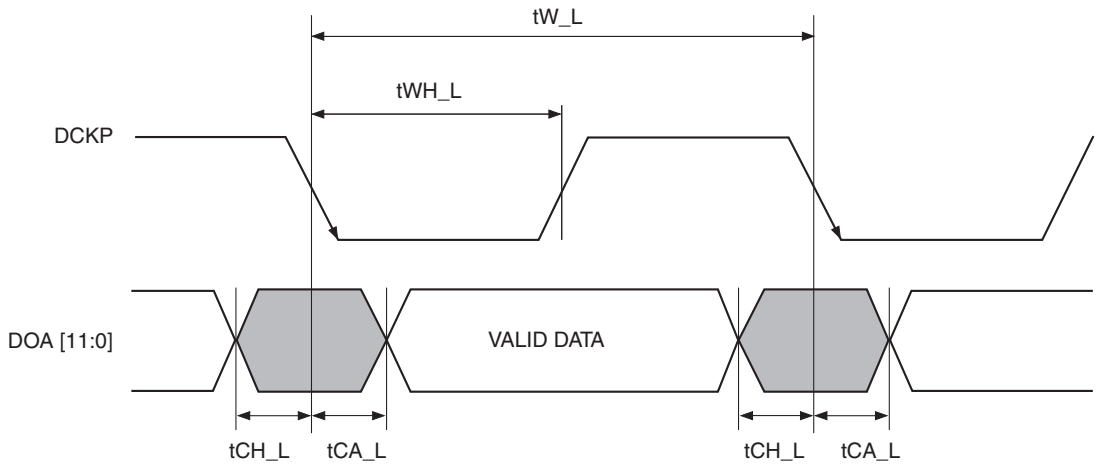
d). Serial Communication



(Output load capacitance: 20pF)

Item	Symbol	Min.	Typ.	Max.	Unit
XCE enable time	tXCE	100			ns
Reset Low level width	tLOW	500			ns
SCK clock frequency	fSCK			13.5	MHz
SDI input setup time	tSI	10			ns
SDI input hold time	tHI	0			ns
TOUT output setup time	tSO			22	ns
TOUT output hold time	tHO	6			ns
XCE input setup time	tSIXCE	20			ns
XCE input hold time	tHIXCE	0			ns
XCE High level width	tWXCE	10			ns

e). DCKP, DOA



(Output load capacitance: 20pF)

Item	Symbol	Min.	Typ.	Max.	Unit
DCKP clock period	tW_L		1000/54		ns
DCKP clock duty	tWH_L	40	50	60	%
Clock access time	tCA_L			2	ns
Output hold time	tOH_L			2	ns

Note) The output clock “DCKP” is output async with the input clock “INCK”.

Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

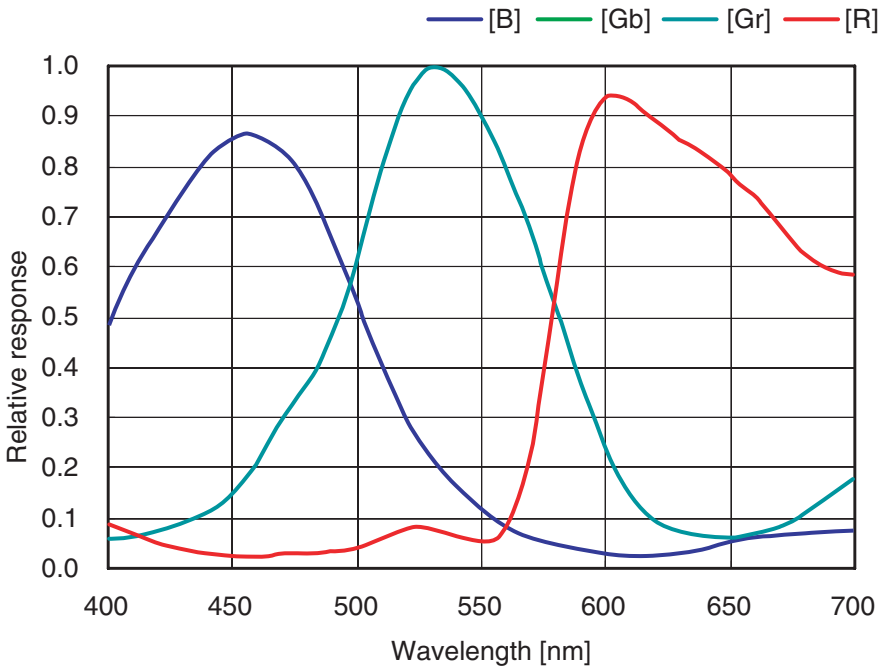


Image Sensor Characteristics

($AV_{DD}0$ = 3.0V, $AV_{DD}1/DV_{DD}/OV_{DD}$ = 1.8V, Ta = 60℃, Gain = 0dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measure-ment method	Remarks
G sensitivity		S	400	460		mV	1	
Sensitivity ratio	R/G	RG	0.4		0.6		2	
	B/G	BG	0.55		0.75			
Saturation signal		Vsat01	830			mV	3	Zone0, I
		Vsat2D	820			mV		Zone0, zoneI, zoneII and zoneII'
Video signal shading		SH01			20	%	4	Zone0, I
		SH2D			25	%		Zone0, zoneI, zoneII and zoneII'
Dark signal		Vdt			2	mV	5	1/30s storage
Dark signal shading		ΔVdt			1	mV	6	1/30s storage
Horizontal stripe R		Lcr			6	%	7	
Horizontal stripe B		Lcb			6	%		
Lag		Lag			0.5	%	8	

Note) 1. Converted value into mV using 1digit = 0.265mV (When 12-bit output) and 1digit = 1.06mV (When 10-bit output).

2. The video signal shading shows the measured values in the wafer state (including color filter) and do not include the characteristics of the cover glass.

Zone Definition of Video Signal Shading

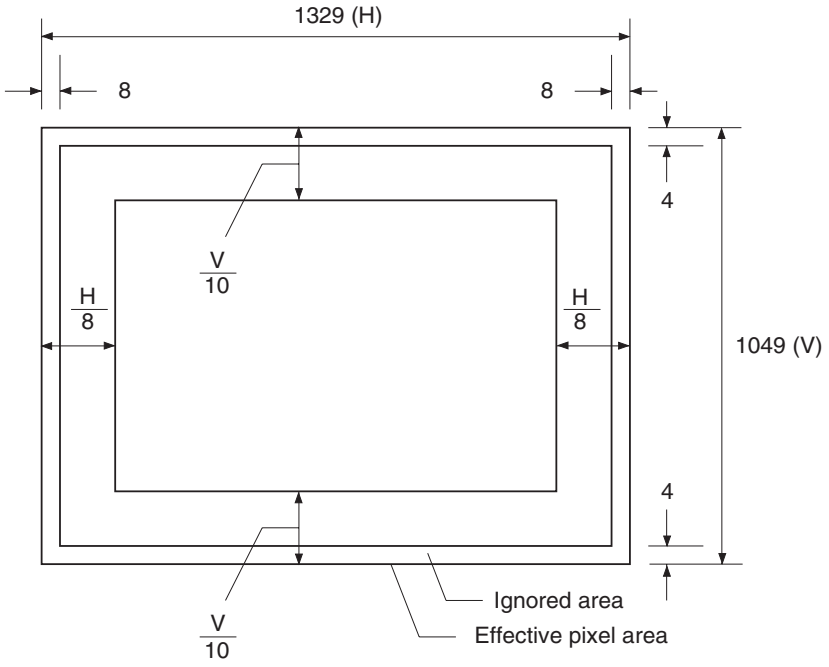


Image Sensor Characteristics Measurement Method

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

Color coding and readout of this image sensor

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –30mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement method

1. Sensitivity
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the Gr and Gb signal outputs (V_{Gr}, V_{Gb}) at the center of the screen, and substitute the values into the following formula.

$$S = (V_{Gr} + V_{GB})/2 \times 100/30 \text{ [mV]}$$

2. Sensitivity ratio
Set to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal outputs is 400mV, measure the R signal output (V_R [mV]), the Gr and Gb signal outputs (V_{Gr}, V_{Gb} [mV]) and B signal output (V_B [mV]) at the center of the screen with the frame readout method, and substitute the values into the following formulas.

$$VG = (V_{Gr} + V_{Gb})/2$$
$$RG = V_R/V_G$$
$$BG = V_B/V_G$$

3. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 400mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
Set to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 400mV. Then measure the maximum value (Gmax [mV]) and minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

$$SH = (Gmax - Gmin)/400 \times 100 \text{ [\%]}$$

5. Dark signal
With the device ambient temperature of 60°C and the device in the light-obstructed state, divide the output difference between 1/30s storage and 1/300s storage by 0.9, and calculate the signal output converted to 1/30s storage. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
After the measurement item 5, measure the maximum value (Vdmax [mV]) and minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

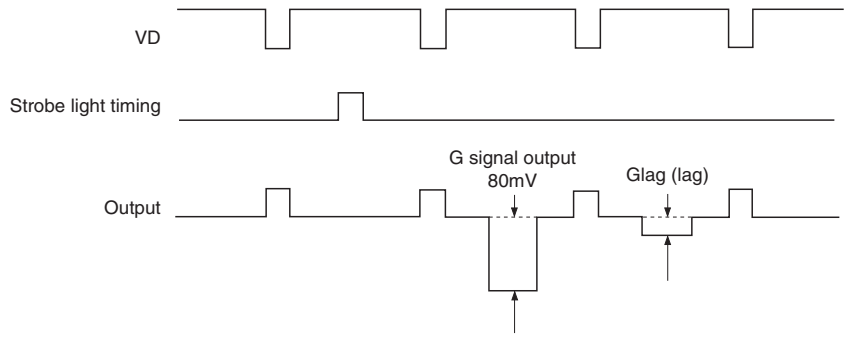
$$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Horizontal stripe
   Set to the standard imaging condition II. After adjusting so that the average value of the Gr signal output is 400mV, insert R and B filters and measure the difference between G signal lines (ΔGlr, ΔGlb [mV]) as well as the average values of the G signal outputs (Gar, Gab). Substitute the values into the following formula.

   $Lci = (\Delta Gli/Gai) \times 100$ [%] (i = r, b)

8. Lag
   Adjust the G signal output value generated by the strobe light to 80mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal level (Glag), and substitute the value into the following formula.

   $Lag = (Glag/80) \times 100$ [%]



Spot Pixel Specifications

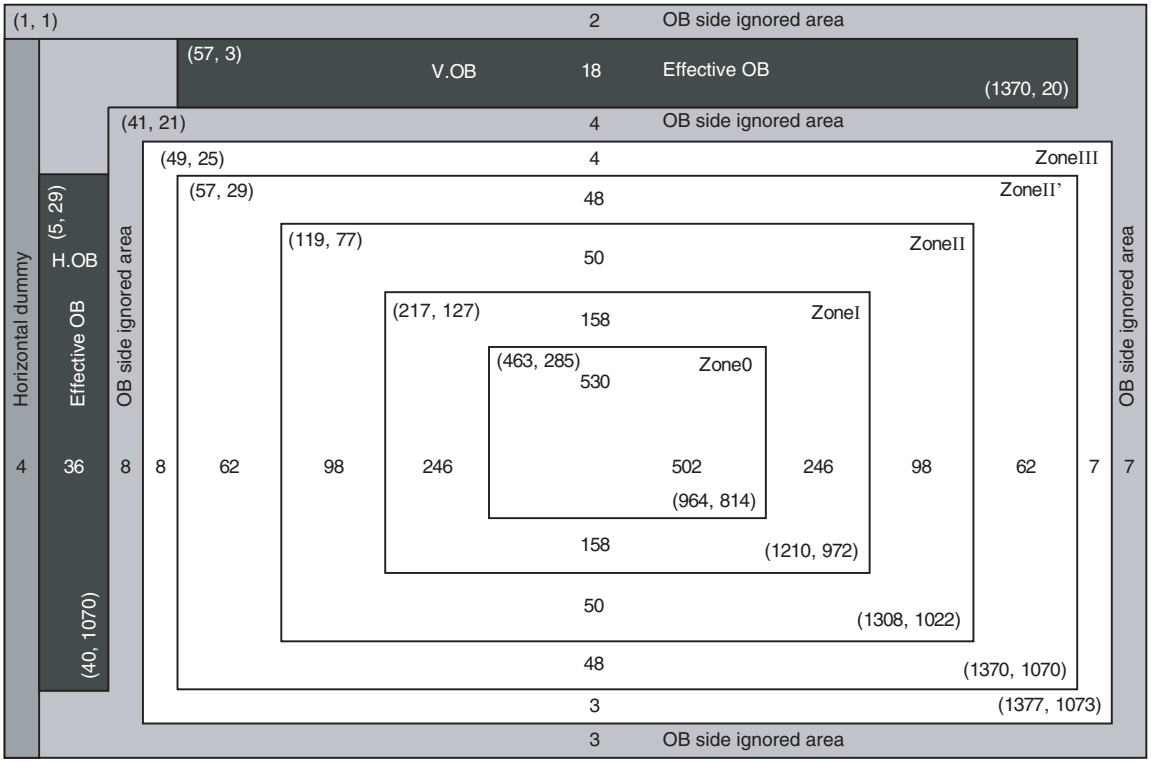
Spot Pixel Specifications

(Ta = 60℃)

Spot pixel	Spot pixel level	Number of allowable spot pixels by zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30% ≤ D	10	No evaluation criteria applied			1	
White pixels in the dark	5.6mV ≤ D	120		No evaluation criteria applied		2	1/30s storage
Black pixels at signal saturated	D ≤ 626mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode.
2. D...Spot pixel level.
3. As for black pixels, white pixels and white pixels in the dark in the horizontal direction, 2 pixels or more within 3 pixels with the same color are rejected, and also 2 adjacent pixels are rejected. As for white pixels in the dark in the vertical direction, 2 adjacent pixels are rejected.

Zone Definition



Notice on White Pixels Specifications

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After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as “White Pixels”.) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards. Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the “Seller”) will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth on the previous page under the heading “Spot Pixels Specifications”, within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products. Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Occurrence Rate of White Pixels

The chart below shows the predictable data on the occurrence rates of White Pixels in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against White Pixels, such as adoption of automatic compensation systems appropriate for each occurrence rate of White Pixels. The data in the chart is based on records of past field tests, and signifies estimated occurrence rates calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Occurrence Rates

White Pixel Level (in case of storage time = 1/30s) (Ta = 60℃)	Occurrence Rate per week
5.6mV or higher	2.7%
10.0mV or higher	1.7%
24.0mV or higher	0.8%
50.0mV or higher	0.4%
72.0mV or higher	0.3%

Note 1) The above data indicates the average occurrence rate of a single White Pixels that will occur when a CMOS image sensor is left for a week.
For example, in a case of a device that has a 1% occurrence rate per week at the 5.6mV or higher effect level, this means that if 1,000 devices are left for a week, a total of 10 devices out of the whole 1,000 devices will have a single White Pixels at the 5.6mV or higher effect level.

Note 2) The occurrence rate of White Pixels fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the occurrence rate of White Pixels.

For Your Reference:

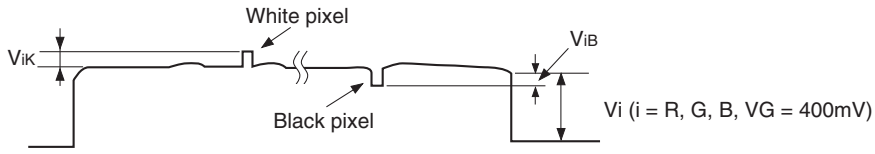
The occurrence rate of White Pixels at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the occurrence rate of White Pixels in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions.Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value of the Gr/Gb/R/B signal outputs is 400mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr/Gb/R/B signal output Vi (i = Gr/Gb/R/B), and substitute the value into the following formula.

   Spot pixel level D = ((V_{iB} or V_{iK})/Average value of Vi) × 100 [%]



Signal output waveform of R/G/B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

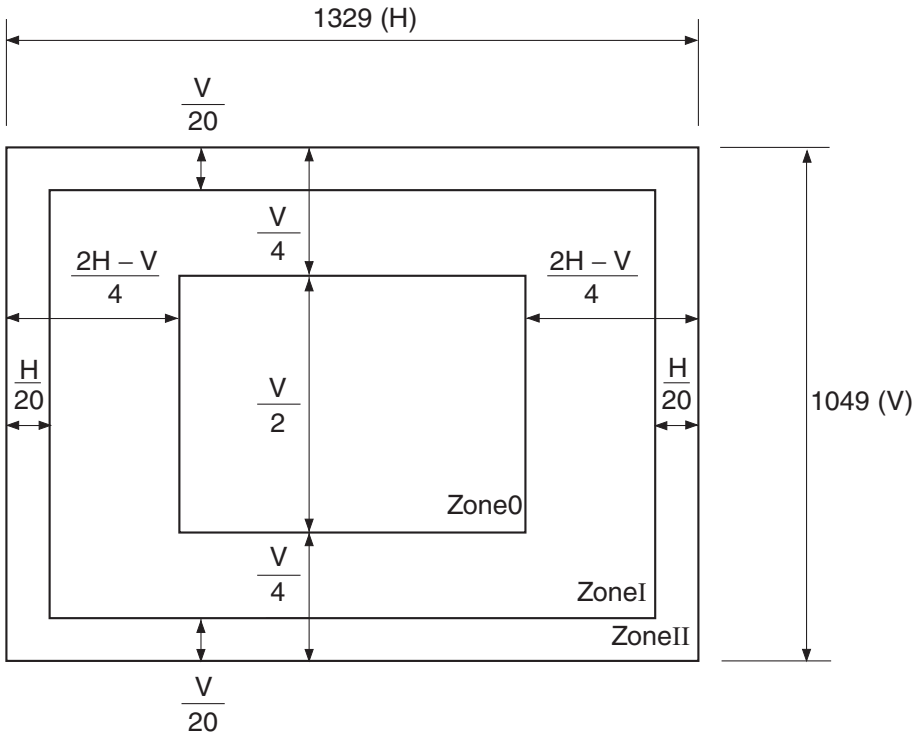
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

Signal output waveform of R/G/B channel

Stain Specifications

Zone	Allowable pixels	Size	Level	Lens diaphragm
0 to II	0	L ≥ 3	R ≥ 8%	F = 16
Means no stain over three lines or more.				

Stain Zone Definition

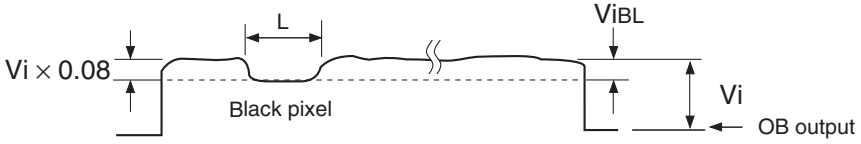


Stain Measurement Method

In the following measurement, set to the standard imaging condition II and adjust the luminous intensity with the lens diaphragm at F16 so that the average value of the G channel signal output is 150mV. Measure the local dip in the average value of the R/G/B channel signal output (V_{iBL}) and then calculate the stain level (R) from the ratio with the average value of the R/G/B channel signal output (Vi).

Stain level R = $(V_{iBL}/Vi) \times 100$ [%] (i = R, G, B)

At the same time, the size (L) of the area where the stain level is 8% or more is determined by line number conversion. The distance from one center of a stain to another is the stain interval, and is also determined in the same fashion by line number conversion.



Signal output waveform of R/G/B channel

Register Map

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
00h	0	STBY	Standby mode switching 0: Normal operation, 3: Standby operation, Others: Setting prohibited	3h	Reflected immediately
	1				
	2	TESTEN	Enables the register setting of address 30h or more. 0: Write disabled, 3: Write enabled, Others: Invalid	0h	Reflected immediately
	3				
	4		(Reserved)		
	5		(Reserved)		
	6		(Reserved)		
	7		(Reserved)		
01h	0	MODE [3:0]	Drive mode switching 0: All-pixel scan, 2: Windows cut-out Mode, 4: Vertical 1/2 elimination, 5: 2 × 2 addition readout, Others: Setting prohibited	0h	(1)
	1				
	2				
	3				
	4	VREVERSE	Vertical scanning direction control 0: Normal, 1: Inverted	0	(1)
	5		Fixed to “0”.	0	
	6		Fixed to “0”.	0	
	7		(Reserved)		
02h	0		Fixed to “1”.	1	
	1		Fixed to “1”.	1	
	2		Fixed to “0”.	0	
	3		Fixed to “0”.	0	
	4		Fixed to “0”.	0	
	5		Fixed to “0”.	0	
	6		Fixed to “0”.	0	
	7		Fixed to “0”.	0	
03h	0	ADRES	Output gradation switching 0: 10-bit output, 2: 12-bit output, Others: Setting prohibited	0h	(1)
	1				
	2		Fixed to “0”.	0	
	3		Fixed to “0”.	0	
	4		Fixed to “0”.	0	
	5		(Reserved)		
	6		(Reserved)		
	7		(Reserved)		
04h	0	FRSEL	Select data rate of the data to be output See the item of “8. Drive Modes”.	3h	(1)
	1				
	2				
	3		Fixed to “0”.	0	
	4		Fixed to “1”.	1	
	5		Fixed to “0”.	0	
	6		(Reserved)		
	7		(Reserved)		
05h	0	SSBRK	Low-speed shutter forced end control See the item of “6-4. Long Exposure Operation”.	0	(1)
	1		Fixed to “0”.	0	
	2		Fixed to “0”.	0	
	3		Fixed to “0”.	0	
	4		(Reserved)		
	5		(Reserved)		
	6		(Reserved)		
	7		(Reserved)		

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
06h	0	SVS [9:0]	LSB When setting long time storage, number of storage frames is specified. See the item of “6-4. Long Exposure Operation”.	000h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7				
07h	0				
	1		MSB		
	2		(Reserved)		
	3		(Reserved)		
	4		(Reserved)		
	5		(Reserved)		
	6		(Reserved)		
	7		(Reserved)		
08h	0	SHS1 [15:0]	LSB	0000h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7		Storage time setting in 1H units See the item of “6-2. Normal Exposure Operation”.		
09h	0				
	1				
	2				
	3				
	4				
	5				
	6				
	7		MSB		
12h	0	SPL1 [9:0]	LSB	000h	(1)
	1				
	2				
	3				
	4		When long time storage, number of sweep frames is specified. See the item of “6-4. Long Exposure Operation”.		
	5				
	6				
	7				
13h	0				
	1		MSB		
	2		Fixed to “0”.	0	
	3		Fixed to “0”.	0	
	4		Fixed to “0”.	0	
	5		Fixed to “0”.	0	
	6		Fixed to “0”.	0	
	7		Fixed to “0”.	0	

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
16h	0	WINPH [10:0]	LSB When windows cut-out Mode, horizontal address in readout start origin is specified. See the item of “8-3. Windows cut-out Mode”.	000h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7				
17h	0				
	1				
	2		MSB		
	3		(Reserved)		
	4	WINPV [10:0]	LSB When windows cut-out Mode, vertical address in readout start origin is specified. See the item of “8-3. Windows cut-out Mode”.	000h	(1)
	5				
	6				
	7				
18h	0				
	1				
	2				
	3				
	4				
	5				
	6		MSB		
	7		(Reserved)		
19h	0	WINWH [10:0]	LSB When windows cut-out Mode, horizontal direction width in readout area is specified. See the item of “8-3. Windows cut-out Mode”.	534h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7				
1Ah	0				
	1				
	2		MSB		
	3		(Reserved)		
	4	WINWV [10:0]	LSB When windows cut-out Mode, vertical direction width in readout area is specified. See the item of “8-3. Windows cut-out Mode”.	419h	(1)
	5				
	6				
	7				
1Bh	0				
	1				
	2				
	3				
	4				
	5				
	6		MSB		
	7		(Reserved)		

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
1Ch	0	AGAING [12:0]	LSB	1000h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7		Analog gain setting See the item of “3. Gain Adjustment Function”.		
1Dh	0				
	1				
	2				
	3				
	4		MSB		
	5		Fixed to “0”.	0	
	6		Fixed to “0”.	0	
	7		(Reserved)	0	
1Eh	0	DGAING	Gr/Gb pixel digital gain setting See the item of “3. Gain Adjustment Function”.	0h	(1)
	1				
	2	DGAINR	R pixel digital gain setting See the item of “3. Gain Adjustment Function”.	0h	(1)
	3				
	4	DGAINB	B pixel digital gain setting See the item of “3. Gain Adjustment Function”.	0h	(1)
	5				
	6		Fixed to “0”.	0	
	7		Fixed to “0”.	0	
1Fh	0	BLKLEVEL [8:0]	LSB	000h	(1)
	1				
	2				
	3				
	4				
	5				
	6				
	7		Black level offset value setting See the item of “4. Black Level Adjustment”.		
20h	0		MSB		
	1		(Reserved)		
	2		(Reserved)		
	3		(Reserved)		
	4		Fixed to “0”.	0	
	5		Fixed to “0”.	0	
	6		(Reserved)		
	7		(Reserved)		

26h	0	XMSTA	Master mode operation starts by switching to 0h.	1	Reflected immediately
	1		(Reserved)		
	2		(Reserved)		
	3		(Reserved)		
	4		(Reserved)		
	5		(Reserved)		
	6		(Reserved)		
	7		(Reserved)		

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
53h	0		Fixed to “1”.	1	
	1	XHSLNG	When master mode operation, output XHS signal width specification 0h: 1 clk width, 1h: 2 clk width, ...6h: 7 clk width, 7h: Setting invalid	5h	Reflected immediately
	2				
	3				
	4	XVSLNG	When master mode operation, output XVS signal width specification 0h: Setting invalid, 1h: 1H width, 2h: 2H width, ...6h: 6H width, 7h: 7H width	6h	Reflected immediately
	5				
	6				
	7		(Reserved)		

62h	[7:0]		Fixed to “32h” *4	04h	Reflected immediately

7Ch	0	VMAX [15:0]	LSB	0000h	Reflected immediately
	1				
	2				
	3				
	4				
	5				
	6				
	7		When master mode operation, vertical period specification See the item of “8. Drive Modes”.		
7Dh	0				
	1				
	2				
	3				
	4				
	5				
	6				
	7		MSB		
7Eh	0		Fixed to “0”.	0	
	1		Fixed to “0”.	0	
	2		Fixed to “0”.	0	
	3		Fixed to “0”.	0	
	4	HMAX [11:0]	LSB	000h	Reflected immediately
	5				
	6				
	7				
7Fh	0		When master mode operation, horizontal period specification See the item of “8. Drive Modes”.		
	1				
	2				
	3				
	4				
	5				
	6				
	7		MSB		

90h	[7:0]		Fixed to “48h” *4	02h	Reflected immediately
9Bh	[7:0]		Fixed to “29h” *4	01h	Reflected immediately
A3h	[7:0]		Fixed to “44h” *4	A4h	Reflected immediately
A4h	[7:0]		Fixed to “28h” *4	27h	Reflected immediately

Address	Bit	Symbol	Description	Default value after reset	Reflection timing
B4h	[7:0]		Fixed to “8Ah” *4	80h	Reflected immediately
B9h	[7:0]		Fixed to “44h” *4	A4h	Reflected immediately
BAh	[7:0]		Fixed to “28h” *4	27h	Reflected immediately
FEh	[7:0]		Fixed to “08h” *4	00h	Reflected immediately

*1 When STBY (address 00h [1:0]) = 3, writing data to the register is prohibited other than the address 00h.

*2 Do not send data to addresses not listed on the register map. Doing so may result in misoperation. However, other registers to require communication to the addresses not listed above may be added. Address setting should be available to FFh.

*3 Both “0” and “1” are allowed for “Reserved”.

*4 The initial setting after reset is required after power-on because change from the default value is needed. The second setting by communication is not needed unless power is off or the system is reset.

Setting Registers by Serial Communication

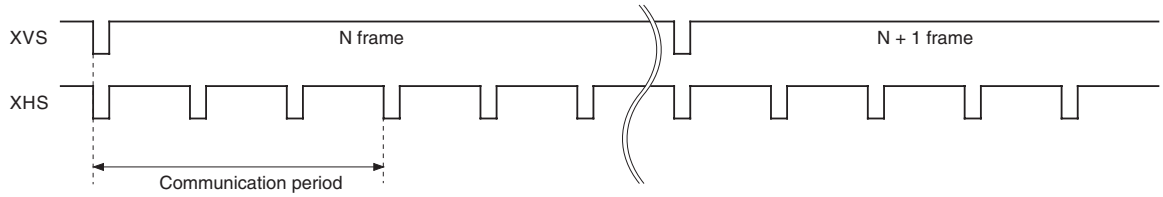
Description of Setting Registers

This sensor can write and read the setting values of the various registers shown in the Register Map by 3-wire serial communication. See “Register Map” for the addresses and setting values to be set. The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Type	Description
ChipID	81h: Register write 82h: Register read
Address	Sets the address according to the Register Map. When using a communication method that sets continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing

Perform register communication within the 3H period after the falling edge of XVS. Register setting values are reflected at the following timing. When communication is performed during the communication period shown in the figure below, items noted as (1) in the reflection timing column of the Register Map are output in the state with the setting value reflected in the N frame. However, note that while the storage time setting is reflected in the N frame, it is reflected to shutter control after N frame readout, so the setting value is reflected to the output in the N + 1 frame. Items that are reflected instantly are reflected at the timing when communication is performed.



Serial Communication and Reflection Timing

Register Write and Read

○ The communication procedure when writing registers is as follows.

1. Set XCE Low to enable the chip's communication function. Execute serial data input using SCK and SDI.
2. Transmit data synchronized with SCK 1 bit at a time from the LSB using SDI. Transfer SDI and TOUT synchronized with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input the Chip ID (81h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The register address is automatically incremented.
5. Input the data to the third and subsequent bytes. The data in the third byte is written to the register address set by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and the data is established in 8-bit units.
6. The register values starting from the register set by the second byte are output from the TOUT pin. The register values before the write operation are output. The actual register values are the input data.
7. Set XCE High to end communication.

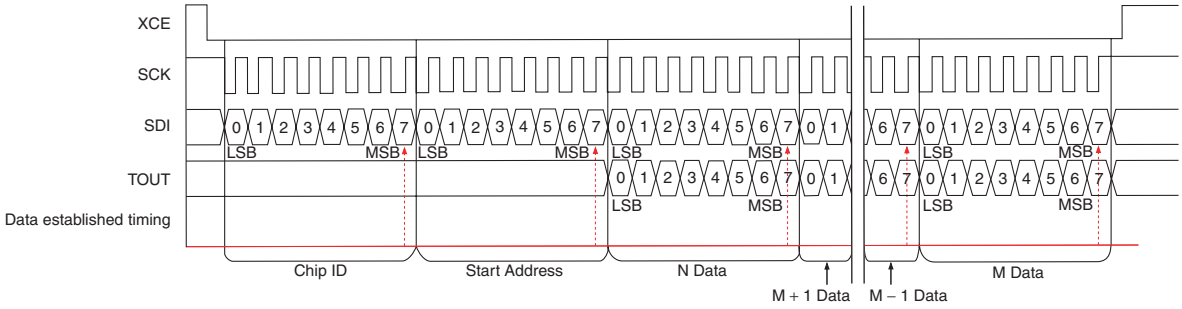
○ The communication procedure when reading registers is as follows.

1. Set XCE Low to enable the chip's communication function. Execute serial data input using SCK and SDI.
2. Transmit data synchronized with SCK 1 bit at a time from the LSB using SDI. Transfer SDI and TOUT synchronized with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
3. Input the Chip ID (82h) to the first byte. If the Chip ID differs, subsequent data is ignored.
4. Input the start address to the second byte. The register address is automatically incremented.
5. Input data to the third and subsequent bytes. Input dummy data (input SCK) in order to read the register. The dummy data is not written to the register. To read continuous data, input the necessary number of bytes of dummy data.
6. The register values starting from the register set by the second byte are output from the TOUT pin. The input data is not written, so the actual register values are output.
7. Set XCE High to end communication.

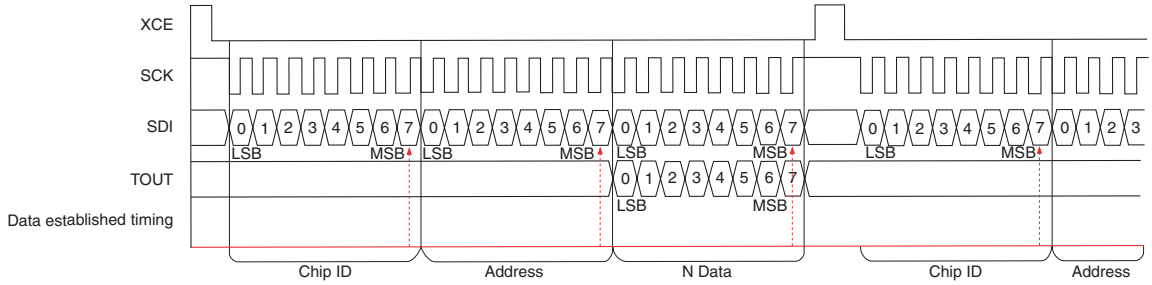
When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.

Note) Even when changing register setting values during imaging, communication should finish within the 3H communication period.

Communication Timing to Registers with Continuous Addresses



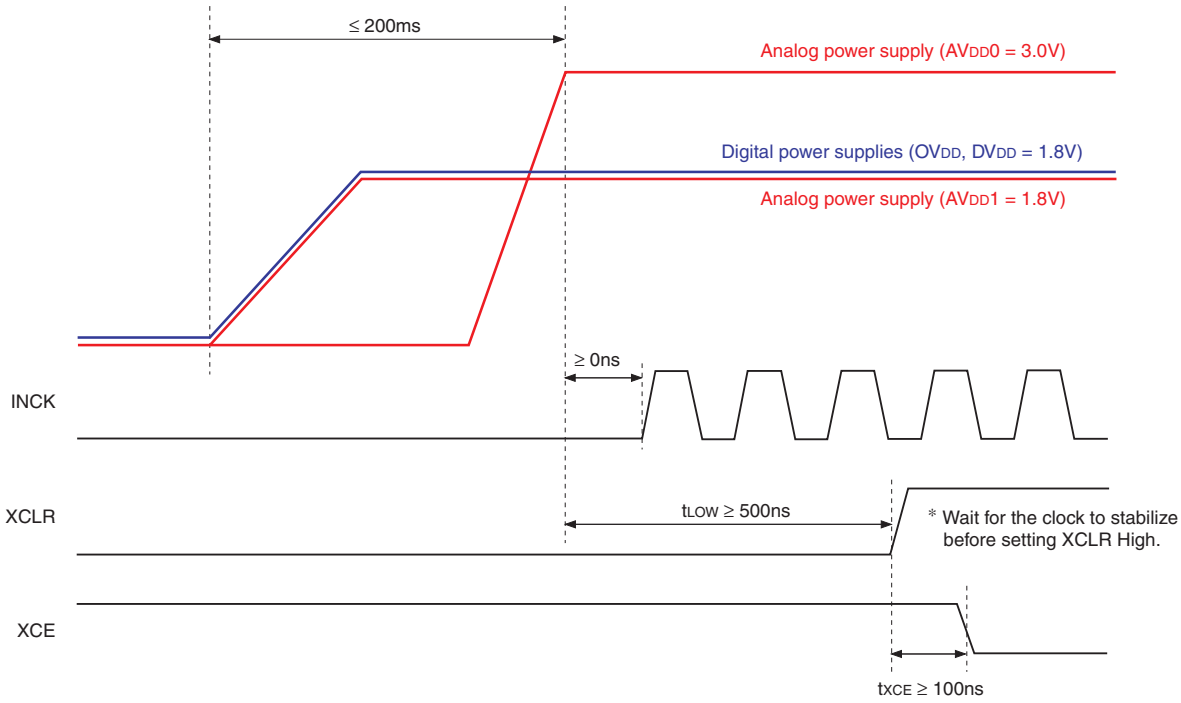
Communication Timing to Registers with Discontinuous Addresses



Power-on Sequence

Description of Operation during Power-on

Turn on the power supplies in the order so that the 1.8V power supplies (OV_{DD}, DV_{DD}, $AV_{DD}1$) rise before the 3.0V power supply ($AV_{DD}0$). In addition, all power supplies should finish rising within 200ms. Input the master clock (INCK) after the 1.8V and 3.0V power supplies have finished rising (OV_{DD}, DV_{DD}, $AV_{DD}1$ = 1.8V and $AV_{DD}0$ = 3.0V). The register values are undefined during power-on, so the system must be reset. Sensor system reset is performed by the XCLR pin. The register values after a reset are the default values. XCLR is asynchronous operation. A XCLR Low period (tLOW) of 500ns or more should be provided after all power supplies have risen. A system reset is applied by setting XCLR High after that. However, wait for the master clock to stabilize before applying the reset (before setting XCLR High). The standby mode must be canceled via communication to activate the sensor after a system reset is applied by setting XCLR High. A period (tXCE) of 100ns or more should be provided after setting XCLR High before inputting the communication enable signal XCE.



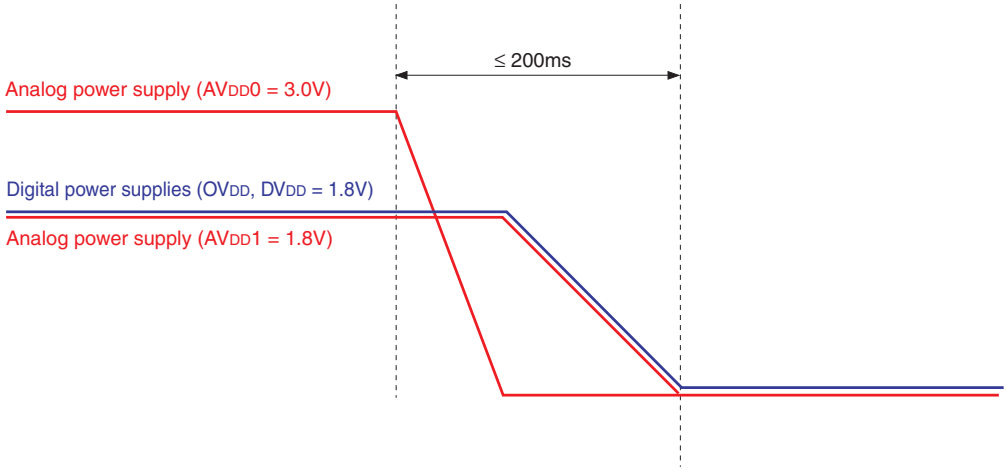
Power-on Sequence

Sequence from Standby Cancel to Stable Image Output

A period of approximately 500ns is required for power supply stabilization. After that, the system reset pulse must be canceled, the XVS and XHS pulses input, and then initialization processing must be performed for the sensor internal circuits. Up to 16 frames (max.) are required until a stable image is output.

Description of Operation during Power-off

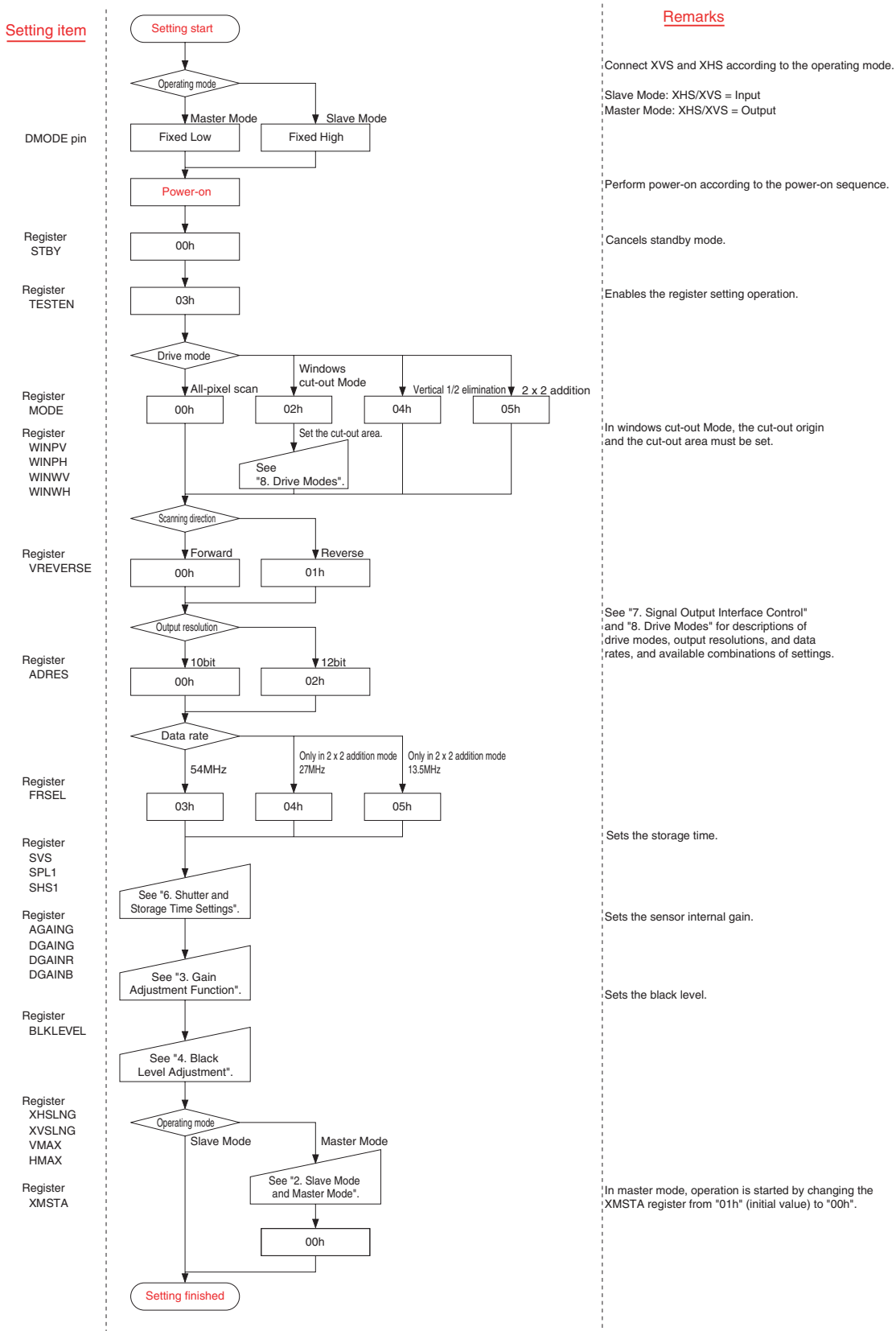
Turn off the 1.8V power supplies (OV_{DD}, DV_{DD}, $AV_{DD}1$) and the 3.0V power supply ($AV_{DD}0$) in the order so that the 3.0V power supply falls first. In addition, all power supplies should finish falling within 200ms. However, when an increase in the transient current of several tens of mA is allowed until power-off, the above sequence and time specifications are ignored, and sensor breakdown will not occur even in this case. After the 1.8V power supplies (OV_{DD}, DV_{DD}, $AV_{DD}1$) fall, set each digital input pin (INCK, XCE, SCK, SDI, XCLR, DMODE) and each I/O pin (XVS, XHS) to 0V or high impedance.



Power-off Sequence

Sensor Setting Flow Chart

The sensor initial setting flow chart is shown below. The initial settings must be made after the sensor is reset immediately following power-on. See the description of each operation in the “Remarks” column for the respective control methods.

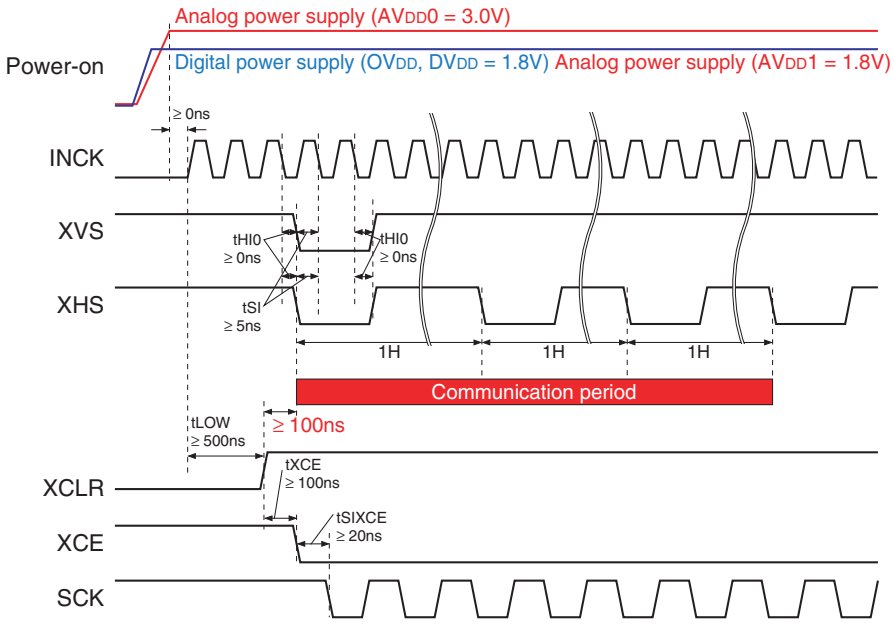


Serial communication period after sensor reset

Slave mode

Communication period is set at the time shown below for sensor initial setting immediately after power-on. In slave mode, vertical and horizontal sync signals (XVS/XHS) are valid only 100ns after fall after sensor reset (XCLR is Low). 3H of serial communication period is from the first XVS fall that becomes valid to the third XHS fall after XHS fall.

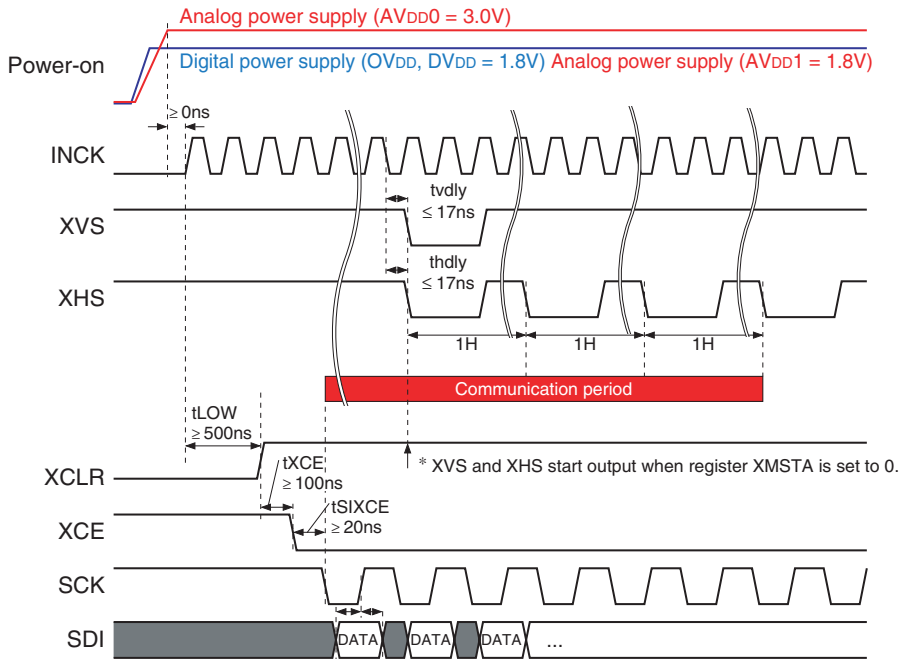
* XVS and XHS signals input when XCLR is Low are ignored. Sensor is in standby mode at that time until the next XVS signal. Register communication in standby mode is possible.



Initial setting timing in slave mode

Master mode

In master mode, initial values of register VMAX (address 7Ch [7:0], 7Dh [7:0]) and HMAX (address 7Eh [7:4], 7Fh [7:0]) are “0h”, so XVS and XHS are not output until the initial setting (register communication) is performed. XVS and XHS start output when master mode start register XMSTA (address 26h [0]) is set to “0” from “1” after registers VMAX and HMAX are set by serial communication at the initial setting. Register communication is possible during standby period until sensor outputs XVS and XHS.



Initial setting timing in master mode

Description of Operation

1. Standby Mode

Sensor operation is stopped and the sensor is set to the standby mode which reduces power consumption by setting the standby control register STBY (address: 00h [1:0]) to “03h”. (Standby mode is established immediately after a reset.) The serial communication function operates even in standby mode, so standby mode can be canceled by setting STBY to “00h”.

Table 1. Description of Standby Settings

STBY [1:0]	Mode	Status	
		Digital circuit	Analog circuit
00h (initial setting)	Normal operating mode	Active	Active
01h	Setting prohibited		
02h			
03h	Standby mode	Stopped	Stopped

2. Slave Mode and Master Mode

The sensor can be switched to slave mode or master mode. The DMODE pin (Pin A8) must be set to switch the mode. After the sensor is set to master mode, the register XMSTA (address: 26h [0]) must be set to “0” to start operation. In addition, when the sensor is operated in master mode, the generated sync signal count is set by the register VMAX (address: 7Ch [7:0], 7Dh [7:0]) for the number of lines in the vertical direction and the register HMAX (address: 7Eh [7:4], 7Fh [7:0]) for the number of clocks in the horizontal direction. Table 2 shows example setting values. For a detailed description of the drive modes, see “8. Drive Modes”.

Table 2. List of Slave and Master Mode Settings (Example: All-pixel Scan Mode)

Setting item	Register details			Setting value		Remarks
	Register	Address	bit	Slave Mode	Master Mode	
DMODE pin	—	—	—	Fixed High	Fixed Low	H: 1.8V L: GND
XMSTA	XMSTA	26h	[0]	N/A	1d: Stops operation (initial value) 0d: Starts operation	Operation in master mode is started by setting “0d”.
XHSLNG	XHSLNG [2:0]	53h	[3:1]	N/A	5h (initial value)	Sets the XHS width
XVSLNG	XVSLNG [2:0]	53h	[6:4]	N/A	6h (initial value)	Sets the XVS width
VMAX	VMAX [7:0]	7Ch	[7:0]	N/A	1082d	Sets the number of lines per frame
	VMAX [15:8]	7Dh	[7:0]			
HMAX	HMAX [3:0]	7Eh	[7:4]	N/A	1656d	Sets the number of clocks per line
	HMAX [11:4]	7Fh	[7:0]			

N/A: The setting is invalid. Fixing to the initial values is recommended in slave mode.

Register	Setting value							
	0h	1h	2h	3h	4h	5h	6h	7h
XHSLNG	1clock	2clock	3clock	4clock	5clock	6clock	7clock	N/A
XVSLNG	N/A	1H	2H	3H	4H	5H	6H	7H

1 clock is the INCK cycle. In addition, the 1H period reference is the number of clocks set by the register HMAX.

3. Gain Adjustment Function

The programmable gain control (PGC) in this device is composed of a 0dB to 18dB analog PGC (APGC) block and a 3-bit shift (6dB to 24dB, 12dB to 30dB, 18dB to 36dB) digital PGC (DPGC) block. See Table 5. for each register setting value.

Note) Linearity of the junction between analog PGC and digital PGC is not guaranteed.

Analog PGC

The analog gain (0dB to 18dB/0.3dB) of the pixels corresponding to each color (RGB) can be set by the analog gain setting register AGAING (address: 1Ch [7:0], 1Dh [4:0]).

Table 3. Analog PGC Registers

Setting item	Register details			Setting value	
	Register	Address	bit	Setting range	Setting prohibited range
AGAING	AGAING [7:0]	1Ch	[7:0]	0200h-1000h	0000h-01ffh 1001h-1fffh
	AGAING [12:8]	1Dh	[4:0]		

Digital PGC

The digital gain can be set by the digital gain setting registers DGAING (address: 1Eh [1:0]), DGAINR (address: 1Eh [3:2]), and DGAINB (address: 1Eh [5:4]). “00h” sets the minimum gain, and “03h” sets the maximum gain (Table 4). Increasing the register setting by 1 LSB bit-shifts the output signal by 1bit.

Table 4. Digital PGC Registers

Setting item	Register details			Setting value
	Register	Address	bit	
DGAING	DGAING [1:0]	1Eh	[1:0]	0h (initial setting): ×1 1h: ×2 2h: ×4 3h: ×8
DGAINR	DGAINR [1:0]	1Eh	[3:2]	
DGAINB	DGAINB [1:0]	1Eh	[5:4]	

Table 5. Register setting value - Gain value list

Total Gain [dB]				
AGAING [12:0] Setting value	DGAING/DGAINR/DGAINB			
	00h	01h	02h	03h
1000h	0.0	6.0	12.0	18.0
F74h	0.3	6.3	12.3	18.3
EEEh	0.6	6.6	12.6	18.6
E6Ch	0.9	6.9	12.9	18.9
DEFh	1.2	7.2	13.2	19.2
D76h	1.5	7.5	13.5	19.5
D01h	1.8	7.8	13.8	19.8
C90h	2.1	8.1	14.1	20.1
C23h	2.4	8.4	14.4	20.4
BB9h	2.7	8.7	14.7	20.7
B53h	3.0	9.0	15.0	21.0
AF1h	3.3	9.3	15.3	21.3
A92h	3.6	9.6	15.6	21.6
A36h	3.9	9.9	15.9	21.9
9DDh	4.2	10.2	16.2	22.2
987h	4.5	10.5	16.5	22.5
935h	4.8	10.8	16.8	22.8
8E4h	5.1	11.1	17.1	23.1
897h	5.4	11.4	17.4	23.4
84Dh	5.7	11.7	17.7	23.7
804h	6.0	12.0	18.0	24.0
7BFh	6.3	12.3	18.3	24.3
77Bh	6.6	12.6	18.6	24.6
73Ah	6.9	12.9	18.9	24.9
6FBh	7.2	13.2	19.2	25.2
6BFh	7.5	13.5	19.5	25.5
684h	7.8	13.8	19.8	25.8
64Bh	8.1	14.1	20.1	26.1
615h	8.4	14.4	20.4	26.4
5E0h	8.7	14.7	20.7	26.7

Total Gain [dB]				
AGAING [12:0] Setting value	DGAING/DGAINR/DGAINB			
	00h	01h	02h	03h
5ADh	9.0	15.0	21.0	27.0
57Bh	9.3	15.3	21.3	27.3
54Ch	9.6	15.6	21.6	27.6
51Eh	9.9	15.9	21.9	27.9
4F1h	10.2	16.2	22.2	28.2
4C6h	10.5	16.5	22.5	28.5
49Dh	10.8	16.8	22.8	28.8
475h	11.1	17.1	23.1	29.1
44Eh	11.4	17.4	23.4	29.4
429h	11.7	17.7	23.7	29.7
404h	12.0	18.0	24.0	30.0
3E1h	12.3	18.3	24.3	30.3
3C0h	12.6	18.6	24.6	30.6
39Fh	12.9	18.9	24.9	30.9
380h	13.2	19.2	25.2	31.2
361h	13.5	19.5	25.5	31.5
344h	13.8	19.8	25.8	31.8
327h	14.1	20.1	26.1	32.1
30Ch	14.4	20.4	26.4	32.4
2F1h	14.7	20.7	26.7	32.7
2D8h	15.0	21.0	27.0	33.0
2BFh	15.3	21.3	27.3	33.3
2A7h	15.6	21.6	27.6	33.6
290h	15.9	21.9	27.9	33.9
27Ah	16.2	22.2	28.2	34.2
264h	16.5	22.5	28.5	34.5
250h	16.8	22.8	28.8	34.8
23Bh	17.1	23.1	29.1	35.1
228h	17.4	23.4	29.4	35.4
215h	17.7	23.7	29.7	35.7
203h	18.0	24.0	30.0	36.0

4. Black Level Adjustment

A black level offset (offset variable range: 000h to 1FFh) can be added to the data, after superimposing the digital gain, by setting the register BLKLEVEL (address: 1Fh [7:0], 20h [0]). Increasing the BLKLEVEL setting by 1 increases the black level by 1LSB. * Recommended setting value: 03Ch (60d)

Table 6. Black Level Adjustment Register

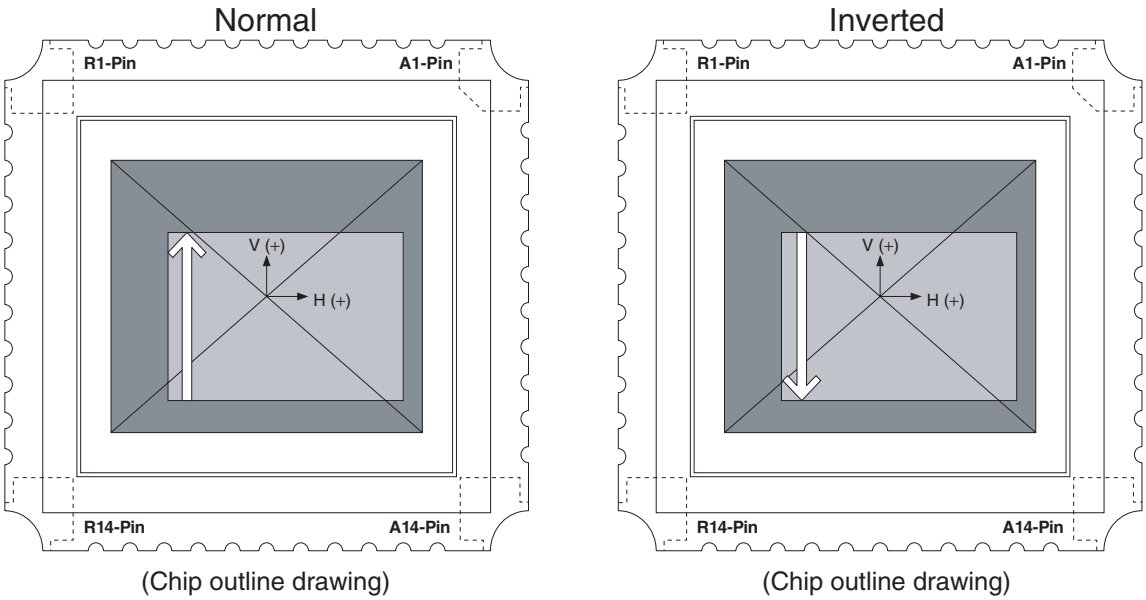
Setting item	Register details			Setting value
	Register	Address	bit	
BLKLEVEL	BLKLEVEL [7:0]	1Fh	[7:0]	000h to 1FFh
	BLKLEVEL [8]	20h	[0]	

5. Vertical Normal/Inverted Drive

The sensor vertical readout direction (normal/inverted) can be switched by setting the register VREVERSE (address: 01h [4]). See “8. Drive Modes” for the readout line order in normal mode and inverted mode. However, note that when normal/inverted switching is performed between frames, one invalid frame is generated in the readout immediately after the readout direction changes.

Table 7. Vertical Drive Direction Setting Register

Setting item	Register details		Setting value
	Address	bit	
VREVERSE	01h	[4]	0h: Normal (initial value) 1h: Inverted



(Chip outline drawing) (Chip outline drawing)

Fig. 1. Outline Drawing of Vertical Normal/Inverted Drive

6. Shutter and Storage Time Settings

This sensor has a variable electronic shutter function that can control the storage time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For storage time control, an image which reflects the setting is output from the frame after the setting changes.

6-1. Example Storage Time Setting

The sensor's storage time is obtained by Formula 2.

$$\text{Storage time} = (\text{1frame period}) \times (\text{SVS} + 1 - \text{SPL1}) - (\text{SHS1}) \times (\text{1H period}) - \delta$$

Formula 2. Storage Time Calculation Formula

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is set in 1H units, so the time is determined by (Number of lines × 1H period).

*2 See "8. Drive Modes" for the 1H period.

*3 δ is a fixed value that depends on the drive mode. Table 8 shows these values.
clk is the number of INCK clocks.

Table 8. List of δ Values

Drive mode	Output gradation	δ [clk]
All-pixel scan mode Windows cut-out Mode Vertical 1/2 elimination mode	10bit	209
	12bit	640
VGA addition mode	12bit	209

In this item, the shutter operation and storage time with the time sequence on the horizontal axis and the vertical address on the vertical axis are shown as the figure below. For simplification, readout operation is noted in line units.

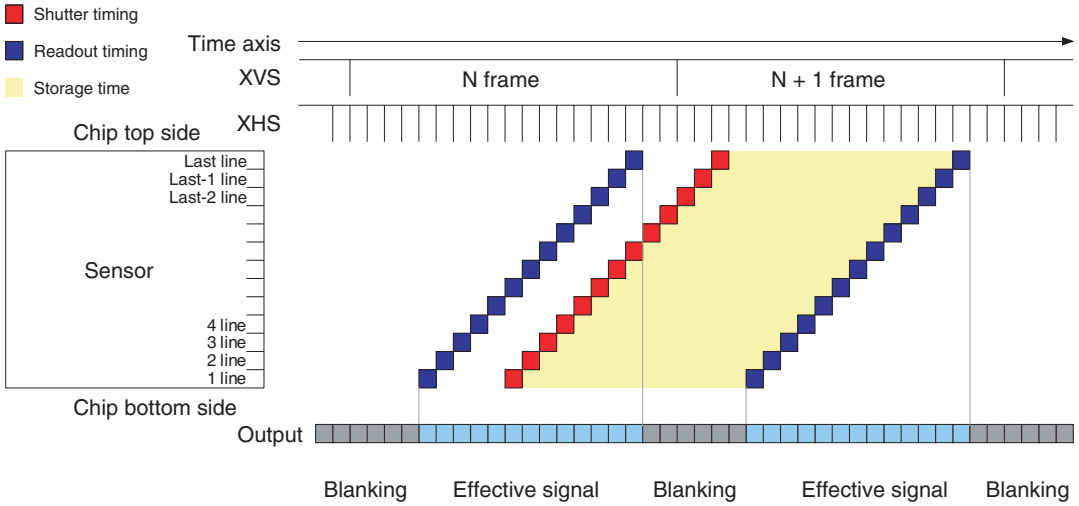


Image Drawing of Shutter Operation

6-2. Normal Exposure Operation (Controlling the Storage Time in 1H Units)

The storage time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the storage time is controlled by the register SHS1 (address: 08h [7:0], 09h [7:0]).

- ◆ Set SHS1 to a value between 0 and (Number of lines per frame – 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the register VMAX (address: 7Ch [7:0], 7Dh [7:0]).
- ◆ The number of lines per frame differs according to the drive mode.

Table 9. Registers Used to Set the Storage Time in 1H Units

Setting item	Register details			Description
	Register	Address	bit	
SHS1	SHS1 [7:0]	08h	[7:0]	Sets the shutter sweep time 0001h to (VMAX setting value – 1)
	SHS1 [15:8]	09h	[7:0]	
VMAX	VMAX [7:0]	7Ch	[7:0]	Sets the number of lines per frame (Only in master mode) See “8. Drive Modes” for the setting value in each mode.
	VMAX [15:8]	7Dh	[7:0]	

For storage time control, an image which reflects the setting is output from one frame after the frame in which the setting changes.

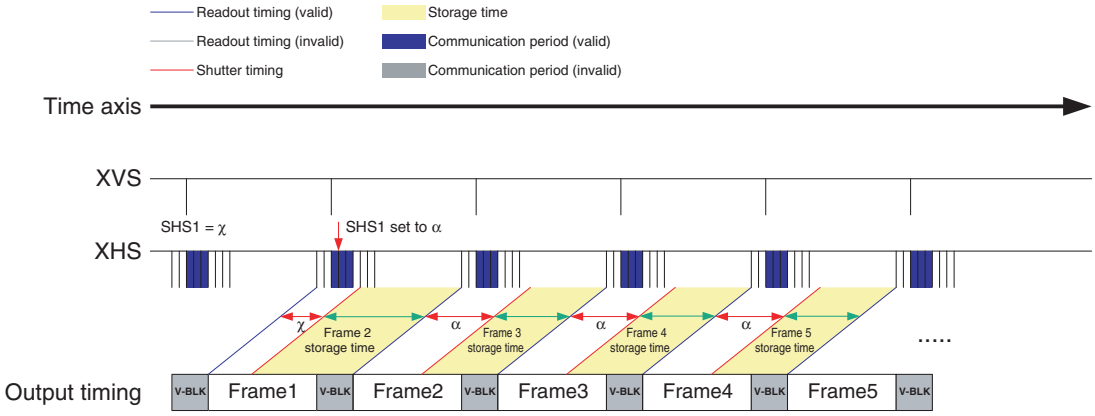


Image Drawing of Storage Time Control within a Frame

6-3. Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long storage operation can be performed by lengthening the frame period. When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval. When the sensor is operating in master mode, it is done by setting a larger register VMAX (address: 7Ch [7:0], 7Dh [7:0]) value compared to normal operation.
Likewise, in slave mode the storage time can be increased by lengthening the input XVS signal pulse interval. When the storage time is extended by increasing the number of lines, the rear blanking increases by an equivalent amount.

- ◆ The maximum VMAX and SHS1 values are 65535d. When the number of lines per frame is set to the maximum value, the storage time in all-pixel scan mode at 30fps is approximately 2s.
- ◆ The imaging characteristics are not guaranteed during long exposure operation.

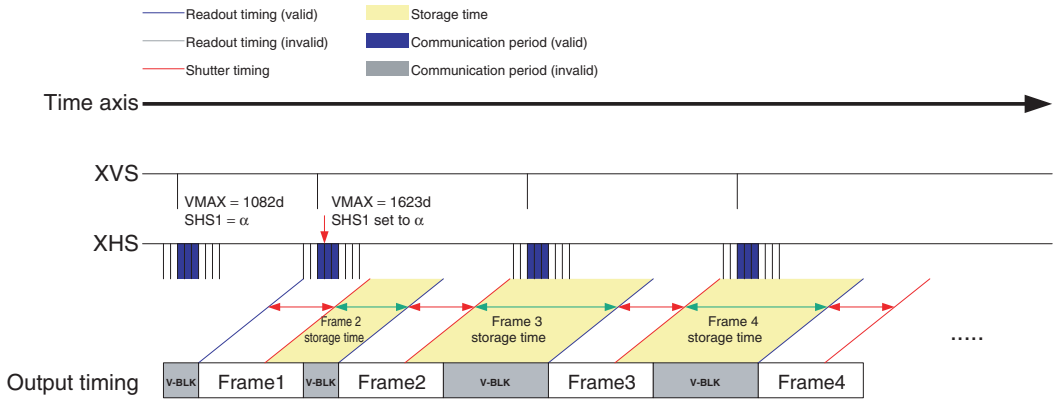


Image Drawing of Long Storage Time Control by Adjusting the 1H Period

6-4. Long Exposure Operation (Controlling the Storage Time in Frame Units)

When setting a long exposure that extends the storage time to one frame or more, set the register SVS (address: 06h [7:0], 07h [1:0]) to the value of the number of storage frames – 1. In addition, the frame in which the shutter operates is set by the register SPL1 (address: 12h [7:0], 13h [1:0]). To further adjust the storage time in 1H units within the frame set by SPL1, set the register SHS1. However, note that performing long storage causes the readout timing and the setting reflection timing to be eliminated according to the value set by SVS, so the frame rate drops. The blanking signal is output in data corresponding to the drop in the frame rate.

- ◆ This description is for the settings in master mode. In slave mode, long storage is set by eliminating the input vertical sync signal (XVS) pulse.
- ◆ When set so that SVS < SPL1, the SPL1 setting value is ignored, and the signal is stored for the number of frames set by SVS.
- ◆ Set SHS1 to a value between 0 and (Number of lines per frame – 1)
- ◆ During long exposure operation, register communication is also reflected at the eliminated timing. To forcibly end operation partway, use the shutter break function.
- ◆ The imaging characteristics are not guaranteed during long exposure operation.

Table 10. Registers Used to Set the Storage Time in Frame Units

Setting item	Register details			Description
	Register	Address	bit	
SSBRK	SSBRK	05h	[0]	Shutter break function
SVS	SVS [7:0]	06h	[7:0]	Sets the number of storage frames
	SVS [9:8]	07h	[1:0]	
SPL1	SPL1 [7:0]	12h	[7:0]	Sets the number of sweep frames
	SPL1 [9:8]	13h	[1:0]	

Storage time control is reflected to the next readout frame to the set frame.

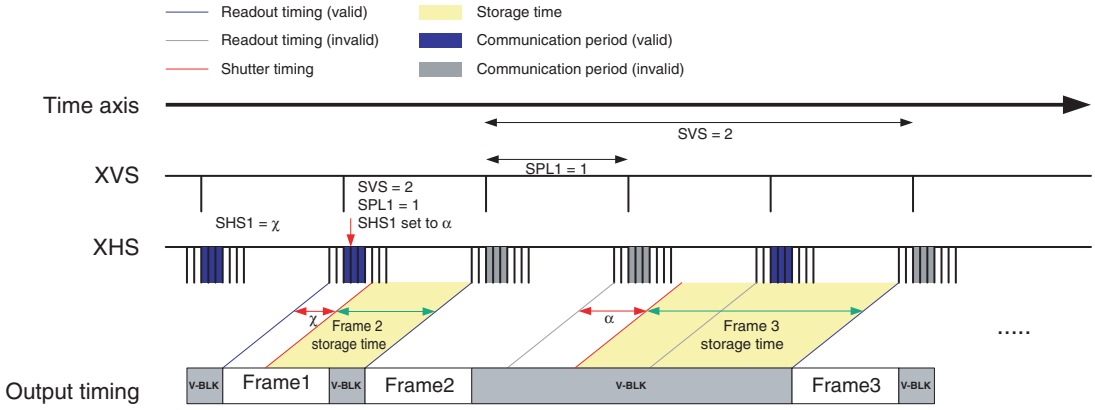


Image Drawing of Long Exposure Control in Frame Units

Shutter Break Function

When changing the storage time setting before the next reflection timing during long storage operation, the setting can be reflected at the normal XVS timing (when the register SVS is set to “0h”) by setting the register SSBRK (address: 05h [0]) to “01h”. The timing at which the register SSBRK is reflected conforms to the frame sequence before SVS is set.

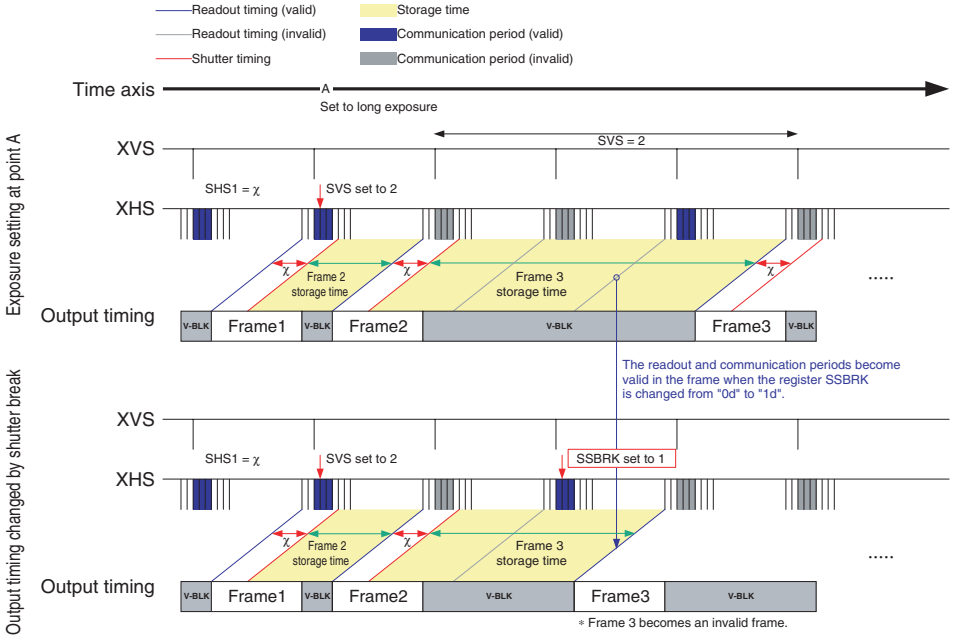


Image Drawing of Shutter Break Function

Depending on the value set when long storage operation starts (point “A” on the time axis), the scheduled output can be stopped partway and settings can be changed as shown in the figure above. In this case, readout occurs in the frame when the register SSBRK is transmitted, and the signal stored up to that point is output. At this time the signal output in the frame when SSBRK is set becomes an invalid signal.

The communication period of the frame in which SSBRK is set to “1d” becomes a valid period during which register transmission can be performed, but this valid period is only the frame during which the register SSBRK changes from “0d” to “1d”. Therefore, when returning to normal exposure after stopping long storage, the registers SVS and SPL1 must both be returned to “0d”. In addition, returning the register SSBRK to “0d” is recommended.

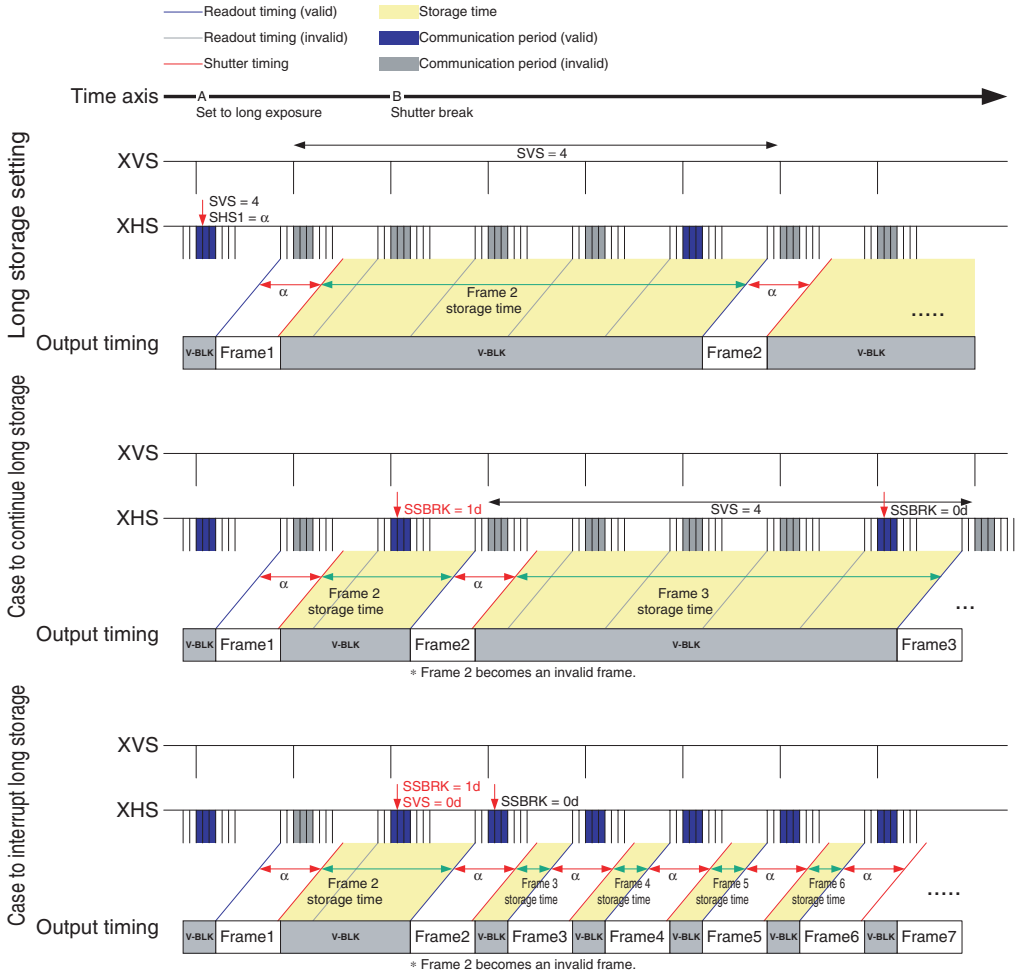


Image Drawing Showing Application of Shutter Break Function

7. Signal Output Interface Control

7-1. Output Signal Range

The output gradation of this sensor can be switched to 10 bits or 12 bits. However, the output gradation is fixed for some drive modes.

Table 11. Output Gradation Setting Register

Setting item	Register details		Output gradation	
	Address	bit	10bit	12bit
ADRES	03h	[1:0]	0	2

When set to 10-bit gradation, the unused ports (DOA [1:0]/DOB [1:0]) are fixed to “0”.

Table 12. Bit Assign per Output Gradation

DO pin	Output bit assign	
	10bit	12bit
DOA [11]	DO [9]	DO [11]
DOA [10]	DO [8]	DO [10]
DOA [9]	DO [7]	DO [9]
DOA [8]	DO [6]	DO [8]
DOA [7]	DO [5]	DO [7]
DOA [6]	DO [4]	DO [6]
DOA [5]	DO [3]	DO [5]
DOA [4]	DO [2]	DO [4]
DOA [3]	DO [1]	DO [3]
DOA [2]	DO [0]	DO [2]
DOA [1]	Fixed to “0”	DO [1]
DOA [0]	Fixed to “0”	DO [0]

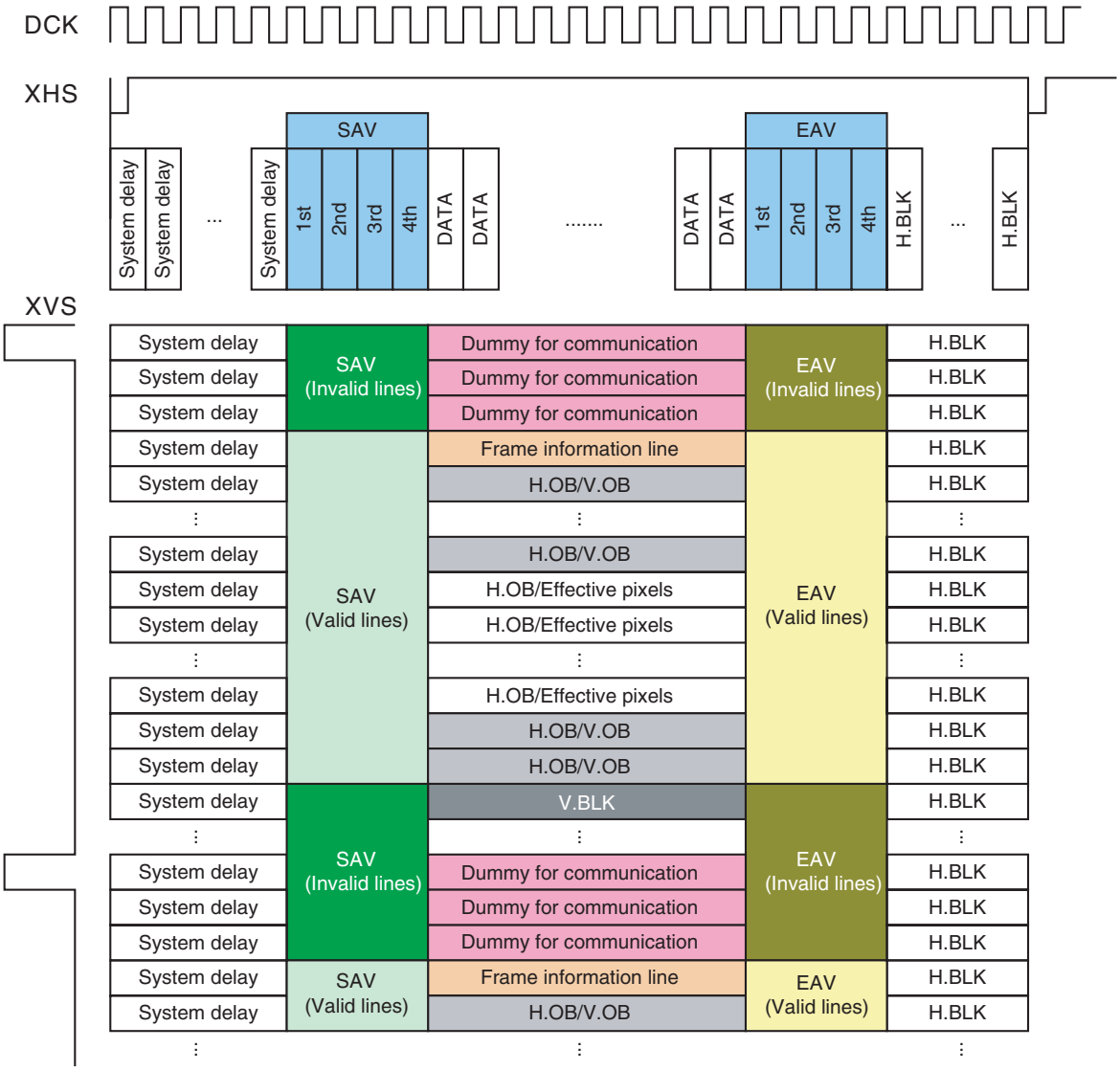
Table 13. Output Range

Output gradation	Output range	
	Min.	Max.
10-bit	000h	3FEh
12-bit	000h	FFEh

Upper limit of the maximum value is set for 10-bit/12-bit sensor output. Sensor signal shows the maximum value when output bit is all High-1 (12-bit: FFEh, 10-bit: 3FEh).

7-2. Sync Codes

Sync codes are attached and output immediately before and immediately after “Dummy signal + OPB signal + Effective pixel data” is output. The figure below shows the output timing. The sync codes are output in the order of 1st, 2nd, 3rd, 4th, and the output values are fixed from 1st to 3rd. (BLK = blanking period)



Sync code	1st code		2nd code		3rd code		4th code	
	10bit	12bit	10bit	12bit	10bit	12bit	10bit	12bit
SAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV (Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV (Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

Sync Code Output Timing

7-3. System Delay

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal.

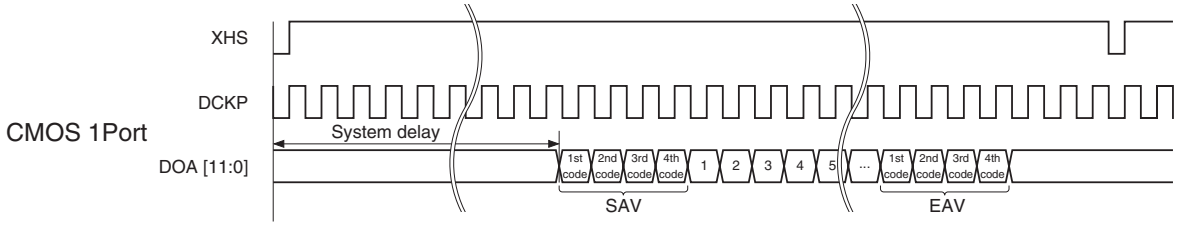


Fig. 2. System Delay

Table 14. List of System Delay for Each Drive Mode

Drive mode	Frame rate [fps]	Data rate [Mpix/s]	System delay [pixels]
All-pixel scan	30.14	54	172
2 × 2 addition readout	30.12	13.5	69
	60.23	27	91
Windows cut-out Mode	60.32	54	172
Vertical 1/2 elimination	60.23	54	172

8. Drive Modes

The table below lists the operating modes available with this sensor. All of the modes in the table below support vertical inverted drive. The initial setting after power-on is all-pixel scan, 30fps, 10 bits.

Table 15. List of Clock Setting Value for Each Drive Mode

Drive mode	Imaging conditions							
	Frame rate [fps]	Data rate [Mpix/s]	Output resolution [bit]	Number of effective pixels		Data width *1		1H period [μs]
				H [pixels]	V [pixels]	H [INCK]	V [line]	
All-pixel scan	30.14	54	10/12	1329	1049	1656	1082	30.67
2 × 2 addition readout	30.12	13.5	12	664	524	3296	544	61.04
	60.23	27	12			1648		30.52
Windows cut-out Mode	60.32	54	10/12	404 (min) to 692 (max)	313 (min) to 505 (max)	1664	538	30.81
Vertical 1/2 elimination	60.23	54	10/12	1329	524	1648	544	30.52

*1 The data width indicates the output sync signal period in master mode.
In slave mode the data width is the input XVS and XHS clock interval.

Table 16. List of Register Setting Value for Each Drive Mode

Drive mode	Imaging conditions			Register setting		
	Frame rate [fps]	Data rate [Mpix/s]	Output resolution [bit]	MODE	ADRES	FRSEL
All-pixel scan	30.14	54	10/12	0h (initial value)	0h/2h	3h: (initial value)
2 × 2 addition readout	30.12	13.5	12	5h	0h *1	5h
	60.23	27	12		0h *1	4h
Windows cut-out Mode	60.32	54	10/12	2h	0h/2h	3h: (initial value)
Vertical 1/2 elimination	60.23	54	10/12	4h	0h/2h	3h: (initial value)

*1 Register address setting should be 10-bit output: 0h, 12-bit output: 2h. However, perform 10-bit setting in 2 × 2 addition mode. 12-bit output is performed after performing 10-bit A/D conversion of pixel signal and 4-pixel digital addition.

* When register values are set to the combination other than the table above, it may cause the malfunction.

8-1. All-Pixel Scan Mode

All pixel signals of sensor are readout.

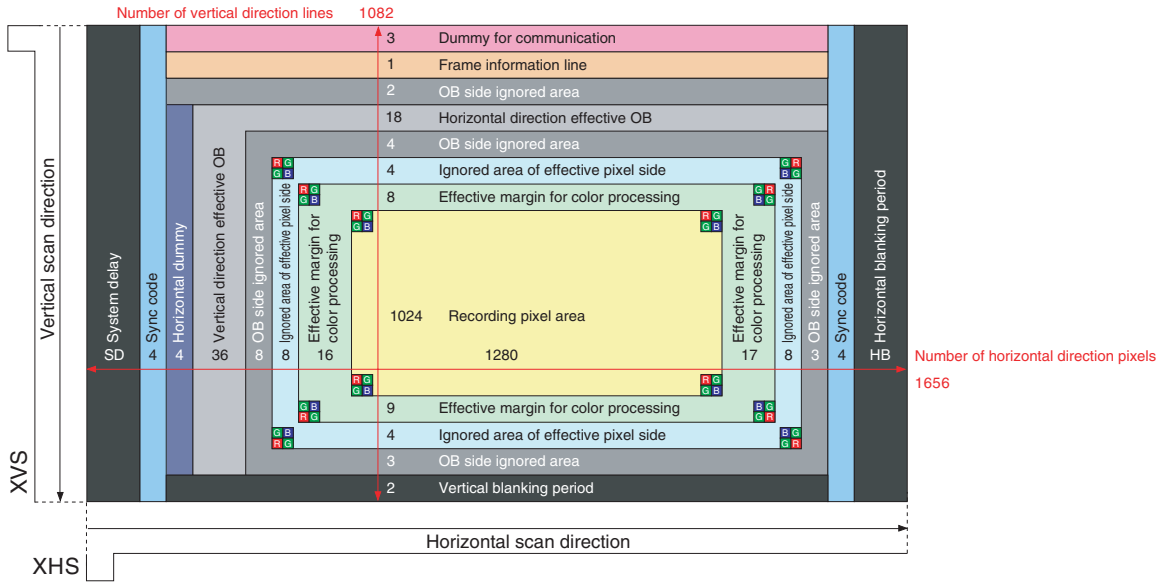


Fig. 3. Pixel Array Image Drawing in All-pixel Scan Mode

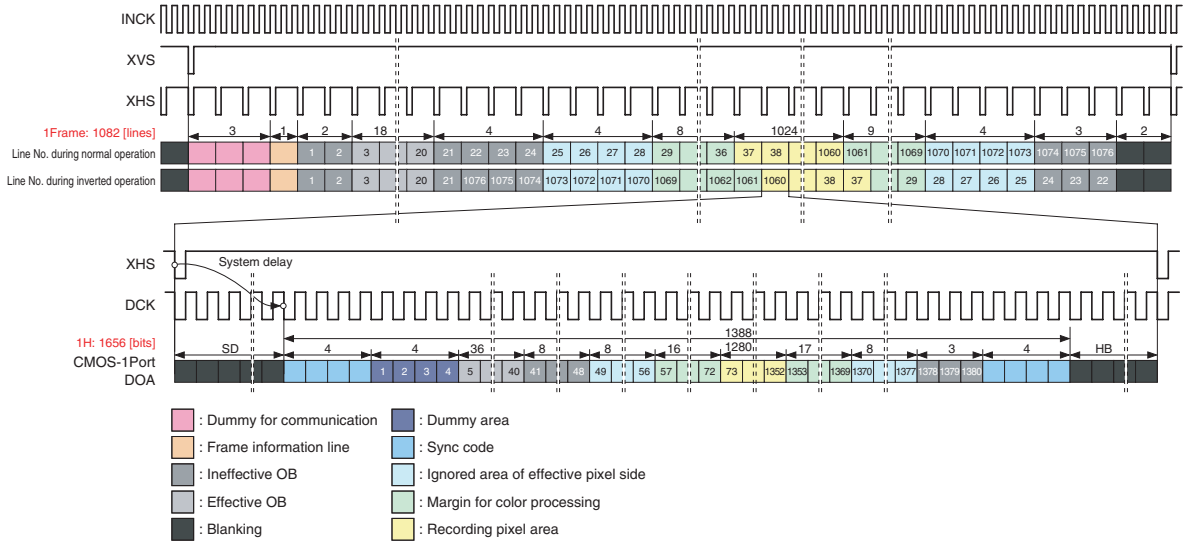


Fig. 4. Drive Timing Chart in All-pixel Scan Mode

8-2. 2 × 2 Addition Readout Mode

Sensor signal is readout by addition of vertical 2 pixels and horizontal 2 pixels.

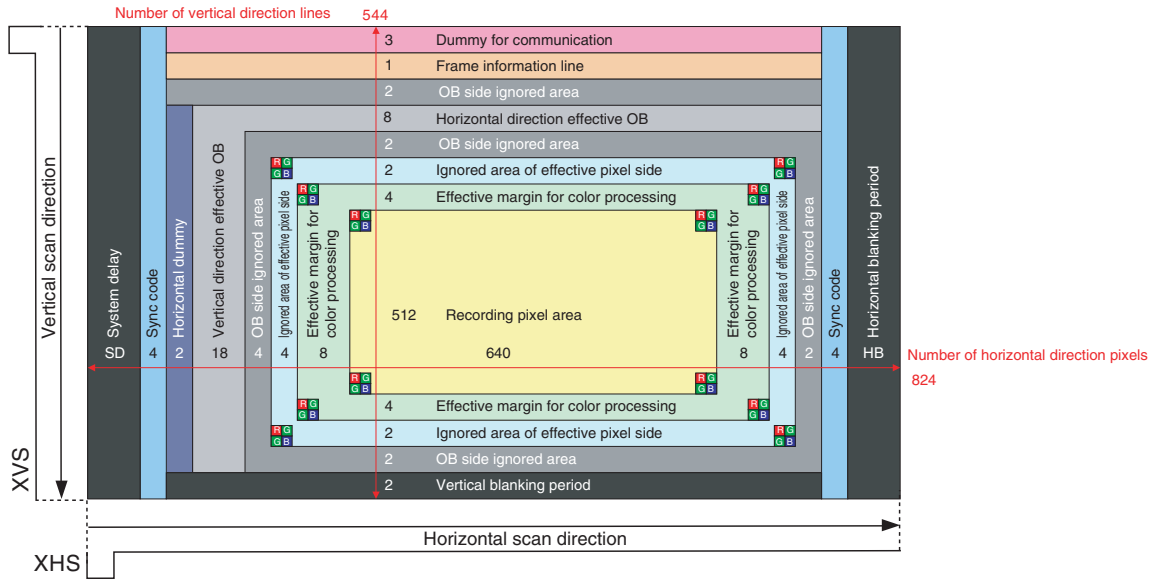


Fig. 5. Pixel Array Image Drawing in 2 × 2 Addition Readout Mode

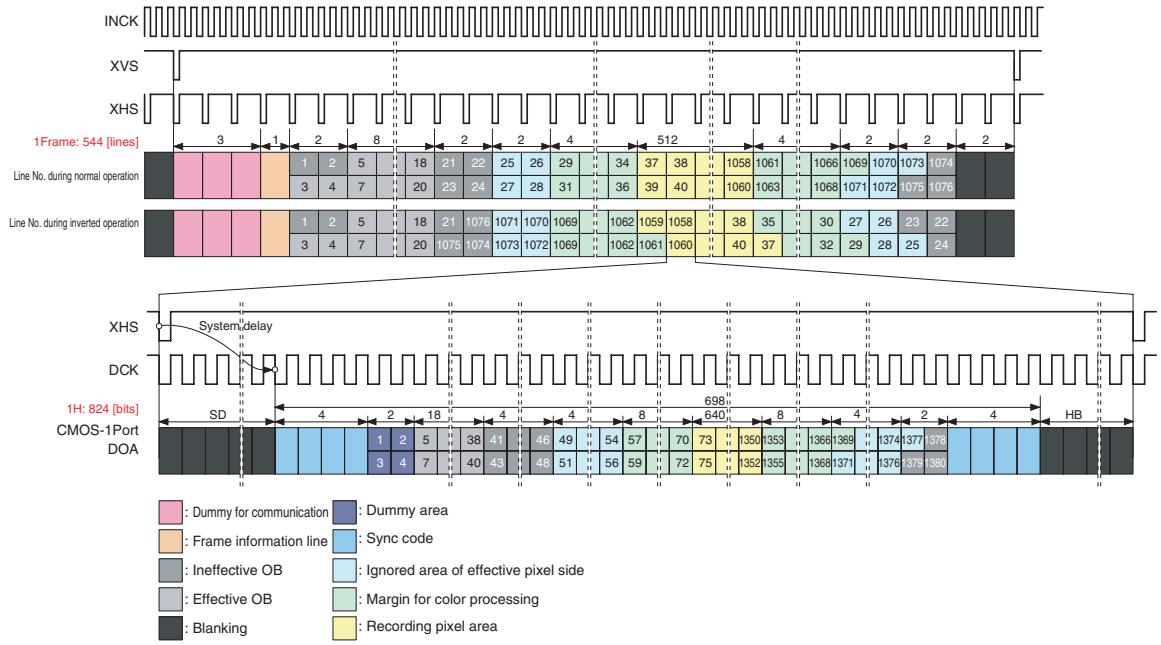


Fig. 6. Drive Timing Chart in 2 × 2 Addition Readout Mode

8-3. Windows Cut-out Mode

Sensor signals are cut-out and readout in arbitrary positions.
Fix and use the cut-out position and the size of window.
When changing the size or the position, set it via all-pixel scan mode.

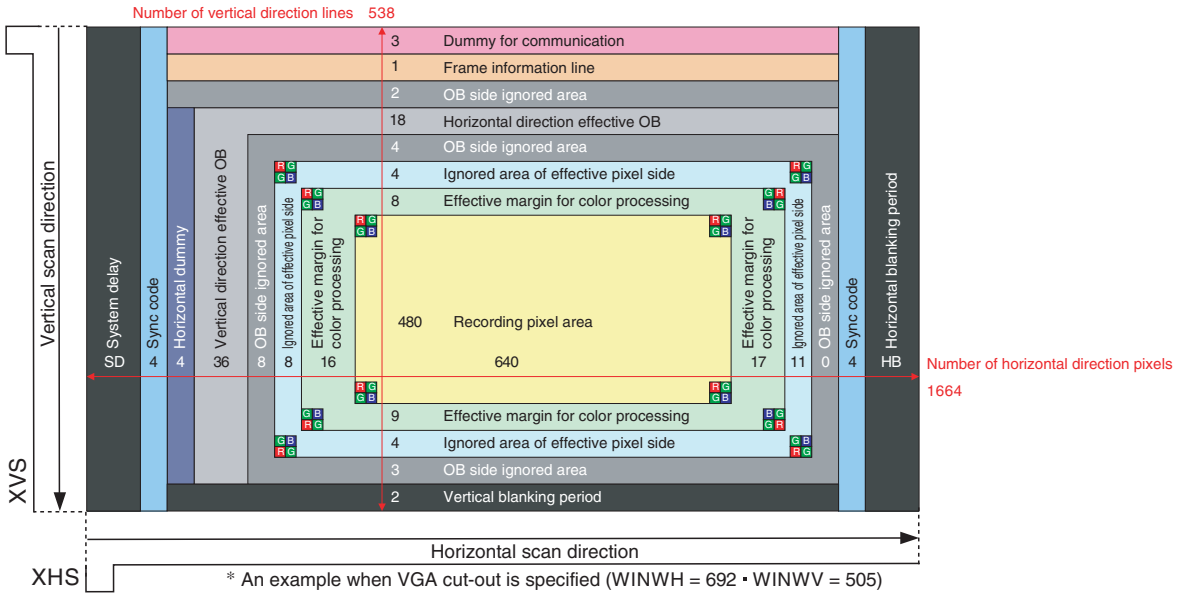


Fig. 7. Pixel Array Image Drawing in Windows Cut-out Mode

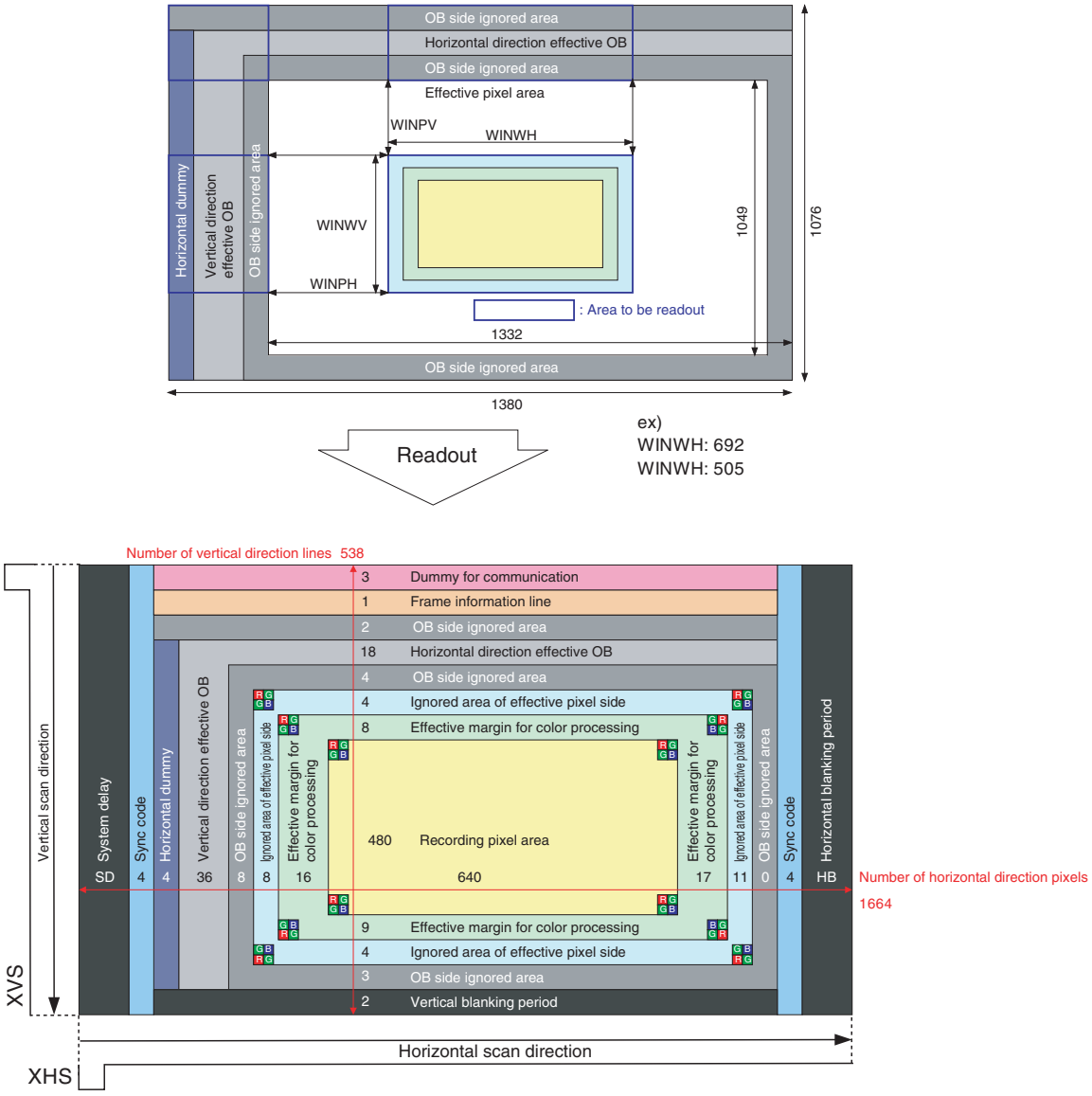


Fig. 8. Readout image drawing in windows Cut-out mode

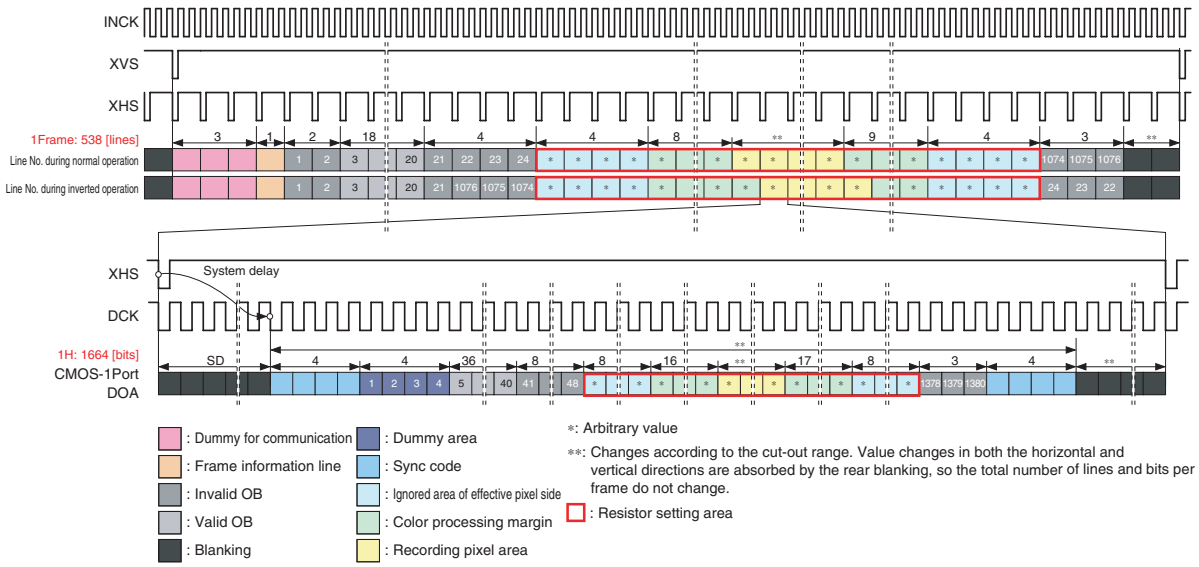


Fig. 9. Drive Timing Chart in Windows Cut-out Mode

Table 17. Window Cut-out Setting Registers

Setting item	Register details			Setting value		Description
	Register	Address	bit	min	max	
WINPH	WINPH [7:0]	16h	[7:0]	0h	3A3h *1	Sets the cut-out start address (horizontal coordinate)
	WINPH [10:8]	17h	[2:0]			
WINPV	WINPV [3:0]	17h	[7:4]	0h	2E0h *1	Sets the cut-out start address (vertical coordinate)
	WINPV [10:4]	18h	[6:0]			
WINWH	WINWH [7:0]	19h	[7:0]	194h	2B4h	Sets the cut-out width
	WINWH [10:8]	1Ah	[2:0]			
WINWV	WINWV [3:0]	1Ah	[7:4]	139h	1F9h	Sets the cut-out height
	WINWV [10:4]	1Bh	[6:0]			

*1 The cut-out start address maximum values differ according to the cut-out area size.

Restrictions on Register Settings

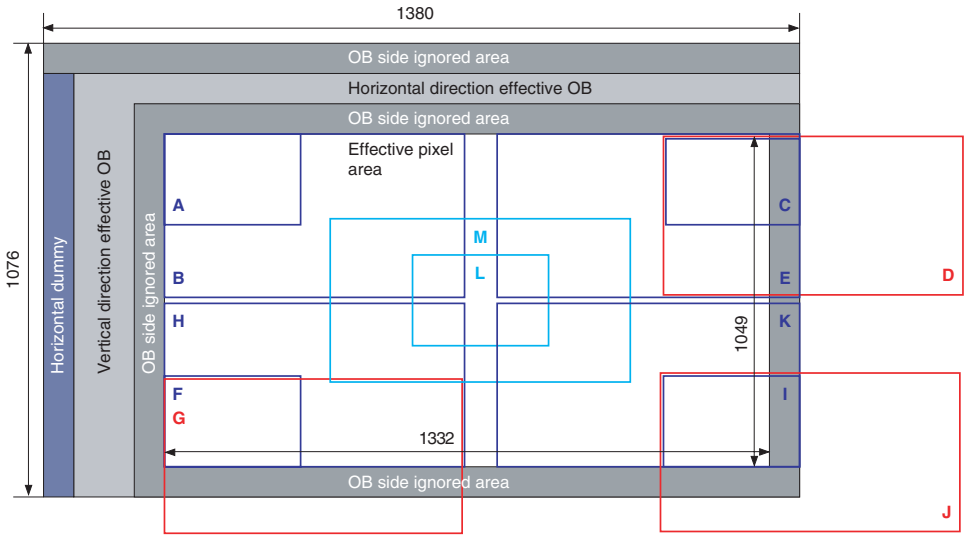
◆ The window start address and area settings should satisfy the following conditions:
WINPH ≥ 0h
WINPV ≥ 0h
WINWH + WINPH ≤ 534h
WINWH + WINPV ≤ 419h

◆ Set the window start address and area settings for the horizontal direction in 4-pixel units. There are no restrictions on the vertical direction as long as the shape satisfies the above conditions.

◆ When the right side (horizontal rear side) of the imaging area is set, the OPB level is output in the effective pixel side ignored area.

Table 18. List of Example Cut-out Area Settings

Cut-out origin settings		Cut-out range settings		Recommended number of recording pixels		Setting allowed	OB output	Position in the figure below
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical			
WINPH	WINPV	WINWH	WINWV					
0	0	404	313	352	288	○	None	A
0	0	692	505	640	480	○	None	B
931	0	404	313	352	288	○	Present	C
931	0	692	505	640	480	×	—	D
643	0	692	505	640	480	○	Present	E
0	736	404	313	352	288	○	None	F
0	736	692	505	640	480	×	—	G
0	544	692	505	640	480	○	None	H
931	736	404	313	352	288	○	Present	I
931	736	692	505	640	480	×	—	J
643	544	692	505	640	480	○	Present	K
467	461	404	313	352	288	○	None	L
323	317	692	505	640	480	○	None	M

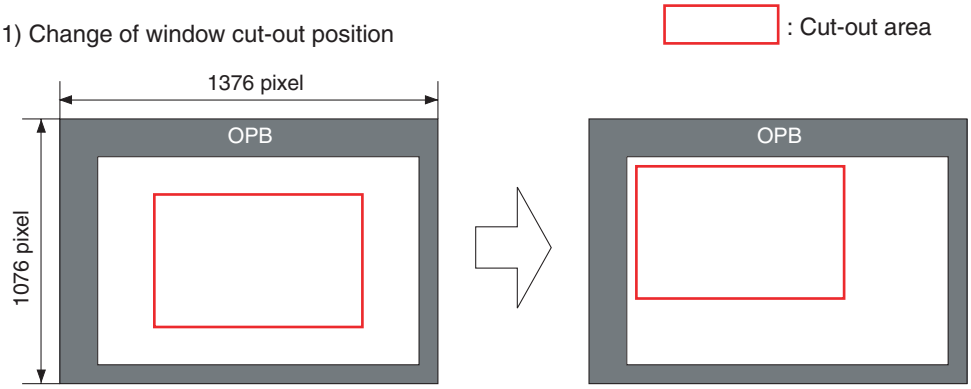


The areas indicated in the figure above show the actual readout areas, and include the color processing margin and the effective pixel side ignored area. The blue areas show examples of allowed settings, and the red areas show examples of prohibited settings.

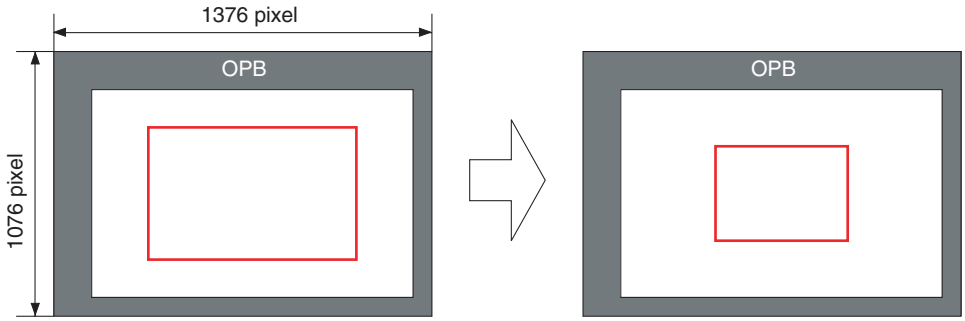
Notes on Window Cut-out Mode

This mode is not optimum for functions such as cut-out angle of view freely and changing window size seamlessly (e-PTZ, etc.). When changing window cut-out setting as shown below, 2 invalid frames occur during transition.

1) Change of window cut-out position



2) Change of window cut-out size



Invalid frame occurs in transition frame regardless of large to small and small to large size.

8-4. Vertical 1/2 Elimination Readout Mode

Sensor signal is readout eliminating lines in vertical direction.

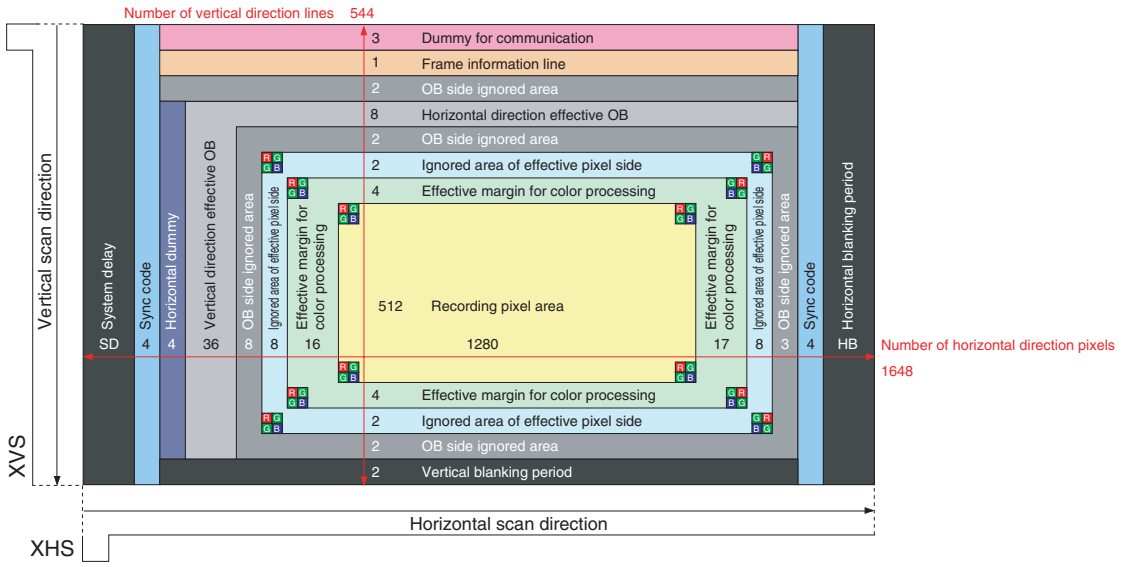


Fig. 10. Pixel Array Image Drawing in Vertical 1/2 Elimination Readout Mode

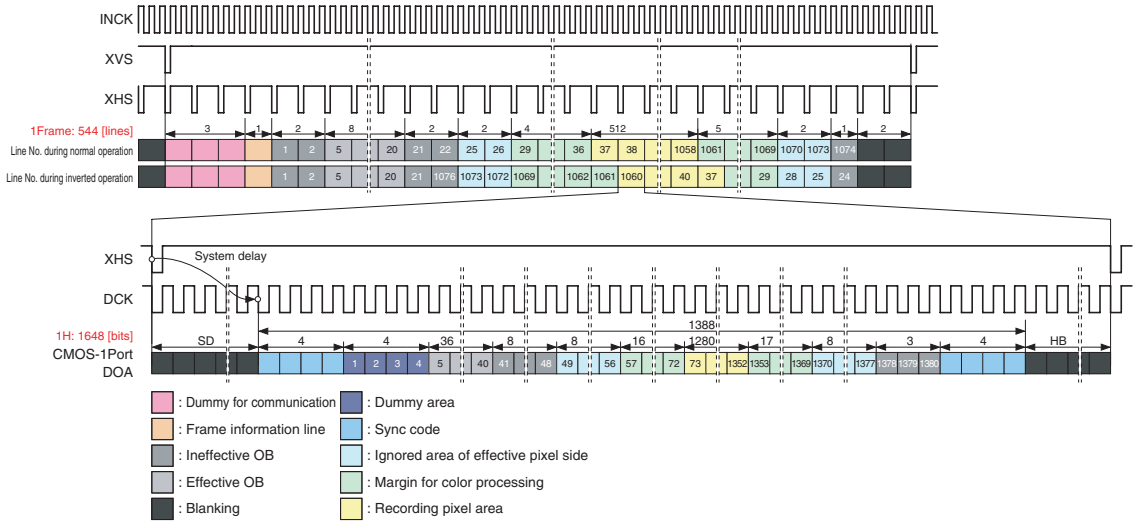


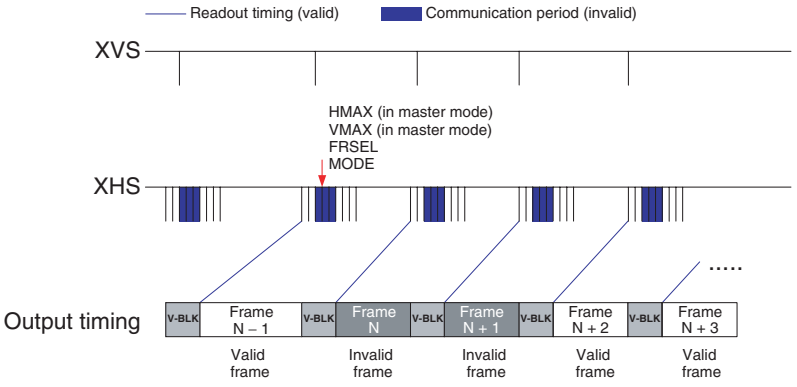
Fig. 11. Drive Timing Chart in Vertical 1/2 Elimination Readout Mode

9. Mode Transitions

When changing between the various drive modes, first set the sensor to the all-pixel scan mode, and then set it again to the desired drive mode. The table below shows the number of invalid frames generated by transition between the various modes. Invalid frames are output from sensor. But the output values may not be proportional to storage time or may not be even on the screen or an image partially saturated may output.

Table 19. Number of Invalid Frames Generated during Mode Transitions

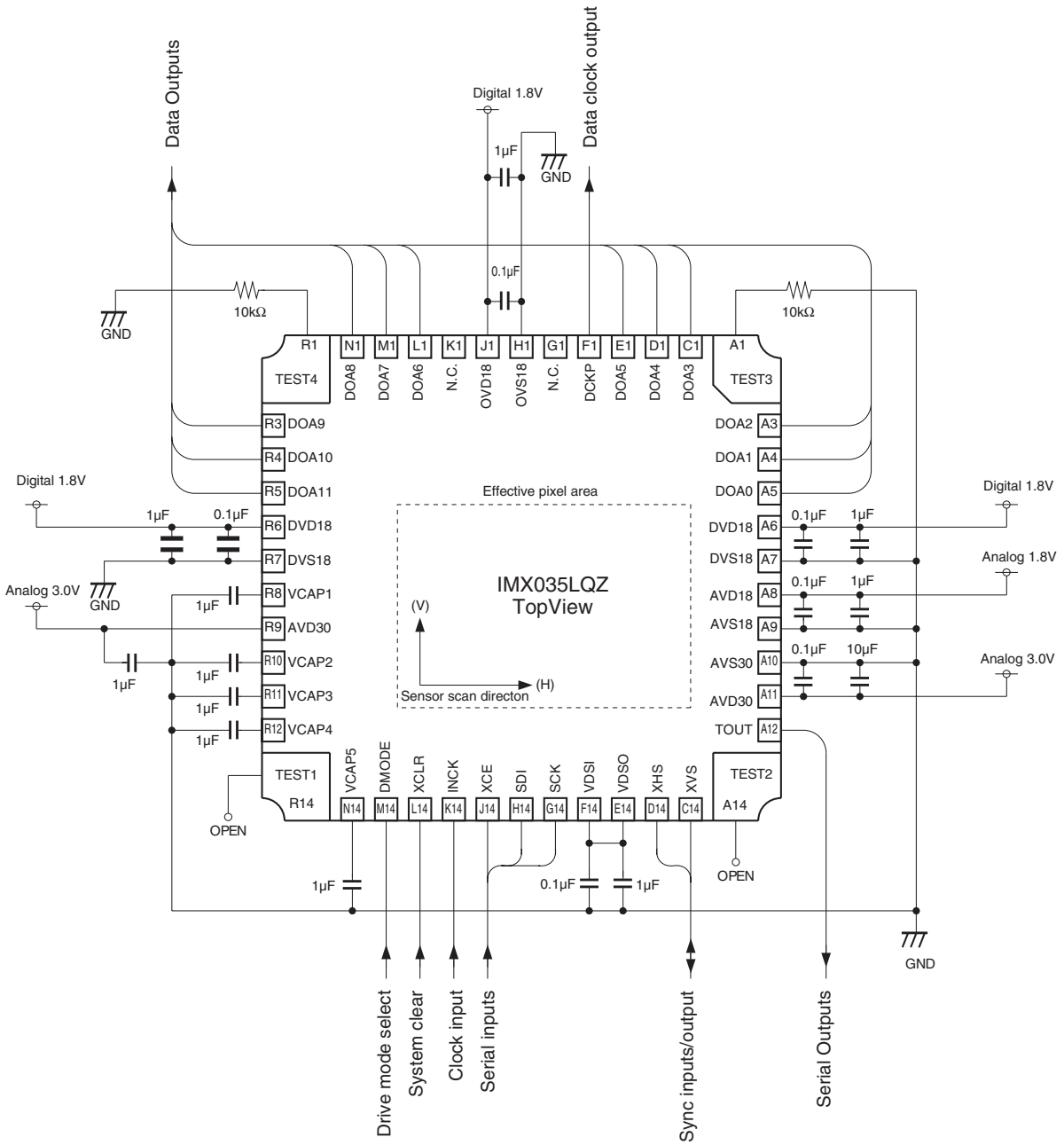
Mode transition	Number of invalid frames
All-pixel scan mode → 2 × 2 addition mode	2
All-pixel scan mode → Window cut-out mode	
All-pixel scan mode → Vertical 1/2 elimination mode	
2 × 2 addition mode → All-pixel scan mode	
Window cut-out mode → All-pixel scan mode	
Vertical 1/2 elimination mode → All-pixel scan mode	



* When a frame period is changed by changing the drive mode, the number of invalid frames is counted using a frame period after the change.

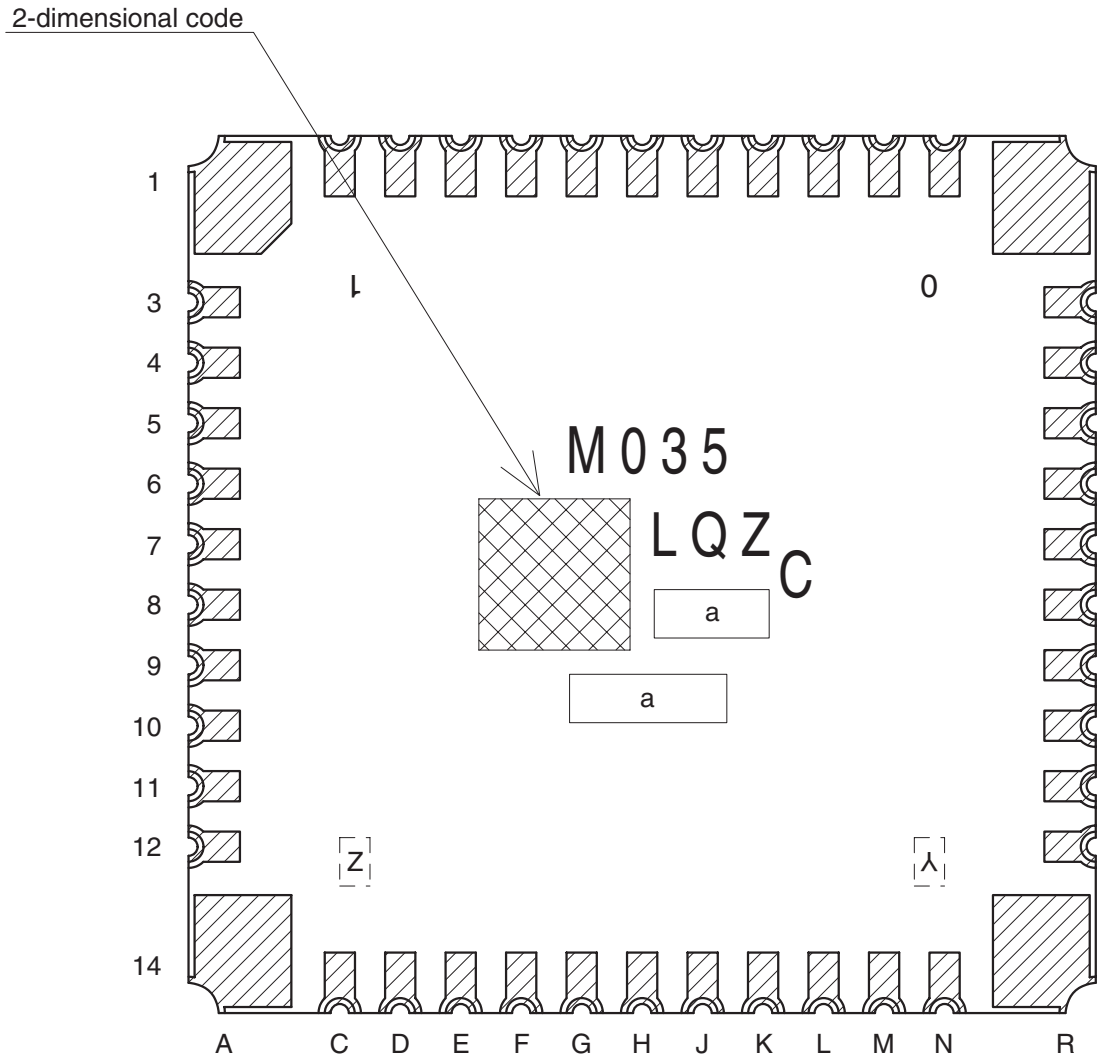
Fig. 12. Invalid Frame Generation Timing

Application Circuit

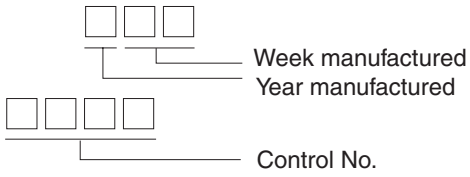


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Marking



a : Lot No. (Max.7)



Note : Following characters enter into Y to Z. (No plating)

Y : In English upper case character, One character.
Z : Number, single number.

Notes On Handling

1. Static charge prevention
   Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)
   (1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (2) The adhesive may cause the marking on the rear surface to disappear.
   (3) If metal, etc., clash or rub against the package, fragments of package may break off and generate dust.
   (4) Acrylate anaerobic adhesives are generally used to attach CMOS image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the CMOS image sensor in place until the adhesive completely hardens. (reference)
   (5) Note that the sensor may be affected when using visible light other than ultraviolet ray and infrared ray etc. on mounting it.

4. Recommended reflow soldering conditions
   The following items should be observed for reflow soldering.
   (1) Temperature profile for reflow soldering

Control Item	Profile (At Part Side Surface)
1. Preheating	150 to 180℃ 60 to 120s
2. Temperature up (down)	+4℃/s or less (−6℃/s or less)
3. Reflow temperature	Over 230℃ 10 to 30s Max. 5℃/s
4. Peak temperature	Max. 240 ± 5℃

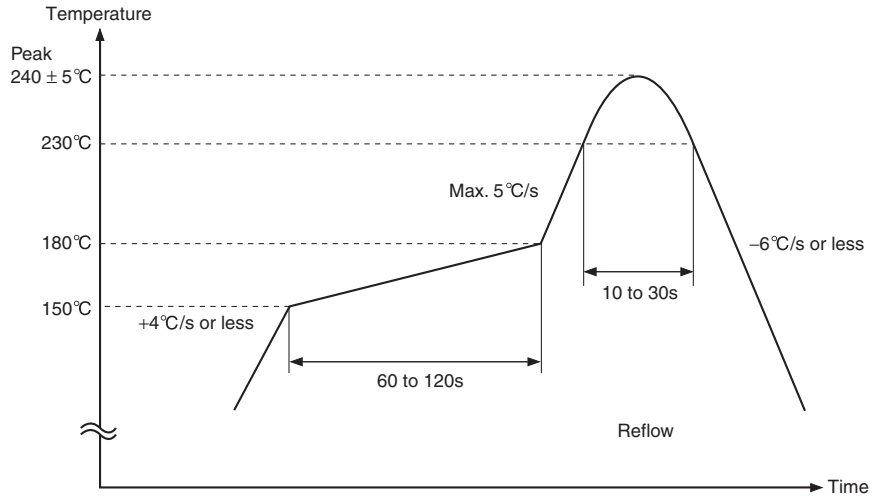


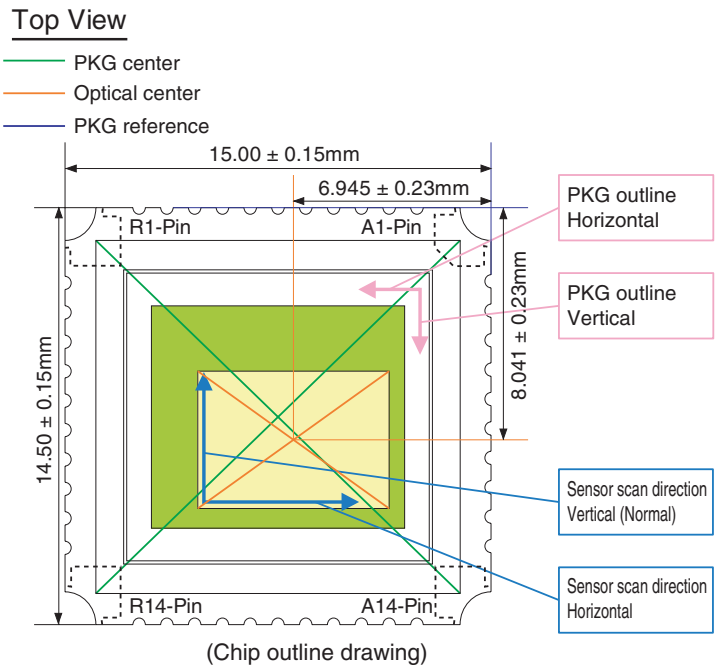
Fig. Reflow Profile (At Part Side Surface)

   (2) Reflow conditions
      (a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245℃.
      (b) Perform the reflow soldering only one time.
      (c) Finish reflow soldering within 72 hours after unsealing the degassed packing.
      Store the products under the condition of temperature of 30℃ or less and humidity of 70% RH or less after unsealing the package.
      (d) Perform re-baking only one time under the condition at 125℃ for 24h.
   (3) Others
      (a) Carry out evaluation for the solder joint reliability in your company.
      (b) After the reflow, the paste of protective tape may remain around the seal glass.
      (The paste residue of protective tape should be ignored except remarkable one.)
      (c) Note that X-ray inspection may affect characteristics of the sensor.

5. Others
   (1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored.
   (2) Exposure to high temperature or humidity will affect the product characteristics. Accordingly avoid storage or use in such conditions.
   (3) Note that characteristics of the sensor may be affected when applying excessive mechanical shocks to it.
   (4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
   (5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Optical Information

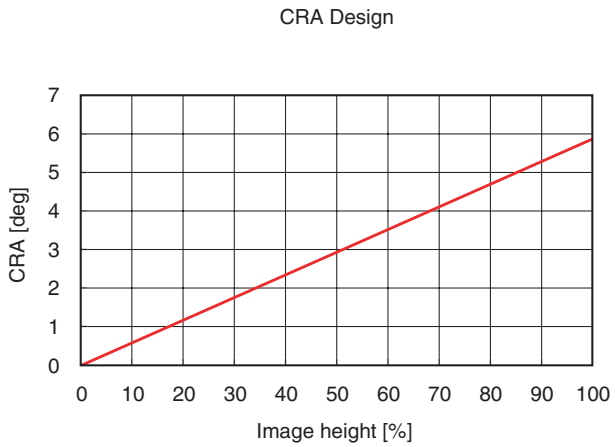
Optical center



(Chip outline drawing)

CRA characteristics

(EPD = –30mm)



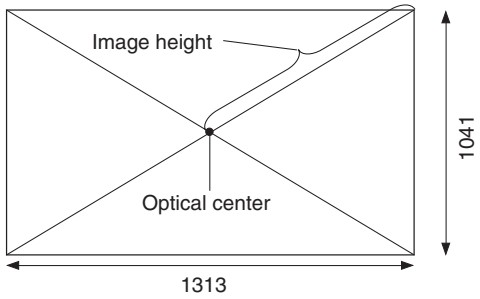
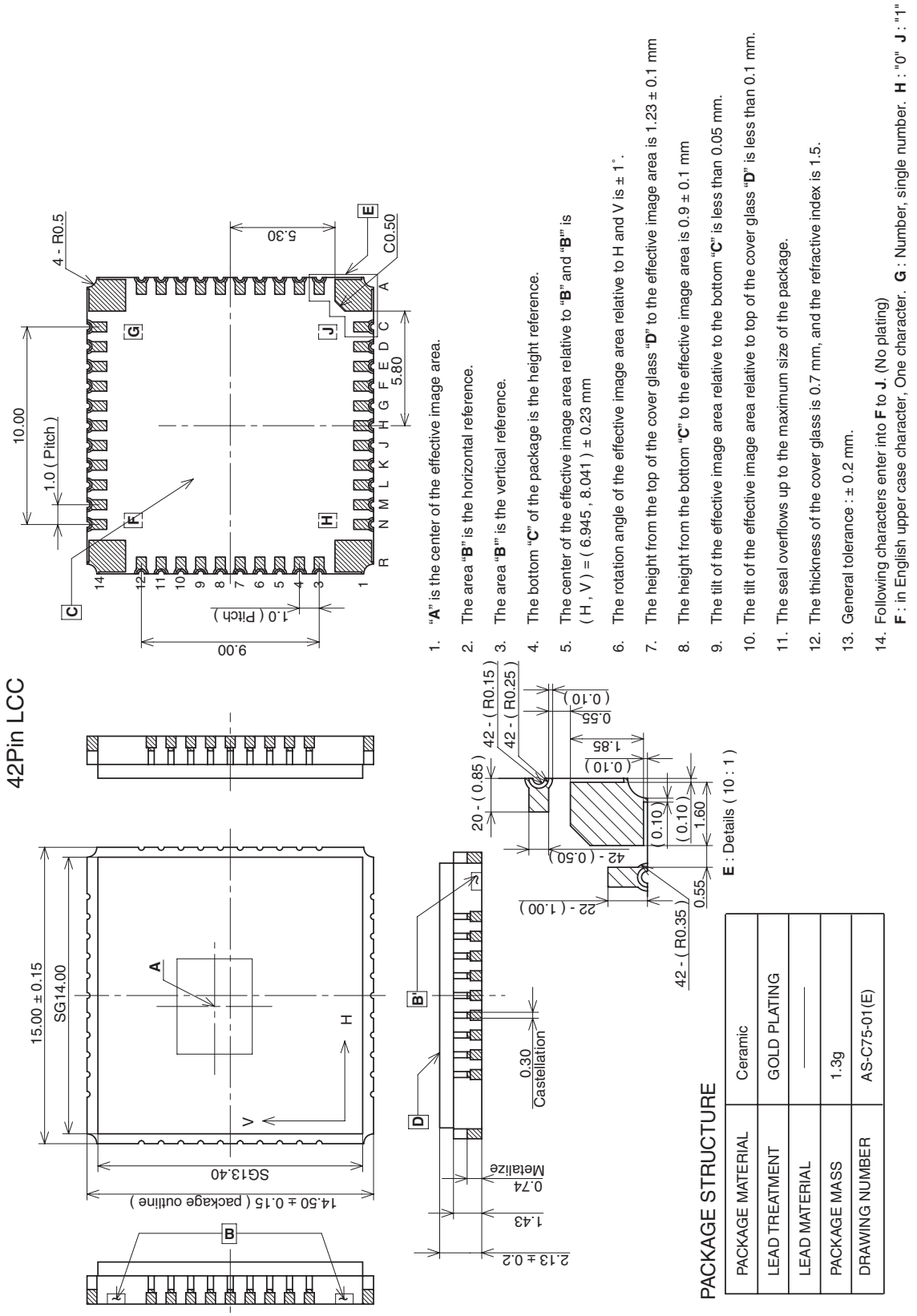


Image Height		CRA (deg)
(%)	(mm)	
0	0.00	0.00
5	0.15	0.29
10	0.30	0.58
15	0.46	0.87
20	0.61	1.16
25	0.76	1.45
30	0.91	1.74
35	1.06	2.03
40	1.22	2.32
45	1.37	2.61
50	1.52	2.91
55	1.67	3.20
60	1.82	3.49
65	1.98	3.78
70	2.13	4.07
75	2.28	4.36
80	2.43	4.65
85	2.58	4.95
90	2.74	5.24
95	2.89	5.53
100	3.04	5.83

Package Outline

(Unit: mm)



1. "**A**" is the center of the effective image area.
2. The area "**B**" is the horizontal reference.
3. The area "**B'**" is the vertical reference.
4. The bottom "**C**" of the package is the height reference.
5. The center of the effective image area relative to "**B**" and "**B'**" is (H , V) = (6.945 , 8.041) ± 0.23 mm
6. The rotation angle of the effective image area relative to H and V is ± 1°.
7. The height from the top of the cover glass "**D**" to the effective image area is 1.23 ± 0.1 mm
8. The height from the bottom "**C**" to the effective image area is 0.9 ± 0.1 mm
9. The tilt of the effective image area relative to the bottom "**C**" is less than 0.05 mm.
10. The tilt of the effective image area relative to top of the cover glass "**D**" is less than 0.1 mm.
11. The seal overflows up to the maximum size of the package.
12. The thickness of the cover glass is 0.7 mm, and the refractive index is 1.5.
13. General tolerance : ± 0.2 mm.
14. Following characters enter into **F** to **J**. (No plating)
    F : in English upper case character, One character. **G** : Number, single number. **H** : "0" **J** : "1"

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	———
PACKAGE MASS	1.3g
DRAWING NUMBER	AS-C75-01(E)