USB2.0 Video Class

Webcam Controller

SN9C2759DM

Datasheet

For the latest data sheet, please visit www.sunnywale.com

Version 1.10

Rev.	Date	Description
1.00	2019-07-30	Formal release
1.01	2019-08-20	Fix Typo Error
1.10	2020-02-07	Add ESD Information

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1 General Description

The SN9C2759DM is a webcam controller with better image quality than before because of improved image quality and also the integrated temporal and spatial noise-reduction circuits. It not only brings noise-free image for human eye but also makes the analysis work in machine-vision easier and more robust.

The major functions of SN9C2759DM include controlling the CMOS sensor, receiving the image data, converting it to video stream, then sending data to the host via USB. It's compliant with USB 2.0 High-Speed (HS) and USB Video Class (UVC) 1.1. Compliance with the public standards makes SN9C2759DM easy to be integrated into various fields of application that need high quality video like NB built-in camera, camcorder, surveillance, video conference and machine vision.

In video part, SN9C2759DM supports MIPI-CSI2 CMOS sensor interfaces and the resolution of ISP is up to MJPG HD@30fps. Besides the excellent noise-reduction, the new generation ISP is high dynamic range (HDR) design to bring better visual experience. The high performance Motion-JPEG engine and bit rate controller provides various compression ratios to meet bandwidth requirement. This system is controlled by the embedded micro-controller with the built-in statistics of AE / AWB. The flexible architecture includes the mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters.

The SN9C2759DM introduces advanced process so that it can keep the power consumption in quite low level and makes the package as small as possible. There are 3 built-in regulators and no needs of external oscillator, these features make it able to further save BOM and PCB area. The SN9C2759DM is the best choice for the compact modern electronic product design.

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2 Feature

2.1 System

- 3.3V single power supply
  - Power consumption
  - standby: < 30mA
  - suspend: <500uA
  - operation: <150mA
- Built-in clock synthesizer and PLL for internal clock generation
- Using external serial flash to store customized code and data (support up to 4Mbits)
- High speed serial flash controller (60MHz) with phase detection
- External RAM is unnecessary
- With 2sets of selectable 1.0V, 1.2V, 1.5V, 1.85V, 2.0V, 2.85V, 3.0V, 3.3V(bypass) LDO to supply CMOS sensor analog and IO power
- QFN32 2mm x 5.5mm package
- 7 GPIO

2.2 USB Controller

- USB 2.0 high-speed (HS) and full-speed (FS) compatible
- USB2.0 HS/FS auto sensing and switching
- USB FS mode and USB disconnection are programmable
- Support device power state – Runtime D3 of ACPI
- Endpoints:
  - CONTROL
  - Interrupt IN: UVC x 1
  - Isochronous IN: UVC x1
- 6 alternate settings for Video Streaming Interface

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2.3 Sensor Interface

- Sensor interface: MIPI-CSI2 1-lane
- Sensor resolution: up to 1280x800
- Sensor data format: YUYV and Bayer RAW
- Sensor pixel clock: up to 120MHz pixel clock
- Control interface: industrial standard 2-wire serial interface

2.4 Color Processing

- AE histogram statistics
- AWB window statistics
- On-the fly defect-pixel cancellation
- Lens shading compensation for R/G/B channel
- Color interpolation with Low pass filter
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels
- Programmable color conversion matrix for R/G/B input
- Temporal noise-reduction
- Advanced spatial noise reduction
- Wide Dynamic Range (WDR)
- De-color aliasing in edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation
- Auto gamma for backlight preview
- Auto frequency detection statistics

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2.5 Scaling Engine

- Combined scaling and windowing function provides similar view angle under different output resolution.
- With LPF to eliminate artifact (Satisfy Microsoft Lync unify under max. scaling down ratio which is 1280→160 pixels)

2.6 JPEG Encoder

- YUV422 baseline JPEG encoder
- Programmable 128 bytes quantization table for Y and C to adjust compression ratio
- Built-in bit rate controller
- Exception handling circuit for suddenly huge bit-rate change that over the capability of rate controller and occurs USB buffer overflow

2.7 Video Streaming

- USB Video Class 1.1 (UVC) compliant
- Formats
  - Support UVC1.1 - Uncompressed YUY2 payload (YUV422, 16bits/pixel)
  - Support UVC1.1 – MJPG422 payload
  - YUY2 & MJPG share the same USB endpoint, the existence of these 2 stream formats are mutual exclusive
- Resolutions & frame rates

	HD	SVGA	VGA
MJPG	60fps	60fps	60fps
YUY2	12fps	20fps	30fps

2.8 Micro Controller and USB Device Features

- Built-in 8032 micro controller
- Auto load extended F/W from external serial flash
- Auto load VID/PID, manufacturer, product and serial number string from external serial flash
- Auto load UVC parameter definition from external serial flash
- Firmware is upgradeable from PC via USB

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- Able to force USB at FS mode & USB disconnect
- Watch dog to auto recovery

2.9 Pre-defined USB Video Class Controls

- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- White Balance Temperature (UVC defined)
- Backlight Compensation (UVC defined)
- Gain (UVC defined)
- Power Line Frequency (UVC defined)
- White Balance Temperature, Auto (UVC defined)
- Auto-Exposure Mode (UVC defined)
- Auto-Exposure Priority (UVC defined)
- Exposure Time(Absolute), (UVC defined)
- LED indicator on video streaming
- UVC Extension unit support

2.10 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, , Microsoft Window 7 32 & 64 bit, Microsoft Window 8/8.1 32 & 64 bit, Microsoft Window 10 32 & 64 bit
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

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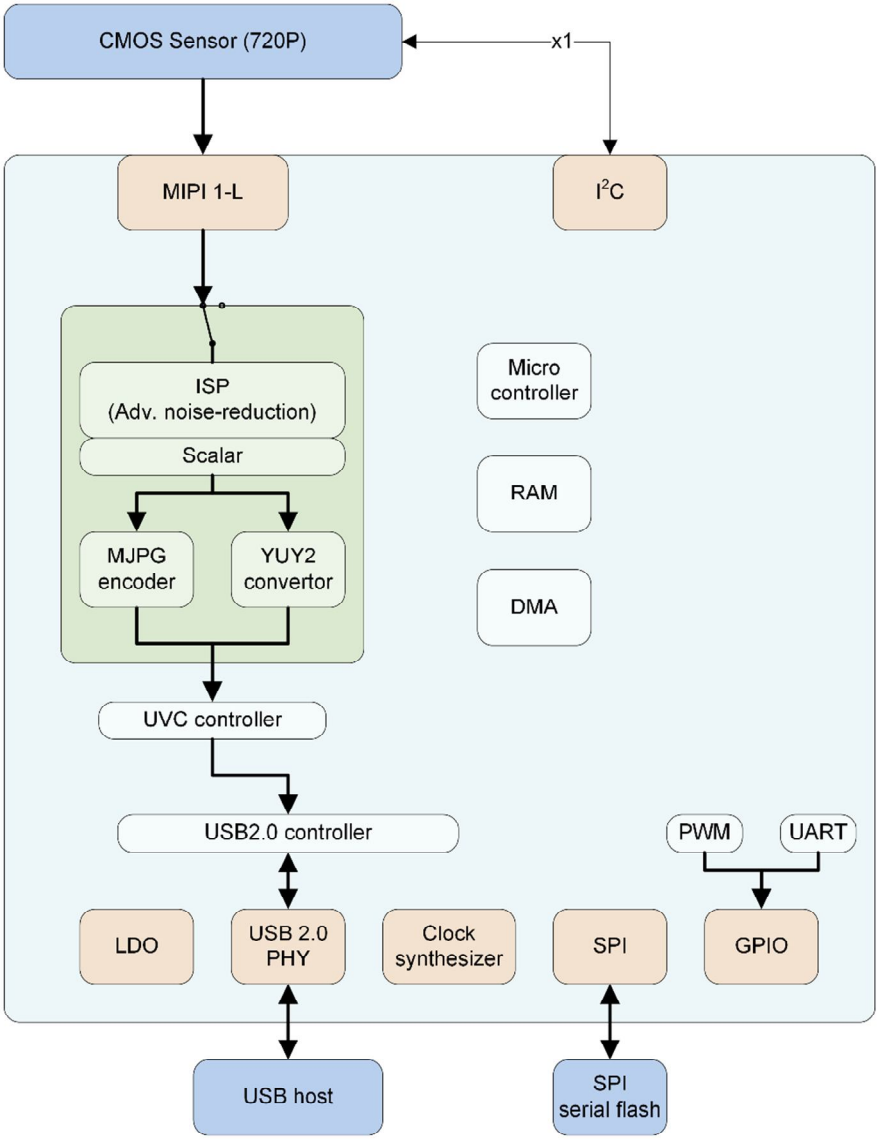
3 Function Block Diagram



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4 Pin Assignment

4.1 SN9C2759DMJG - QFN32

4.1.1 Pin-Out Diagram

		VDD33	GND	SF_SI	SF_SCK	SF_CS	SF_SO	GPIO[2]	GND	VDD12	VDDA_SEN	VDD33	VDDIO_SEN	GPIO[7]		
		29	28	27	26	25	24	23	22	21	20	19	18	17		
VDD12	30														16	VDD12
DM	31							**SN9C2759DMJG/QFN32-2x5.5**							15	DN0
DP	32														14	DP0
		1	2	3	4	5	6	7	8	9	10	11	12	13		
		GPIO[0]	GPIO[1]	VDD12	GPIO[6]	GND	GPIO[4]	GPIO[3]	SDA	SCL	SEN_CLK	GND	DPCK	DNCK		

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4.1.2 Pin-Out Description

Pin No	Pin Name	Mode			Desctiption
		Power Up	Normal	Suspend	
1	GPIO0	I	B	PD	General purpose I/O. Default for LED control.
2	GPIO1	I	B	PD	General purpose I/O. Default for SPI serial flash write protect control.
3	VDD12	P	P	P	DSP core power.
4	GPIO6	I	B	PD	General purpose I/O.
5	GND	P	P	P	Ground.
6	GPIO4	I	B	PD	General purpose I/O.
7	GPIO3	I	B	PD	General purpose I/O. Default for sensor power down control. (1.8v/3.3v)
8	SDA	I	B	PD	I2C data for sensor.
9	SCL	I	B	PD	I2C clock for sensor.
10	SEN_CLK	O	O	O	Sensor clock.
11	GND	P	P	P	Ground.
12	DPCK	A	A	A	MIPI sensor clock lane positive signal.
13	DNCK	A	A	A	MIPI sensor clock lane negative signal.
14	DP0	A	A	A	MIPI sensor data lane 0 positive signal.
15	DN0	A	A	A	MIPI sensor data lane 0 negative signal.
16	VDD12	P	P	P	DSP core power.
17	GPIO7	I	B	PD	General purpose I/O.
18	VDDIO_SEN	P	P	P	Sensor I/O power supply. Default 1.8V.
19	VDD33	P	P	P	DSP system power.
20	VDDA_SEN	P	P	P	Sensor analog power supply. Default 2.8V.
21	VDD12	P	P	P	DSP core power.
22	GND	P	P	P	Ground.
23	GPIO2	I	B	PD	General purpose I/O. Default for sensor LDO enable control.
24	SF_SO	O	O	O	SPI data out to serial flash.
25	SF_CS	O	O	O	SPI chip select to serial flash.
26	SF_SCK	O	O	O	SPI clock to serial flash.
27	SF_SI	I	I	PD	SPI data in from serial flash.
28	GND	P	P	P	Ground.
29	VDD33	P	P	P	DSP system power.
30	VDD12	P	P	P	DSP core power.
31	DM	A	A	A	USB D-.
32	DP	A	A	A	USB D+.

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5 Electrical Characteristics

5.1 DC Operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD33_18	Power Supply	-0.3 ~ 3.6	V
DVDD	Power Supply	-0.12 ~ 1.32	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

ESD (Electrostatic Discharge ESD) Susceptibility Voltage			
	Human Body Model (HBM)	Machine Model (MM)	Charged-Device Model (CDM)
All Pin	≧5000V	≧200V	≧500V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	Power Supply		3.3		V
VDD33_18	Power Supply		3.3/1.8		V
DVDD	Power Supply		1.2		V
Vin	Input voltage		3.3		V
Supply current Consumed from D3V3	Current Supply		150	200	mA
Suspend current Consumed from D3V3	Power Supply			500	uA

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5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and

VDD33=3.0 ~ 3.6V, VDD33_18=1.62 ~ 3.6V, Ta=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDD33_18)	Input low voltage	CMOS	-0.3		0.2*VDD33_18	V
Vih(VDD33_18)	Input high voltage	CMOS	0.8*VDD33_18		VDD33_18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	µA
Iih	Input high current	no pull-up or pull-down	-1		1	µA
Ioz	Tri-state leakage current		-1		1	µA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

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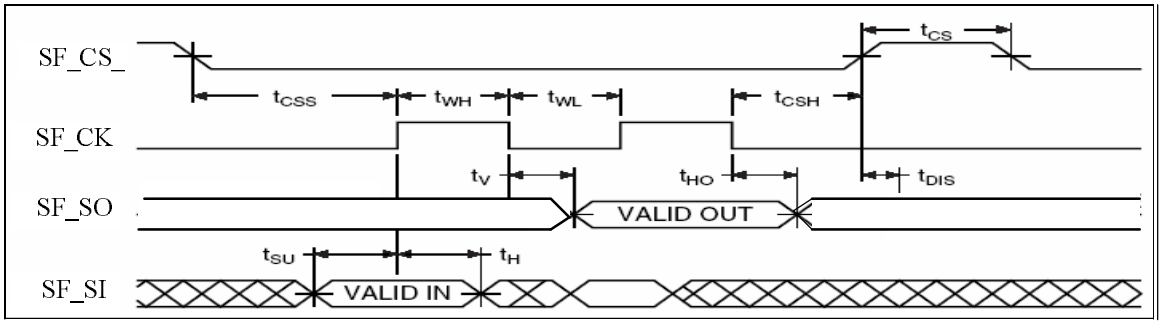
5.2 AC Operating Condition

5.2.1 Serial Flash Interface



- fSCK = 24 MHz (SPEED=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

- fSCK = 12 MHz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns

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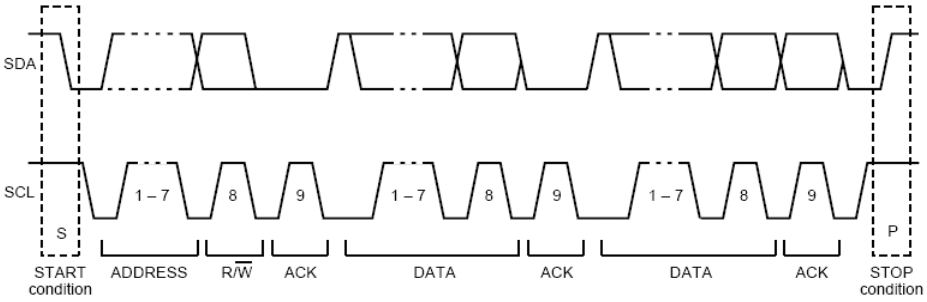
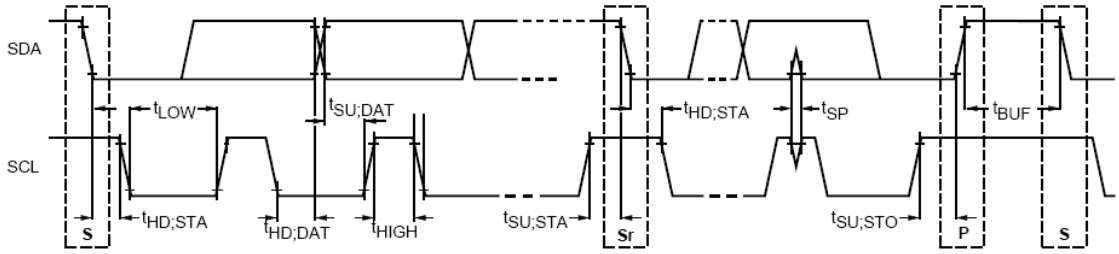
5.2.2 I2C Control Interface



A complete data transfer.



Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns

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Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

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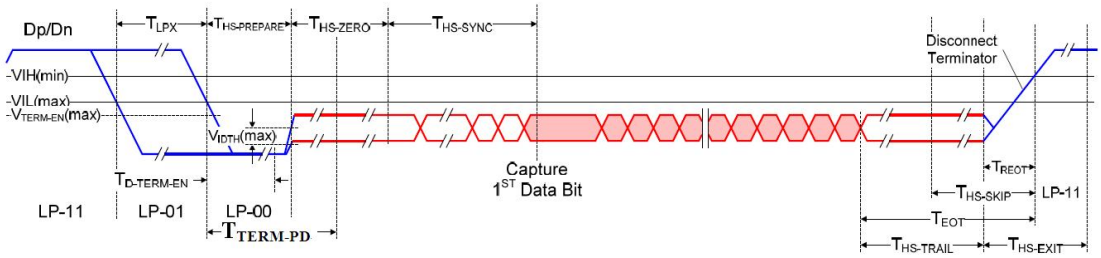
5.2.3 MIPI Sensor Interface

High-speed Data Transmission



- MIPI Operation Timing Parameters

Parameter	Min	Max	Unit
$T_{LPX(1)}$	66		ns
$T_{HS-PREPARE(2)}$	66	85ns + 6*$UI_{(3)}$	ns
$T_{HS-ZERO(4)}$	120	2*[$T_{HS-EXIT}$ – (110ns+10*UI)]	ns
$T_{HS-TRAIL(5)}$	16*UI		ns
$T_{HS-EXIT(6)}$	240ns + 110*UI		ns
$T_{EOT(7)}$	16*UI	105ns + 12*UI	ns

1. T_{LPX} is the time from the end of LP-11state to the start of LP-00 state.
2. $T_{HS-PREPARE}$ is the time from the start of LP-00 to the start of the HS-0 state.
3. UI is the one data bit time.
4. $T_{HS-ZERO}$ is the time during HS-0 state.
5. $T_{HS-TRAIL}$ is the time that the transmitter drives the differential state after last data bit of HS burst.
6. $T_{HS-EXIT}$ is the time from the end of $T_{HS-TRAIL}$ to the start of the LP-01 of the next packet.
7. T_{EOT} is the time from the end of $T_{HS-TRAIL}$ to Low-Power state that mean DP = 1 and DN = 1.

- The ranges of the red marked parameters for the above table must be satisfied. The other parameters can reference the document of MIPI Alliance Specification for DPHY.
- $T_{TERM-PD}$ is the time from termination enable to the release of power down. The range of $T_{TERM-PD}$ is from ($T_{HS-PREPARE}$ + 33 ns) to ($T_{HS-ZERO}$ + $T_{HS-PREPARE}$ – 33ns) and the suggestion value is the min($T_{HS-PREPARE}$ + 0.5*$T_{HS-ZERO}$, 495ns).

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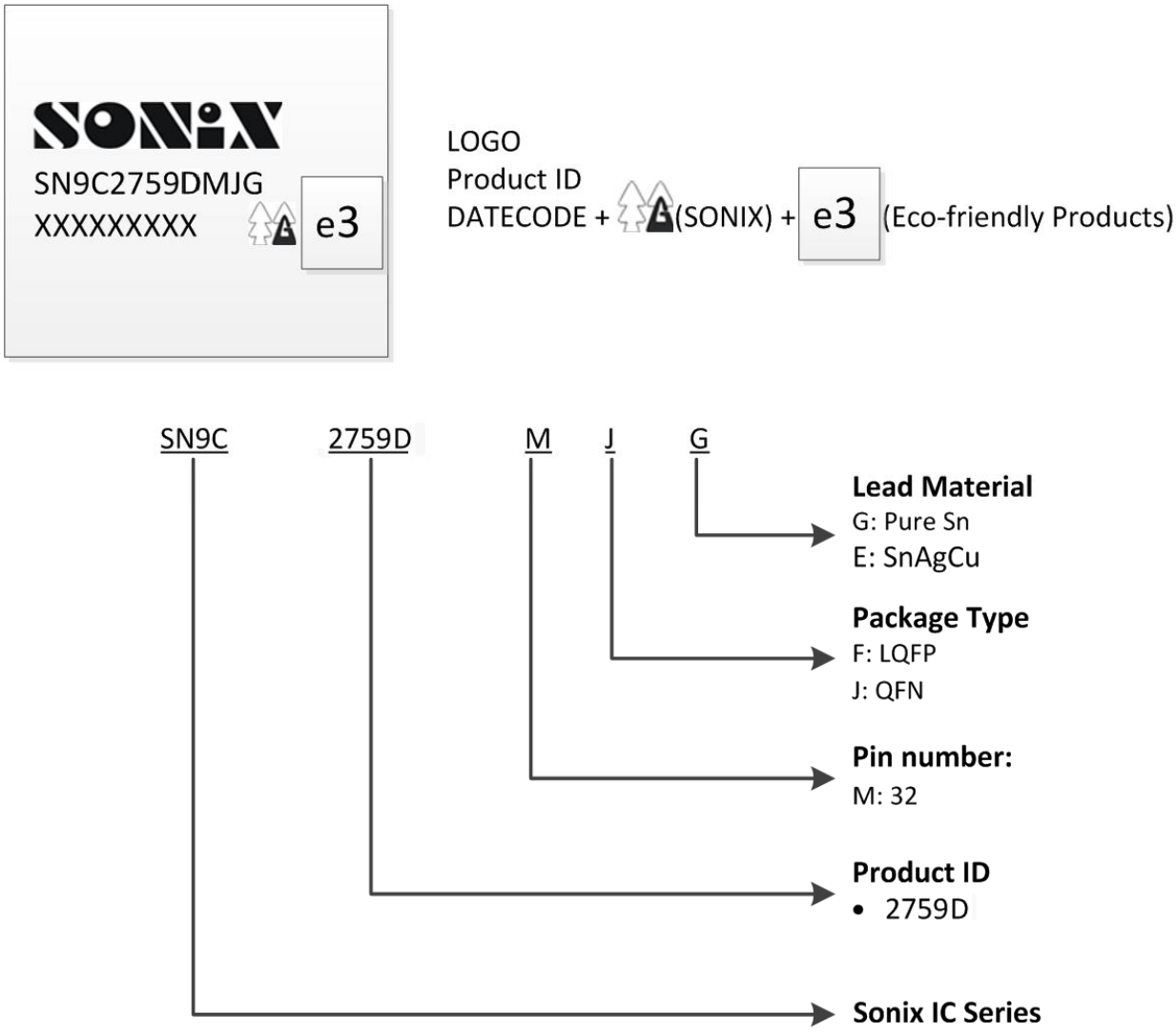
6 Package

6.1 Nomenclature



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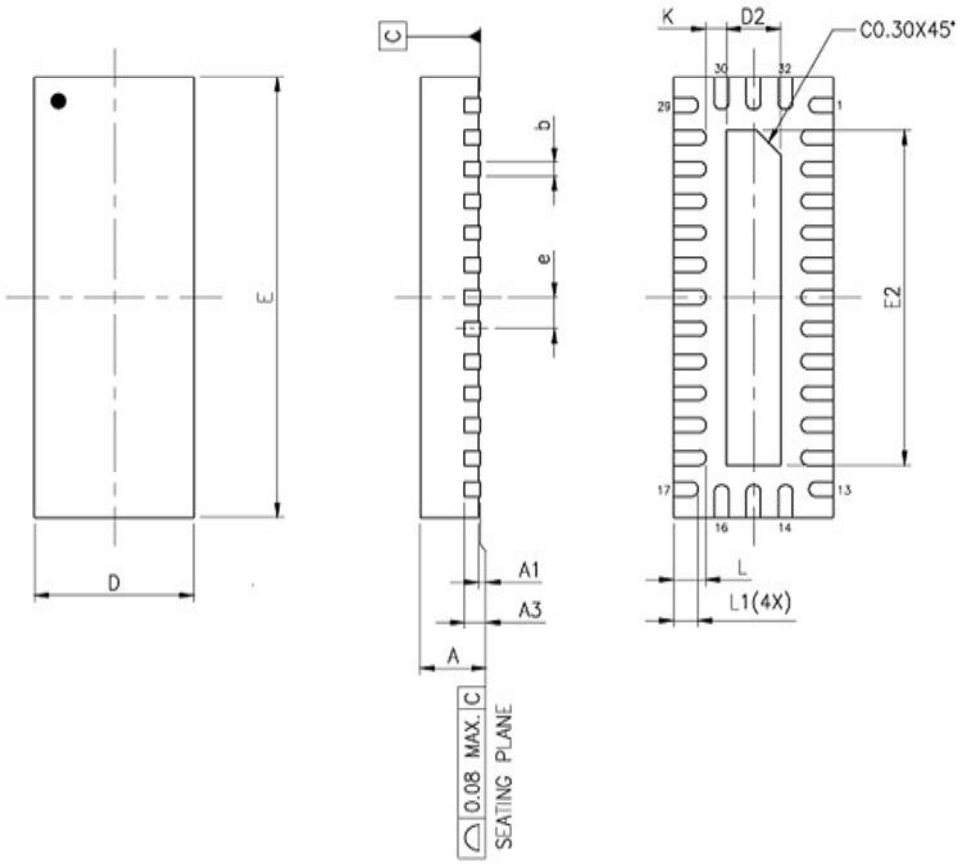
6.2 SN9C2759DMJG - QFN32

6.2.1 Drawing



6.2.2 Dimension

SYMBOLS	MIN.	NOM.	MAX.	NOTES:
A	0.70	0.75	0.80	1. ALL DIMENSIONS ARE IN MILLIMETERS 2. DIMENSION b ALLPIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA. 3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS
A1	0.00	0.02	005	
A3	0.203 REF			
b	0.15	0.20	0.25	
D	2.00 BSC			
E	5.50 BSC			
e	0.40 BSC			
D2	0.65	0.70	0.75	
E2	4.15	4.20	4.25	
L	0.35	0.40	0.45	
L1	0.25	0.30	0.35	
K	0.20	-	-	

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