SONY

Diagonal 15.86 mm (Type 1) CMOS Image Sensor with Square Pixel for Monochrome Cameras

TENTATIVE

IMX183CLK-J

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Description

The IMX183CLK-J is a diagonal 15.86 mm (Type 1) CMOS image sensor with a monochrome square pixel array and approximately 20.48 M effective pixels. 12-bit digital output makes it possible to output the signals of approximately 20.48 M effective pixels with high definition for shooting still picture.
In addition, this sensor enables output effective approximately 9.03 M effective pixels (aspect ratio approx.17:9) signal performed horizontal and vertical cropping at 59.94 frame/s in 10-bit digital output format for high-definition moving picture.
Furthermore, it realizes 12-bit digital output for shooting high-speed and high-definition moving pictures by horizontal and vertical addition and elimination.
Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable storage time. In addition, as this product is designed for consumer use applications, note that when used for other applications, Sony Semiconductor Solutions Corporation does not guarantee the quality and reliability of the product. This lack of guarantee should be kept in mind when using this product for other than consumer use applications. Consult your Sony Semiconductor Solutions Corporation sales representative if you have any questions.

Features

- Input clock frequency 72 MHz
- All-pixel scan mode
  Horizontal/vertical 2/2-line binning mode
  Horizontal/vertical 3/3-line binning mode
  Vertical 2/9 subsampling binning horizontal 3 binning mode
  Vertical 2/9 subsampling binning horizontal 3 binning mode low power comsumption
  Vertical 2/19 subsampling binning horizontal 3 binning mode
  Vertical 2 binning horizontal 2/4 subsampling mode
- High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- Variable-speed shutter function (minimum unit: 1 horizontal sync signal period (1XHS))
- Low power consumption
- H driver, V driver and serial communication circuit on chip
- CDS/PGA on chip. Gain +27 dB (step pitch 0.1 dB)
- 9-bit/10-bit/12-bit A/D conversion on chip
- All-pixel simultaneous reset supported (use with mechanical shutter)
- 118-pin high-precision ceramic package

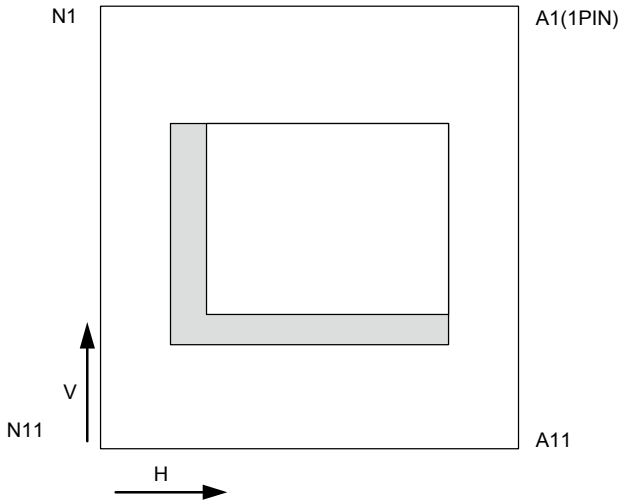
Exmor R

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 15.86 mm (Type 1)
- ◆Total number of pixels
  5640 (H) × 3710 (V) approx. 20.92 M pixels
- ◆Number of effective pixels
  - Type 1 approx. 20.48 M pixels use : 5544 (H) × 3694 (V) approx. 20.48 M pixels
  - Type 1/1.4 approx. 9.03 M pixels use : 4152 (H) × 2174 (V) approx. 9.03 M pixels
- ◆Number of active pixels
  - Type 1 approx. 20.48 M pixels use : 5496 (H) × 3672 (V) approx. 20.18 M pixels diagonal 15.86 mm
  - Type 1/1.4 approx. 9.03 M pixels use : 4128 (H) × 2168 (V) approx. 8.95 M pixels diagonal 11.19 mm
- ◆Number of recommended recording pixels
  - Type 1 approx. 20.48 M pixels use : 5472 (H) × 3648 (V) approx. 19.96 M pixels aspect ratio 3:2
  - Type 1/1.4 approx. 9.03 M pixels use : 4096 (H) × 2160 (V) approx. 8.85 M pixels aspect ratio approx. 17:9
- ◆Chip size
  16.05 mm (H) × 12.61 mm (V)
- ◆Unit cell size
  2.40 µm (H) × 2.40 µm (V)
- ◆Optical black
  Horizontal (H) direction : Front 48 pixels, rear 0 pixel
  Vertical (V) direction : Front 16 pixels, rear 0 pixel
- ◆Substrate material
  Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Absolute Maximum Ratings

Supply voltage 1	V_{ADD} [*1]	–0.3 to +3.3	V
Supply voltage 2	V_{DDD1} [*2]	–0.5 to +2.0	V
Supply voltage 3	V_{DDD2} [*3]	–0.5 to +3.3	V
Input voltage (digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
Output voltage (digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
Guaranteed operating temperature	T_{OPR}	–10 to +75	˚C
Storage guarantee temperature	T_{STG}	–30 to +80	˚C
Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

Supply voltage 1	V_{ADD} [*1]	2.9 ± 0.1	V
Supply voltage 2	V_{DDD1} [*2]	1.2 ± 0.1	V
Supply voltage 3	V_{DDD2} [*3]	1.8 ± 0.1	V
Input voltage (digital)	V_I	–0.1 to V_{DDD2} + 0.1	V
Output voltage (digital)	V_O	–0.1 to V_{DDD2} + 0.1	V

[*1] V_{ADD}: V_{DD}SUB, V_{DD}HCM1 to 2, V_{DD}HVS, V_{DD}HPX, V_{DD}HDA1 to 2, V_{DD}HCP (2.9 V power supply)
[*2] V_{DDD1}: V_{DD}LCN1 to 6, V_{DD}LSC1 to 2, V_{DD}LPL (1.2 V power supply)
[*3] V_{DDD2}: V_{DD}MIO, V_{DD}MIF1 to 2(1.8 V power supply)

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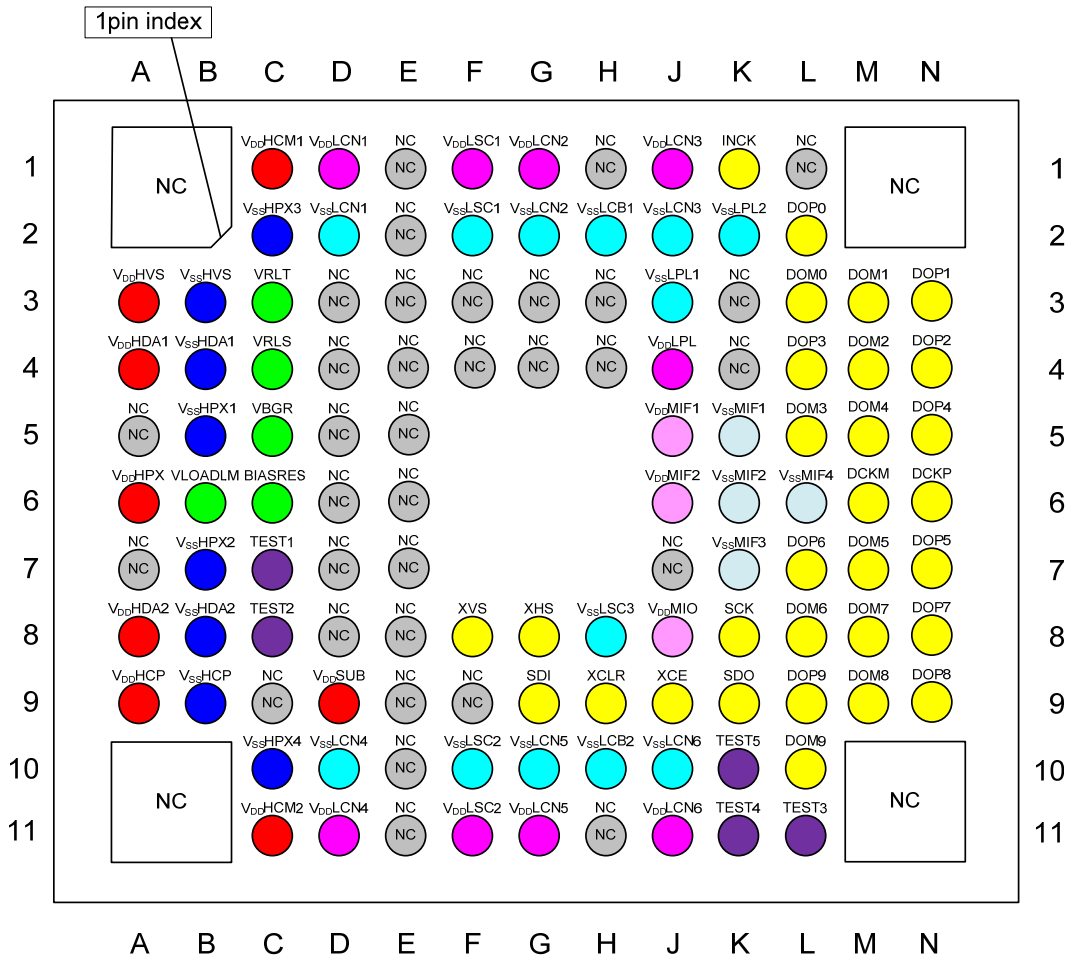
General-0.0.9

Contents

Pin Configuration

(Bottom View)



Pin Description

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
A3	V_{DD}HVS	Power	A	Analog power supply (2.9 V)	—	
A4	V_{DD}HDA1	Power	A	Analog power supply (2.9 V)	—	
A6	V_{DD}HPX	Power	A	Analog power supply (2.9 V)	—	
A8	V_{DD}HDA2	Power	A	Analog power supply (2.9 V)	—	
A9	V_{DD}HCP	Power	A	Analog power supply (2.9 V)	—	
B3	V_{SS}HVS	GND	A	Analog GND (2.9 V)	—	
B4	V_{SS}HDA1	GND	A	Analog GND (2.9 V)	—	
B5	V_{SS}HPX1	GND	A	Analog GND (2.9 V)	—	
B6	VLOADLM	O	A	Capacitor connection	Pull-down	
B7	V_{SS}HPX2	GND	A	Analog GND (2.9 V)	—	
B8	V_{SS}HDA2	GND	A	Analog GND (2.9 V)	—	
B9	V_{SS}HCP	GND	A	Analog GND (2.9 V)	—	
C1	V_{DD}HCM1	Power	A	Analog power supply (2.9 V)	—	
C2	V_{SS}HPX3	GND	A	Analog GND (2.9 V)	—	
C3	VRLT	O	A	Capacitor connection	Pull-down	
C4	VRLS	O	A	Capacitor connection	Pull-down	
C5	VBGR	O	A	Capacitor connection	Hi-Z	
C6	BIASRES	O	A	Resistor connection	Hi-Z	
C7	TEST1	O	A	Test	Hi-Z	Leave open. (No connection)
C8	TEST2	O	A	Test	Hi-Z	Leave open. (No connection)
C10	V_{SS}HPX4	GND	A	Analog GND (2.9 V)	—	
C11	V_{DD}HCM2	Power	A	Analog power supply (2.9 V)	—	
D1	V_{DD}LCN1	Power	D	Digital power supply (1.2 V)	—	
D2	V_{SS}LCN1	GND	D	Digital GND (1.2 V)	—	
D9	V_{DD}SUB	Power	A	Analog power supply (2.9 V)	—	
D10	V_{SS}LCN4	GND	D	Digital GND (1.2 V)	—	
D11	V_{DD}LCN4	Power	D	Digital power supply (1.2 V)	—	
F1	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
F2	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
F8	XVS	I	D	Vertical sync signal input	—	
F10	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
F11	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
G1	V_{DD}LCN2	Power	D	Digital power supply (1.2 V)	—	
G2	V_{SS}LCN2	GND	D	Digital GND (1.2 V)	—	
G8	XHS	I	D	Horizontal sync signal input	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
G9	SDI	I	D	Serial communication data input	—	
G10	V_{SS}LCN5	GND	D	Digital GND (1.2 V)	—	
G11	V_{DD}LCN5	Power	D	Digital power supply (1.2 V)	—	
H2	V_{SS}LCB1	GND	D	Digital GND (1.2 V)	—	
H8	V_{SS}LSC3	GND	D	Digital GND (1.2 V)	—	
H9	XCLR	I	D	Reset pulse input	—	
H10	V_{SS}LCB2	GND	D	Digital GND (1.2 V)	—	
J1	V_{DD}LCN3	Power	D	Digital power supply (1.2 V)	—	
J2	V_{SS}LCN3	GND	D	Digital GND (1.2 V)	—	
J3	V_{SS}LPL1	GND	D	Digital GND (1.2 V)	—	
J4	V_{DD}LPL	Power	D	Digital power supply (1.2 V)	—	
J5	V_{DD}MIF1	Power	D	Digital power supply (1.8 V)	—	
J6	V_{DD}MIF2	Power	D	Digital power supply (1.8 V)	—	
J8	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
J9	XCE	I	D	Serial communication enable input	—	
J10	V_{SS}LCN6	GND	D	Digital GND (1.2 V)	—	
J11	V_{DD}LCN6	Power	D	Digital power supply (1.2 V)	—	
K1	INCK	I	D	Input clock	—	
K2	V_{SS}LPL2	GND	D	Digital GND (1.2 V)	—	
K5	V_{SS}MIF1	GND	D	Digital GND (1.8 V)	—	
K6	V_{SS}MIF2	GND	D	Digital GND (1.8 V)	—	
K7	V_{SS}MIF3	GND	D	Digital GND (1.8 V)	—	
K8	SCK	I	D	Serial communication clock input	—	
K9	SDO	O	D	Test output	Low Level	Leave open. (No connection)
K10	TEST5	O	D	Test	Low Level	Leave open. (No connection)
K11	TEST4	I	D	Test	—	Leave open. (No connection)
L2	DOP0	O	D	Digital LVDS output	Hi-Z	
L3	DOM0	O	D	Digital LVDS output	Hi-Z	
L4	DOP3	O	D	Digital LVDS output	Hi-Z	
L5	DOM3	O	D	Digital LVDS output	Hi-Z	
L6	V_{SS}MIF4	GND	D	Digital GND (1.8 V)	—	
L7	DOP6	O	D	Digital LVDS output	Hi-Z	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
L8	DOM6	O	D	Digital LVDS output	Hi-Z	
L9	DOP9	O	D	Digital LVDS output	Hi-Z	
L10	DOM9	O	D	Digital LVDS output	Hi-Z	
L11	TEST3	I	D	Test	—	Leave open. (No connection)
M3	DOM1	O	D	Digital LVDS output	Hi-Z	
M4	DOM2	O	D	Digital LVDS output	Hi-Z	
M5	DOM4	O	D	Digital LVDS output	Hi-Z	
M6	DCKM	O	D	Digital LVDS output	Hi-Z	
M7	DOM5	O	D	Digital LVDS output	Hi-Z	
M8	DOM7	O	D	Digital LVDS output	Hi-Z	
M9	DOM8	O	D	Digital LVDS output	Hi-Z	
N3	DOP1	O	D	Digital LVDS output	Hi-Z	
N4	DOP2	O	D	Digital LVDS output	Hi-Z	
N5	DOP4	O	D	Digital LVDS output	Hi-Z	
N6	DCKP	O	D	Digital LVDS output	Hi-Z	
N7	DOP5	O	D	Digital LVDS output	Hi-Z	
N8	DOP7	O	D	Digital LVDS output	Hi-Z	
N9	DOP8	O	D	Digital LVDS output	Hi-Z	

Electrical Characteristics

Electrical characteristics of the IMX183CLK-J are shown below.

1. DC Characteristics

Current Consumption and Gain Variable Range

(V_{ADD} = 3.0 V, V_{DDD1} = 1.3 V, V_{DDD2} = 1.9 V, Tj = 60 ˚C, Reference Gain (0 dB), approximately 19.96 M pixels readout (MODE0), 21.98 frame/s)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	150	mA	
Current consumption (Digital)	I_{DDD1}	—	—	180	mA	
Current consumption (I/O)	I_{DDD2}	—	—	27	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	70	μA	In the dark
Standby current (Digital)	$I_{DDD1STB}$	—	—	11500	μA	In the dark
Standby current (I/O)	$I_{DDD2STB}$	—	—	15	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage

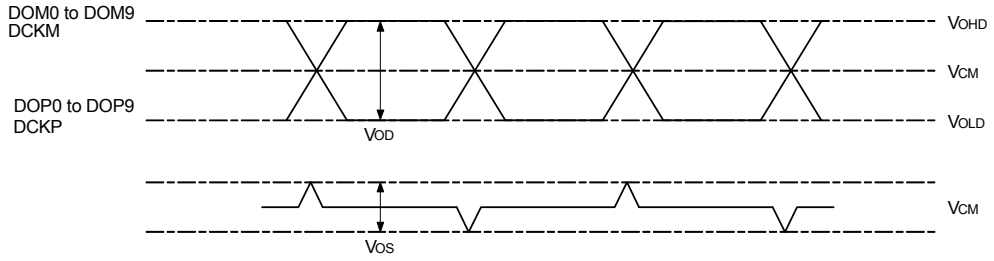
Item		Pins	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	Analog	V_{DD}SUB V_{DD}HCM1 to 2, V_{DD}HVS, V_{DD}HPX V_{DD}HDA1 to 2, V_{DD}HCP	V_{ADD}	2.80	2.90	3.00	V	
	Digital	V_{DD}LCN1 to 6, V_{DD}LSC1 to 2, V_{DD}LPL	V_{DDD1}	1.10	1.20	1.30	V	
	I/O	V_{DD}MIO, V_{DD}MIF1 to 2	V_{DDD2}	1.70	1.80	1.90	V	
Digital input voltage		XCLR, INCK, SCK, SDI, XCE, XHS, XVS	V_{IH}	0.8 × V_{DDD2}	—	V_{DDD2} + 0.1	V	
			V_{IL}	–0.1	—	0.2 × V_{DDD2}	V	
Digital input leakage current			I_{LI}	–1.0	—	1.0	μA	

LVDS Output DC Characteristics

(Termination resistance: 100 Ω, LVDS current : 1.5 mA)

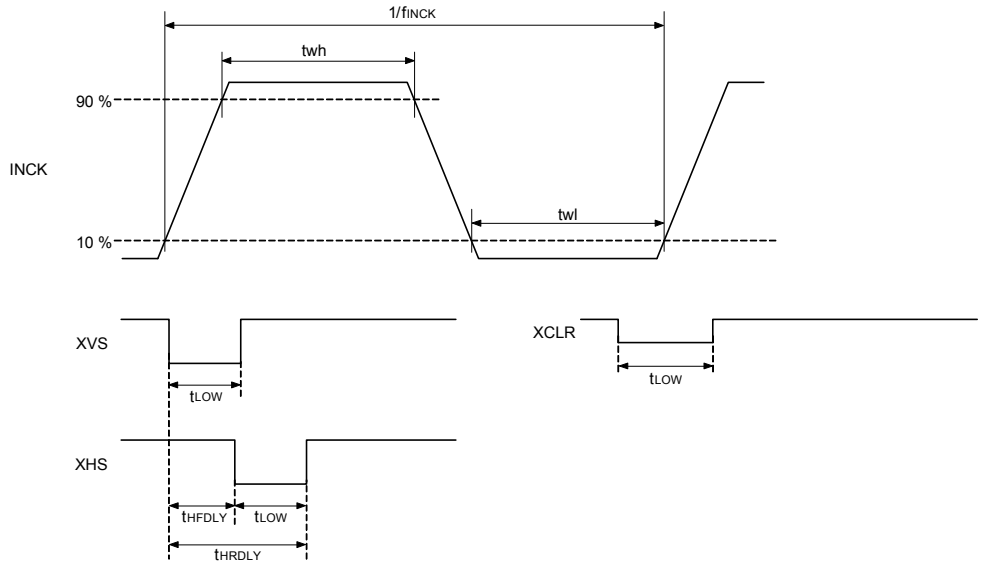
Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit
Digital output voltage	DOP0 to DOP9, DOM0 to DOM9, DCKP, DCKM	Amplitude voltage	V_{OD}	100	150	200	mV
		Common voltage	V_{CM}	$V_{DDD2}/2$ – 100	$V_{DDD2}/2$	$V_{DDD2}/2$ + 100	mV
		Common voltage fluctuation	V_{OS}	—	20	—	mV
		High level output voltage	V_{OHD}	V_{CM} + 50	V_{CM} + 75	V_{CM} + 100	mV
		Low level output voltage	V_{OLD}	V_{CM} – 100	V_{CM} – 75	V_{CM} – 50	mV
		Difference between amplitude voltage channels	V_{ODP}	—	—	50	mV
		Difference between common voltage channels	V_{OSP}	—	—	50	mV

LVDS output



2. AC Characteristics

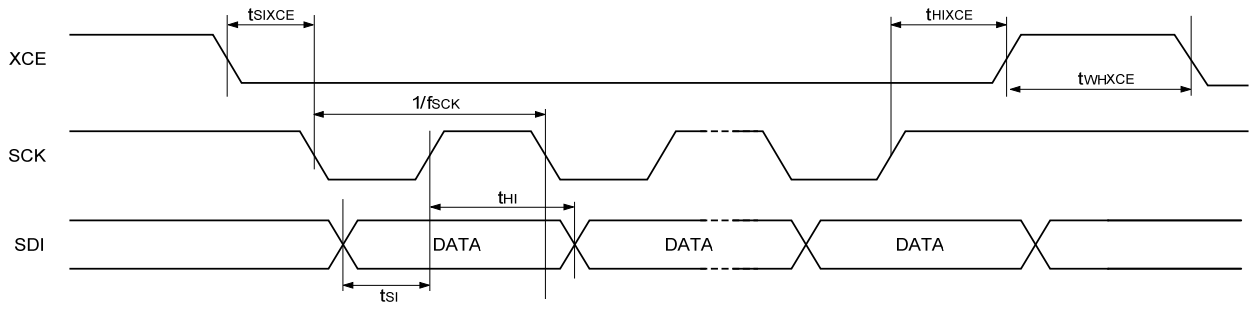
INCK, XVS, XHS, XCLR



Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	71.0	72.0	73.0	MHz
INCK Low level pulse width	twl	5	—	—	ns
INCK High level pulse width	twh	5	—	—	ns
Clock duty	—	40	50	60	%
XVS Low level pulse width	t_{LOW}	55	—	167	ns
XHS Low level pulse width	t_{LOW}	55	—	167	ns
XVS fall – XHS fall width	t_{HFDLY}	0	—	—	ns
XVS fall – XHS rise width	t_{HRDLY}	55	—	167	ns
XCLR Low level pulse width	t_{LOW}	100	—	—	ns

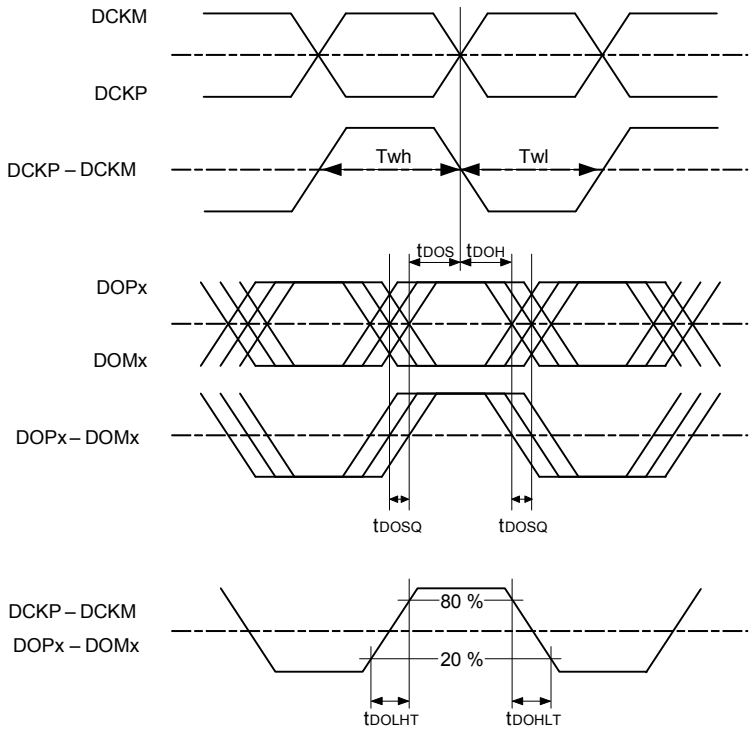
Serial Communication

Serial Control Interface Timing



Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	—	36	MHz
SDI input setup time	t_{SI}	7	—	—	ns
SDI input hold time	t_{HI}	7	—	—	ns
XCE input setup time	t_{SIXCE}	10	—	—	ns
XCE input hold time	t_{HIXCE}	10	—	—	ns
XCE High level pulse width	t_{WHXCE}	27	—	—	ns

3. LVDS output

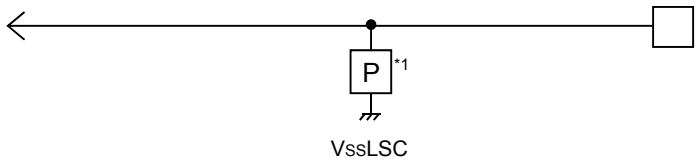
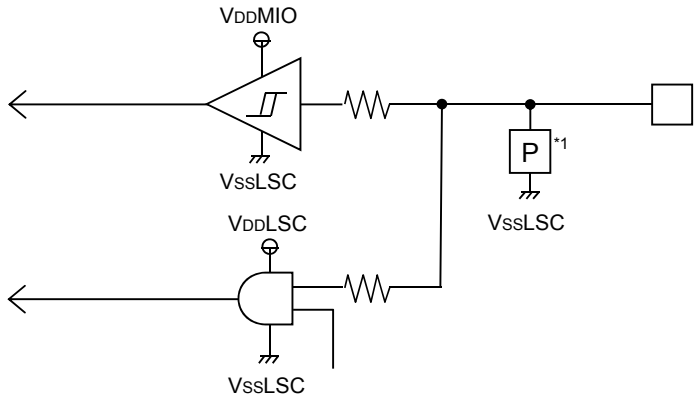
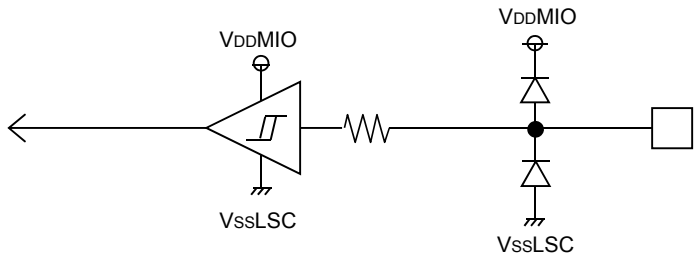
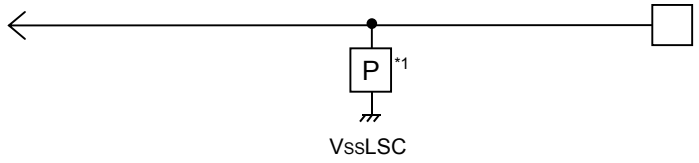
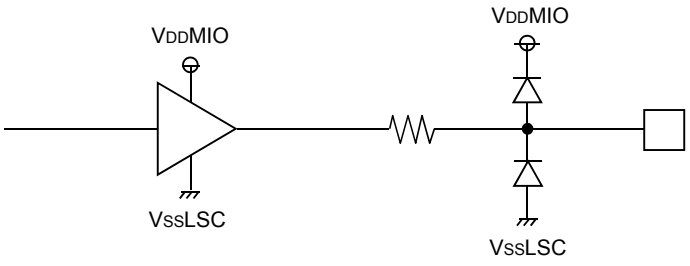


Note) "x" stands for the alphabets of 0 to 9 and the time chart is specified for all output channels.

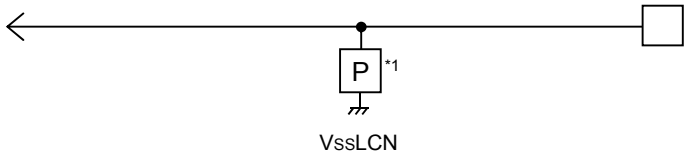
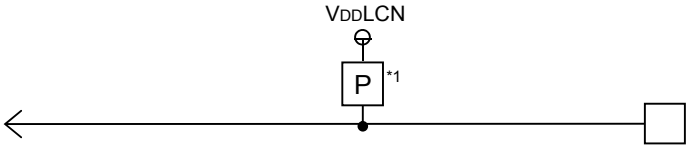
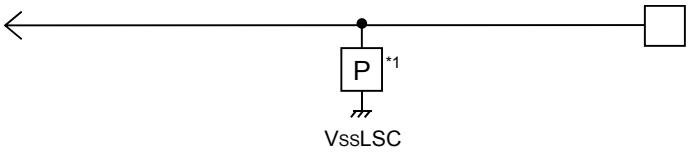
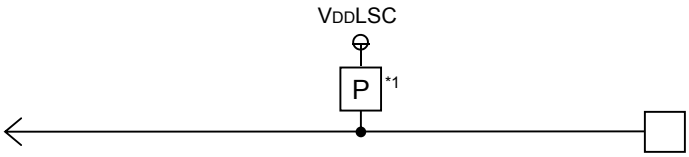
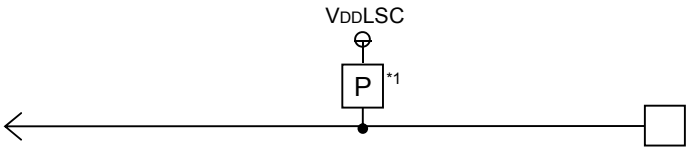
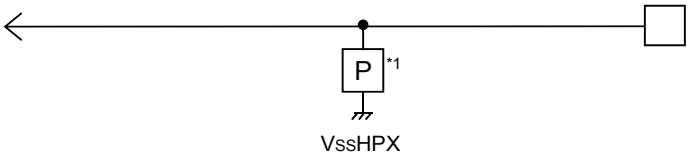
(Termination resistance: 100 Ω, load capacitance: 0 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DO skew time (including jitter)	t_{DOSQ}	—	—	361	ps	Data rate 288 MHzDDR
DO setup time	t_{DOS}	420	—	—	ps	Data rate 288 MHzDDR
DO hold time	t_{DOH}	420	—	—	ps	Data rate 288 MHzDDR
DO rise time	t_{DOLHT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DO fall time	t_{DOHLT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DCK duty cycle	D_{DCDCK}	45	50	55	%	
DCK pulse width	Twh,Twl	1319	—	—	ps	Including period jitter

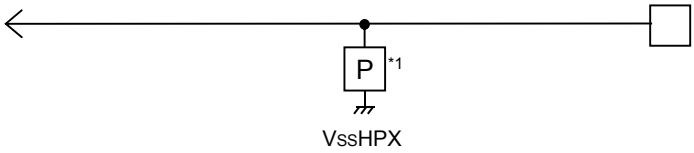
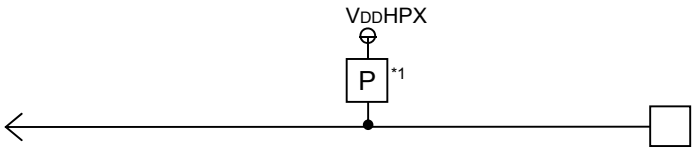
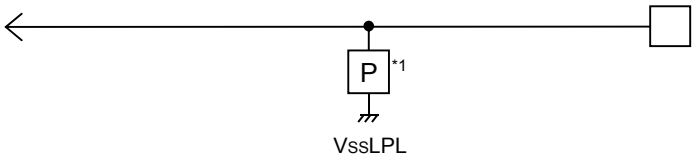
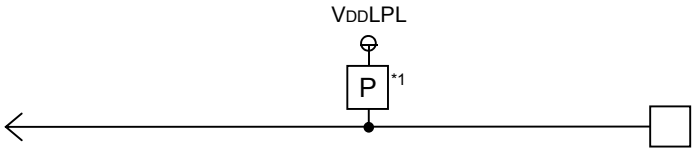
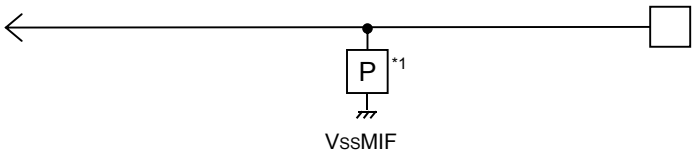
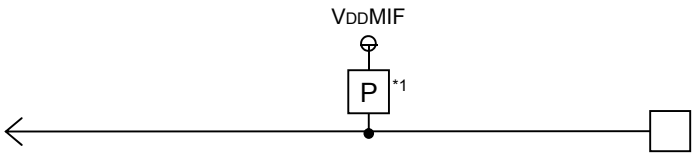
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
V_{DD}SUB	
XCLR	
XCE SCK SDI XHS XVS INCK	
V_{DD}MIO	
SDO	

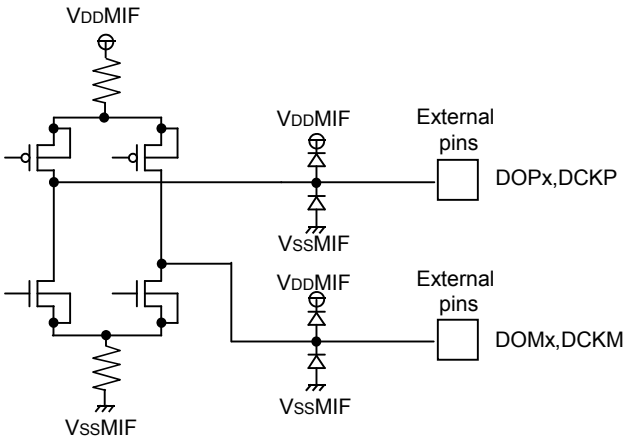
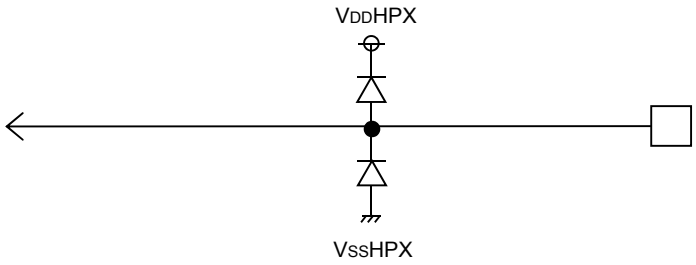
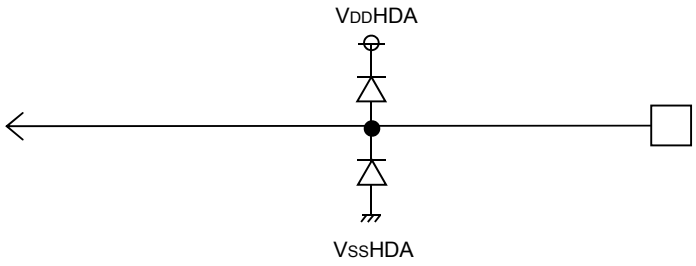
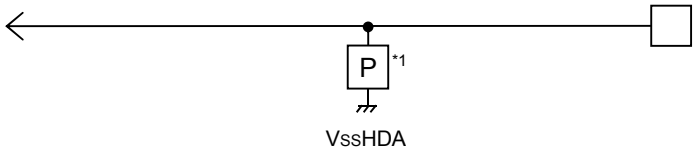
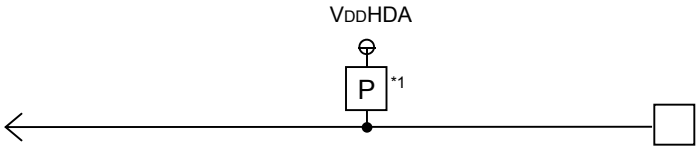
☐: External pins

Symbol	Equivalent circuit
V_{DD}LCN1 V_{DD}LCN2 V_{DD}LCN3 V_{DD}LCN4 V_{DD}LCN5 V_{DD}LCN6	
V_{SS}LCN1 V_{SS}LCN2 V_{SS}LCN3 V_{SS}LCN4 V_{SS}LCN5 V_{SS}LCN6	
V_{DD}LSC1 V_{DD}LSC2	
V_{SS}LSC1 V_{SS}LSC2 V_{SS}LSC3	
V_{SS}LCB1 V_{SS}LCB2	
V_{DD}HCM1 V_{DD}HCM2	

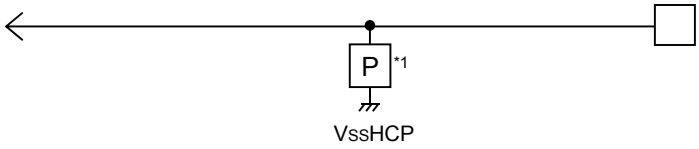
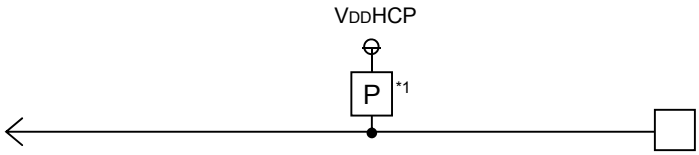
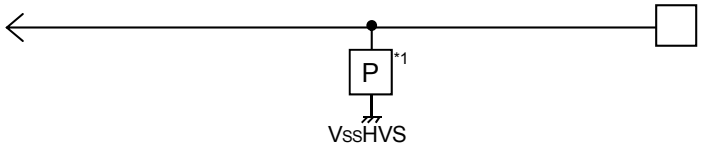
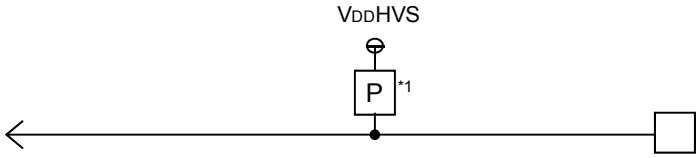
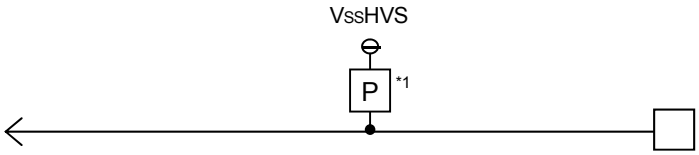
□: External pins

Symbol	Equivalent circuit
V_{DD}HPX	
V_{SS}HPX1 V_{SS}HPX2 V_{SS}HPX3 V_{SS}HPX4	
V_{DD}LPL	
V_{SS}LPL1 V_{SS}LPL2	
V_{DD}MIF1 V_{DD}MIF2	
V_{SS}MIF1 V_{SS}MIF2 V_{SS}MIF3 V_{SS}MIF4	

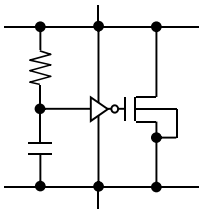
☐: External pins

Symbol	Equivalent circuit
DOPx (x = 0 to 9) DOMx (x = 0 to 9) DCKP DCKM	
VLOADLM	
BIASRES VBGR	
V_{DD}HDA1 V_{DD}HDA2	
V_{SS}HDA1 V_{SS}HDA2	

□: External pins

Symbol	Equivalent circuit
V_{DD}HCP	
V_{SS}HCP	
V_{DD}HVS	
V_{SS}HVS	
VRLS VRLT	

Description of special symbol

Symbol	Equivalent circuit
	

☐: External pins

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics)

T.B.D

Image Sensor Characteristics

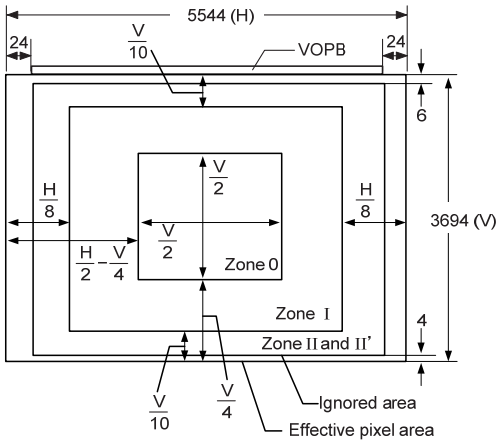
(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, 19.98 frame/s, Reference Gain (0 dB))

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	T.B.D	T.B.D	T.B.D	digit*1	1	1/30 s integration conversion value Zone 0
Saturation signal	Vsat	3824	—	—	digit*1	2	Zone 0, zone I, zone II and zone II'
Video signal shading	SHg	—	—	20	%	3	Zone 0 and zone I (the figure below)
		—	—	25			Zone 0, zone I, zone II and zone II' (the figure below)
Dark signal	Vdt	0	—	0.85	digit*1	4	1/30 s integration conversion value Zone 0, zone I, zone II and zone II'
Dark signal shading	ΔVdt	0	—	1.20	digit*1	5	1/30 s integration conversion value Zone 0, zone I, zone II and zone II'
Dark signal difference	VdOB	−0.41	—	0.41	digit*1	6	1/30 s integration conversion value Zone 0, zone I, zone II and zone II'

*1 Shows digit when 12-bit output.
Example of digit conversion: 1 digit ≈ 0.9858 mV when 10-bit output, 1 digit ≈ 0.2465 mV when 12-bit output.

1. Zone Definition of Image Sensor Characteristics

Zone definition of image sensor characteristics and reference position during dark signal measurement are shown below.



Zone Definition of Image Sensor Characteristics and Reference Position during Dark Signal Measurement

Image Sensor Characteristics Measurement Method

1. Measurement Conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
(2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output.

2. Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance –31.5 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/198.1 s, measure the signal outputs (Vs) at the center of the screen (Zone 0) , and substitute the values into the following formula.

$$S = Vs \times 198.1/30 \text{ [digit]}$$

2. Saturation signal
Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times the intensity with the average value of the signal output, 469 digit when 10-bit output (1874 digit when 12-bit output). Measure the minimum values of the signal when shooting in rolling shutter mode.

3. Video signal shading
Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 469 digit when 10-bit output (1874 digit when 12-bit output). Then measure the maximum value (Vmax [digit]) and the minimum value (Vmin [digit]) of the signal output, and substitute the values into the following formula.

- When 10-bit output
  $SH = (Vmax – Vmin)/469 \times 100$ [%]
- When 12-bit output
  $SH = (Vmax – Vmin)/1874 \times 100$ [%]

4. Dark signal
Measure the average value (Vdt [digit]) of the signal output in zone 0 to zone II' in the light-obstructed state. Define the average value of the signal output accumulated in 1 frame period (t1v) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: t1h) as Vdt1H, and then substitute the values into the following formula.

$$Vdt = (Vdt1V – Vdt1H)/(t1v – t1h)/30 \text{ [digit]}$$

5. Dark signal shading
   Following the item 4, measure the maximum value (Vdmax [digit]) and minimum value (Vdmin [digit]) of the dark signal output, and substitute the values into the following formula.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [digit]}$$

6. Dark signal difference
   Following the item 5, measure the average value of the dark signal output (VdOB [digit]) in zone 0 to zone II' using the optical black (vertical direction VOPB area) level as a reference.

Setting Registers by Serial Communication

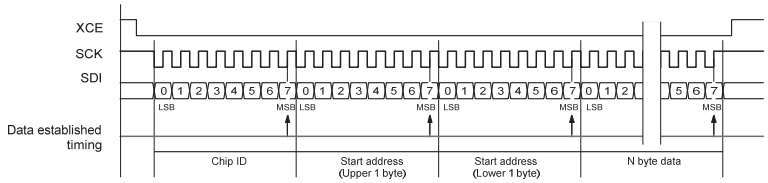
Sensor operation is controlled by the register settings. Follow the procedure below and make the register settings by serial communication.

1. Set XCE Low to enable the chip's serial communication function.
2. Transmit serial data (SDI) synchronized with SCK 1 bit at a time from the lower bits.
3. Transmit the Chip ID (fixed value: 81h) in the first byte.
4. Transmit the address value of the register to be set in the second and third bytes.
5. Transmit the register setting value to the address designated by the second and third bytes in the fourth byte.
6. Transmit the register setting value to the address following the address designated by the second and third bytes in the fifth byte.
7. Transmit the register setting values to subsequent addresses in order thereafter.
8. Set XCE High to end serial communication.

The IMX183CLK-J clears the Chip ID and address setting data by setting XCE High.
Therefore, the Chip ID and address settings must also be made when the next serial communication is performed.
Continuous write across upper bytes is prohibited. When writing across upper bytes, first complete the above sequence, and then perform communication again. In addition, when jumping to a discontinuous address, also first complete the above sequence, and then perform communication again.
Perform serial communication within the 6XHS period (recommended serial communication period) after the fall of XVS to avoid affecting the image quality.
Settings made by serial communication are basically updated immediately each time 1 byte of setting values is transmitted. However, in some exceptional cases (electronic shutter setting, etc.), register setting values are updated immediately before the start of readout immediately after the recommended serial communication period (7th XHS). For details, see “Register Map” on pages 26 to 27 and “1. Register Value Reflection Timing to Output Data” on page 28.

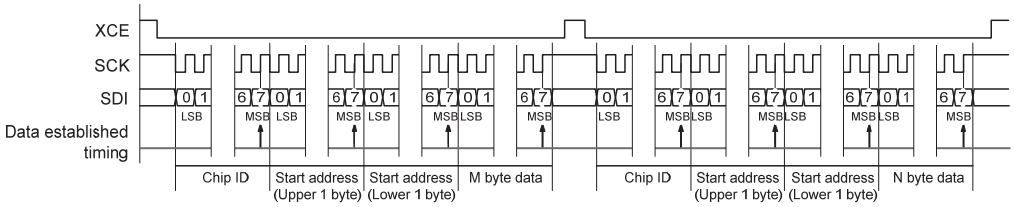
Note) 1. Communication is always accepted.
2. Communication should be completed within the recommended serial communication period to prevent noise. However, this restriction does not apply during the readout period of non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), so register communication can be performed other than during the communication period of those frames.

Example of Serial Communication Timing 1



Example of Serial Communication 1

Example of Serial Communication Timing 2



Example of Serial Communication 2

Register Map

The register map is given below.

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
0000h	[0]	1h	Immediately	STANDBY	0h: Normal operation 1h: Overall standby	Setting range: 0h to 1h
	[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communication block	Setting range: 0h to 1h
	[3:2]	0h			—	Set the default value.
	[4]	0h	Immediately	SLEEP	0h: Normal operation 1h: Low power consumption drive in exposure of global reset shutter operation	Setting range: 0h to 1h
	[7:5]	0h			—	Set the default value.
0001h	[0]	0h	Immediately	DCKRST	When changed from 0h to 1h: Fixes the LVDS clock output phase	Setting range: 0h to 1h After the fix, the value is automatically returned to 0h.
	[3:1]	0h			—	Set the default value.
	[4]	0h	Communication end frame *1	CLPSQRST	When changed from 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
	[7:5]	0h	Immediately		—	Set the default value.
0002h	[0]	0h	*1	SSBRK	When changed from 0h to 1h: Interrupt enable	Setting range: 0h to 1h After the interrupt, the value is automatically returned to 0h.
	[7:1]	00h			—	Set the default value.
0003h	[3:0]	3h	*1	STBLVDS	0h: 10 ch 1h: 8 ch 2h: 6 ch 3h: 4 ch 4h: 2 ch 5h: 1 ch Fh: All channel standby	Allowable setting values are 0h to 5h and Fh.
	[6:4]	3h	*1	CHSEL	Number of LVDS output 0h: 10 ch 1h: 8 ch 2h: 6 ch 3h: 4 ch 4h: 2 ch 5h: 1 ch	Setting range: 0h to 5h
	[7]	0h			—	Set the default value.
0004h	[7:0]	2Eh	*1	MDSEL1	Readout drive mode register 1	Set the value according to each readout mode register setting.
0005h	[7:0]	18h	*1	MDSEL2	Readout drive mode register 2	Set the value according to each readout mode register setting.
0006h	[7:0]	10h	*1	MDSEL3	Readout drive mode register 3	Set the value according to each readout mode register setting.
0007h	[7:0]	00h	*1	MDSEL4	Readout drive mode register 4	Set the value according to each readout mode register setting.
0008h	[0]	0h	*1	SMD	0h: Rolling shutter 1h: Global reset shutter	Setting range: 0h to 1h
	[3:1]	0h			—	Set the default value.
	[7:4]	0h	*1	GSVR	Specifies the vertical period to perform readout during global reset shutter drive	Setting range: 0h to Fh
0009h	[7:0]	000h	*1	PGC	Analog gain setting	Setting range: 0h to 7A5h
000Ah	[2:0]					
	[7:3]	00h			—	Set the default value.
000Bh	[7:0]	0007h	Next frame after communication end *2	SHR	Specifies the integration start horizontal period	Setting range is shown in ”Description of Registers”
000Ch	[7:0]					
000Dh	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0h to FFFFh
000Eh	[7:0]					
000Fh	[7:0]	0000h	*2	SPL	Specifies the integration start vertical period	Setting range: 0h to FFFFh
0010h	[7:0]					
0011h	[1:0]	0h	*1	DGAIN	Digital gain setting 0h: 0 dB gain setting value 1h: +6 dB gain setting value 2h: +12 dB gain setting value 3h: +18 dB gain setting value	Setting range: 0h to 3h
	[7:2]	00h			—	Set the default value.

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
001Ah	[0]	0h	*1	MDVREV	0h : Vertical direction normal readout 1h : Vertical direction inversion readout	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
0045h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 0h to FFh 10-bit readout mode : 1 digit/1h 12-bit readout mode : 4 digit/1h
0058h	[7:0]	36h	Immediately	PLSTMG11	Drive pulse timing setting 11	Set to 37h
005Ah	[7:0]	2Ah	Immediately	PLSTMG66	Drive pulse timing setting 66	Set to 2Bh
006Fh	[7:0]	000h	Immediately	VWINPOS	Start position of vertical arbitrary cropping (two's compliment)	Setting range is shown in "Description of Register"
0070h	[3:0]					
	[7:4]	0h			—	Set the default value.
0071h	[7:0]	0000h	Immediately	VWIDCUT	Width of vertical arbitrary cropping	Setting range is shown in "Description of Register"
0072h	[2:0]					
	[7:3]	0h			—	Set the default value.
0312h	[7:0]	12h	Immediately	PLSTMG16	Drive pulse timing setting 16	Set to 11h
0355h	[7:0]	01h	Immediately	PLSTMG85	Drive pulse timing setting 85	Set to 00h
0381h	[7:0]	01h	Immediately	PLSTMG17	Drive pulse timing setting 17	Set to 00h
052Eh	[7:0]	00h	Immediately	PLSTMG67	Drive pulse timing setting 67	Set to 02h
0530h	[7:0]	0Eh	Immediately	PLSTMG22	Drive pulse timing setting 22	Set to 0Bh
0531h	[7:0]	0Eh	Immediately	PLSTMG23	Drive pulse timing setting 23	Set to 0Bh
0532h	[7:0]	0Eh	Immediately	PLSTMG24	Drive pulse timing setting 24	Set to 0Bh
0533h	[7:0]	0Eh	Immediately	PLSTMG25	Drive pulse timing setting 25	Set to 0Bh
0534h	[7:0]	0Eh	Immediately	PLSTMG26	Drive pulse timing setting 26	Set to 0Bh
0535h	[7:0]	0Eh	Immediately	PLSTMG27	Drive pulse timing setting 27	Set to 0Bh
053Fh	[7:0]	1Ah	Immediately	PLSTMG34	Drive pulse timing setting 34	Set to 1Dh
0541h	[7:0]	1Eh	Immediately	PLSTMG36	Drive pulse timing setting 36	Set to 1Dh
0545h	[7:0]	01h	Immediately	PLSTMG37	Drive pulse timing setting 37	Set to 00h
0549h	[7:0]	04h	Immediately	PLSTMG62	Drive pulse timing setting 62	Set to 02h
054Bh	[7:0]	07h	Immediately	PLSTMG38	Drive pulse timing setting 38	Set to 00h
0555h	[7:0]	05h	Immediately	PLSTMG64	Drive pulse timing setting 64	Set to 02h
0563h	[7:0]	07h	Immediately	PLSTMG70	Drive pulse timing setting 70	Set to 05h
05A4h	[7:0]	0696h	Immediately	PLSTMG45	Drive pulse timing setting 45	Set to 0700h
05A5h	[7:0]					
05AAh	[7:0]	01h	Immediately	PLSTMG61	Drive pulse timing setting 61	Set to 00h
05D1h	[7:0]	18h	Immediately	PLSTMG46	Drive pulse timing setting 46	Set to 16h
05D2h	[7:0]	18h	Immediately	PLSTMG47	Drive pulse timing setting 47	Set to 15h
05D3h	[7:0]	16h	Immediately	PLSTMG48	Drive pulse timing setting 48	Set to 14h
065Ch	[7:0]	00h	Immediately	PLSTMG58	Drive pulse timing setting 58	Set to 01h
065Eh	[7:0]	1Ch	Immediately	PLSTMG63	Drive pulse timing setting 63	Set to 01h

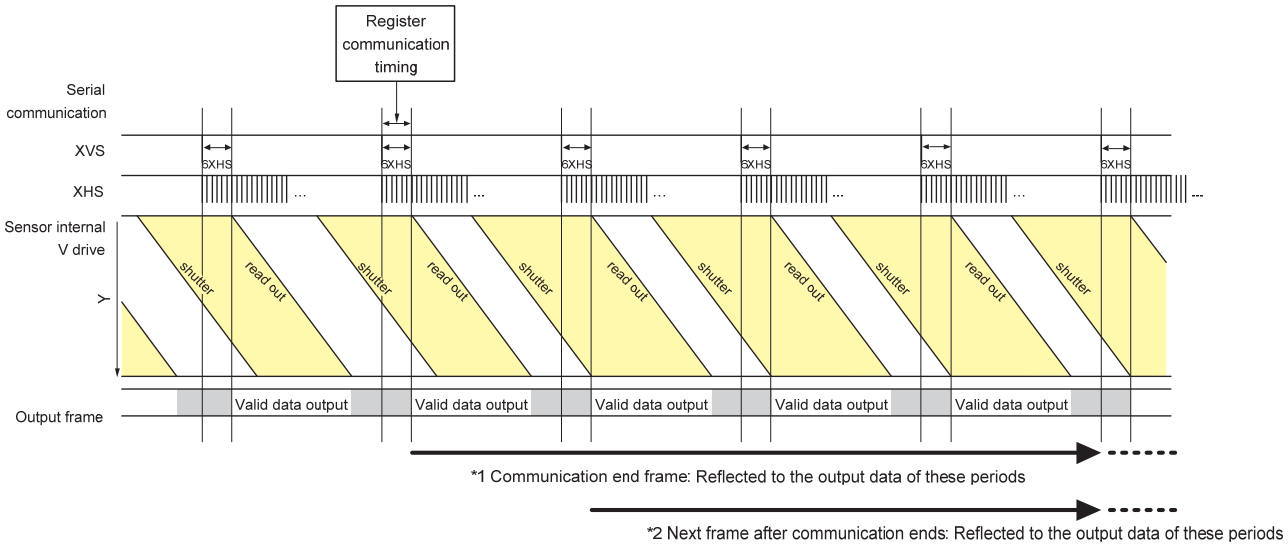
Note) • The "Default value" column indicates the initial value set in each register in the status before register communication is performed after start-up or after the reset signal XCLR is set to Low to reset the sensor.
• Operation is not guaranteed when using register settings other than noted in these specifications.
Do not access addresses not noted in the table above, and do not set register values other than those noted in "2. Description of Registers" on pages 29 to 39.
• When changing the mode, the address set designated in "3. Register Settings for Each Readout Drive Mode" on page 39 must be written.
• For the detailed reflection timing, see "1. Register Value Reflection Timing to Output Data" on page 28.

1. Register Value Reflection Timing to Output Data

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1. Communication end frame	The communication contents are reflected to the output data from the V period during which communication was performed.
*2. Next frame after communication end	The communication contents are reflected to the output data from the next V period after the V period during which communication was performed.

For which reflection timing of each register, see “Register Map” on pages 26 to 27.



2. Description of Register

Total Standby Control

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY (address 0000h, bit [0]) to “1h”.
(Standby mode is established immediately after reset.)
The serial communication block operates even in standby mode, so standby mode can be canceled by setting “0h” in the STANDBY register.

STANDBY Setting

Register value	Function
0h	Normal operation
1h	Overall standby

Digital Circuit Standby Control

Sensor digital circuit operation other than the serial communication block is stopped by setting the digital circuit standby control register STBLOGIC (address 0000h, bit [1]) to "1h". This register is valid only when STANDBY = 0h.
(Standby mode is established according to the STANDBY register initial value immediately after a reset.)
Set this register according to the recommended sequence during power-on or when canceling standby mode.

STBLOGIC Setting

Register value	Function
0h	Normal operation
1h	Digital circuit standby other than serial communications block

LVDS Clock Output Phase Fixed

The clock phase relative to the sync code start data in the LVDS data output is fixed by the LVDS clock output phase fixing register DCKRST (address 0001h, bit [0]). Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the phase fixing process, so there is no need to write “0h”.

DCKRST Operation Setting

Register value	Function
Changed from 0h to 1h	Fixes the LVDS clock output phase

Clamp Reset

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST (address 0001h, bit [4]). Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the reset process, so there is no need to write “0h”.

CLPSQRS Operation Setting

Register value	Function
Changed from 0h to 1h	Resets the internal clamp circuit operation status

Break Mode

In rolling shutter (normal shutter) operating mode (address 0008h, bit [0], SMD = 0h), XVS can be subsampled according to SVR.
In addition, in global reset shutter operating mode (SMD = 1h), XVS can be subsampled according to SVR during the exposure period, and then according to GSVR during the readout period.
This XVS subsampling operation can be stopped and then restarted from the start of the exposure period using the break mode register SSBRK (address 0002h, bit [0]).
This register automatically returns to “0h” after the break process, so there is no need to write “0h”.

SSBRK Setting

Register value	Function
Changed from 0h to 1h	Interrupt enable

subLVDS Standby Control

This sensor can set the subLVDS to standby mode according to the setting value by setting the subLVDS standby control register STBLVDS (address 0003h, bit [3:0]).

STBLVDS Setting

Register value	Function
0h	10 ch
1h	8 ch
2h	6 ch
3h	4 ch
4h	2 ch
5h	1 ch
Fh	All channel standby

subLVDS standby control is shown below.

dec	bin	hex	Function	DO0	DO1	DO2	DO3	DO4	DCK	DO5	DO6	DO7	DO8	DO9
STBLVDS[3:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	STBY	Active	Active	Active	STBY	Active	Active	Active
2d	0010b	2h	6 ch	STBY	Active	Active	STBY	Active	Active	Active	STBY	Active	Active	STBY
3d	0011b	3h	4 ch	STBY	STBY	Active	STBY	Active	Active	Active	STBY	Active	STBY	STBY
4d	0100b	4h	2 ch	STBY	STBY	STBY	STBY	Active	Active	Active	STBY	STBY	STBY	STBY
5d	0101b	5h	1 ch	STBY	STBY	STBY	STBY	Active	Active	STBY	STBY	STBY	STBY	STBY
15d	1111b	Fh	All Standby	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY

Number of LVDS Output Channels Selection

This sensor can set the number of output channels according to the setting value by setting the number of LVDS output channels selection register CHSEL (address 0003h, bit [6:4]).

CHSEL Setting

Register value	Function
0h	10 ch
1h	8 ch
2h	6 ch
3h	4 ch
4h	2 ch
5h	1 ch

Number of LVDS channels control is shown below.

dec	bin	hex	Function	DO0	DO1	DO2	DO3	DO4	DCK	DO5	DO6	DO7	DO8	DO9
CHSEL[2:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Active	Active
2d	0010b	2h	6 ch	Fixed Low	Active	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Active	Fixed Low
3d	0011b	3h	4 ch	Fixed Low	Fixed Low	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Fixed Low	Fixed Low
4d	0100b	4h	2 ch	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Active	Active	Active	Fixed Low	Fixed Low	Fixed Low	Fixed Low
5d	0101b	5h	1 ch	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Active	Active	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Fixed Low

Electronic Shutter Timing

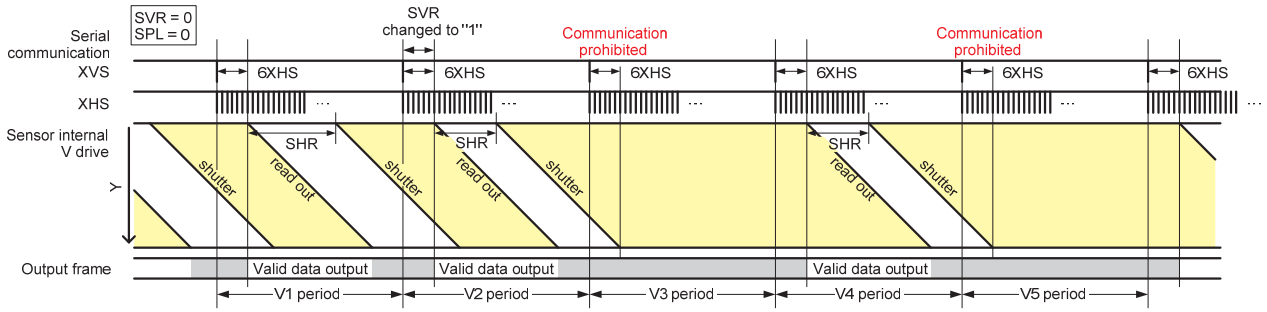
The exposure start timing can be designated by setting the electronic shutter timing register SHR (address 000Bh, bit [7:0] and address 000Ch, bit [7:0]). Designate the lower 8 bits in address 000Bh and the upper 8 bits in address 000Ch, for a total of 16 bits.
Note that this setting value unit is 1XHS period regardless of the readout drive mode. In addition, the vertical sync signal XVS can be subsampled inside the sensor according to the SVR register (address 000Dh, bit [7:0] and address 000Eh, bit [7:0]). The vertical sync signal period inside the sensor is (SVR + 1).
When setting the electronic shutter during the vertical sync signal subsampling period, the SPL register (address 000Fh, bit [7:0] and address 0010h, bit [7:0]) is available.

Shutter Setting

<table>
<tr><th>Register</th><th colspan="2">Register value</th><th>Function</th></tr>
<tr><td rowspan="6">SHR</td><td>8 to {(SVR + 1) × Number of XHS pulses per frame – 4}</td><td>Readout mode No.0, 1
All-pixel scan mode (12 bit/10 bit)</td><td rowspan="6">Specifies the integration start horizontal period</td></tr>
<tr><td>10 to {(SVR + 1) × Number of XHS pulses per frame – 4}</td><td>Readout mode No.2, 2A, 7
Horizontal/vertical 2/2-line binning mode (Horizontal and vertical weighted binning)
Vertical 2 binning horizontal 2/4 subsampling mode (Vertical weighted 2 binning)</td></tr>
<tr><td>15 to {(SVR + 1) × Number of XHS pulses per frame – 8}</td><td>Readout mode No.3
Horizontal/vertical 3/3-line binning mode</td></tr>
<tr><td>4 to {(SVR + 1) × Number of XHS pulses per frame – 2}</td><td>Readout mode No. 4, 6
Vertical 2/9 subsampling binning horizontal 3 binning mode
Vertical 2/19 subsampling binning horizontal 3 binning mode</td></tr>
<tr><td>4 to {(SVR + 1) × Number of XHS pulses per frame /4 – 2}</td><td>Readout mode No.5
Vertical 2/9 subsampling binning horizontal 3 binning mode (low power consumption drive)</td></tr>
<tr><td>0 to {(SVR + 1) × Number of XHS pulses per frame – 130}</td><td>Global reset shutter mode (SMD = 1)</td></tr>
<tr><td>SVR</td><td colspan="2">0h to FFFFh *Note 2.</td><td>Specifies the integration shutdown vertical period</td></tr>
<tr><td>SPL</td><td colspan="2">0h to FFFFh *Note 2.</td><td>Specifies the integration start vertical period</td></tr>
</table>

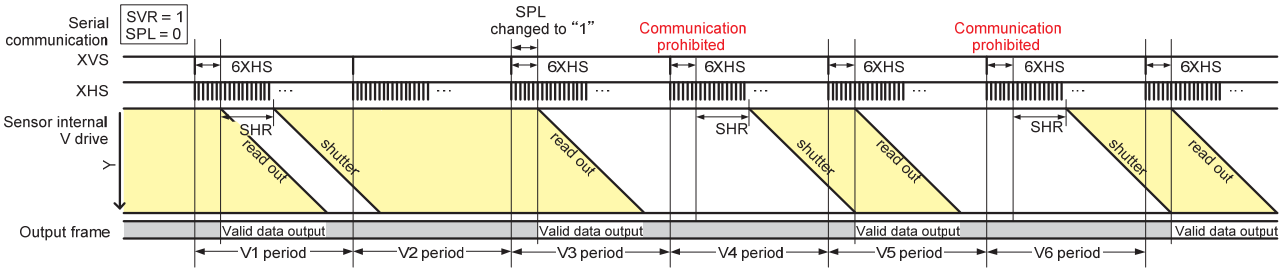
Note) 1. See “Integration Time in Each Readout Drive Mode” on page 63 for the integration time calculation formula.
2. The SVR and SPL register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 0008h, bit [0]).

Example of Electronic Shutter Operation 1



Example of SVR operation

Example of Electronic Shutter Operation 2



Example of SVR and SPL operation

Note) In vertical sync signal subsampling periods (Electronic Shutter Operation Example 1: V3 and V5 periods, Electronic Shutter Operation Example 2: V4 and V6 periods), communication is prohibited during the normal communication period (the 6XHS period after the vertical sync signal XVS is input), except in the following case.

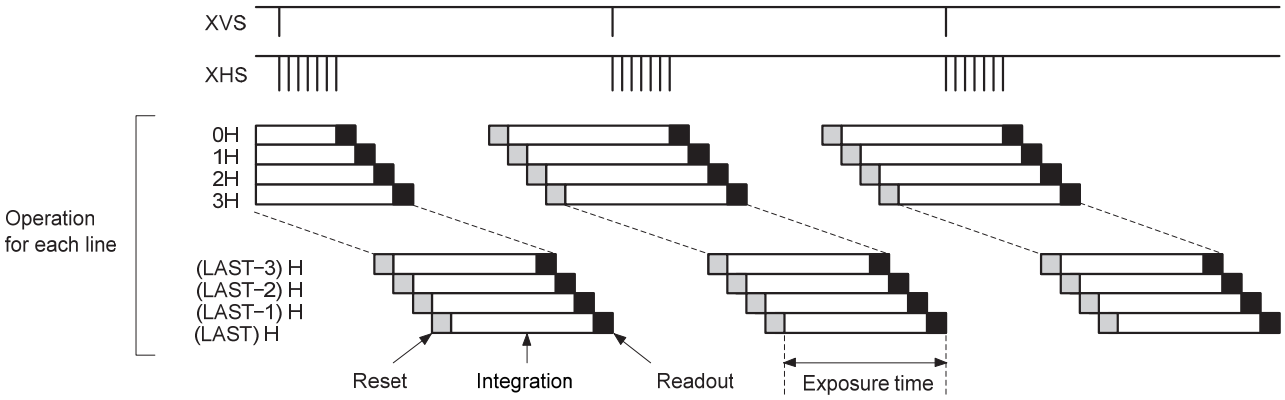
- When stopping vertical sync signal subsampling using the break mode register SSBRK.

Electronic Shutter Drive Mode

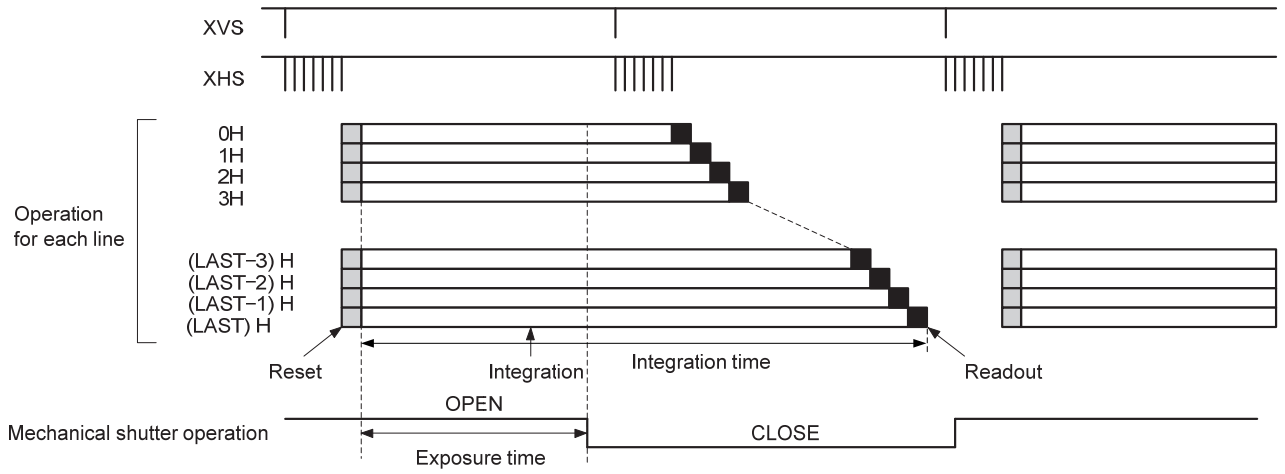
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD (address 0008h, bit [0]). Rolling shutter operation performs pixel reset and integration sequentially in line units in sync with the XHS signal. Global reset shutter operation resets all pixels at once and then starts integration after that.
("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.)
The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.

SMD Setting

Register value	Function
0h	Rolling shutter (normal shutter mode)
1h	Global reset shutter



Rolling Shutter Operation



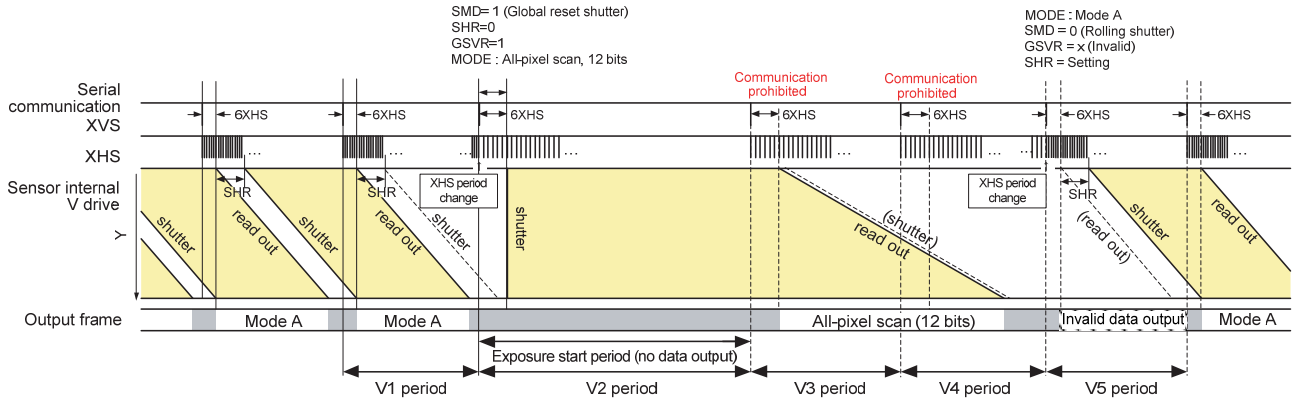
Global Reset Shutter Operation

Readout Timing

The vertical sync signal XVS can be subsampled inside the sensor during the readout period (V3 and V4 periods) in global reset shutter drive mode (address 0008h, bit [0], SMD = 1h) by setting the readout timing register GSVR (address 0008h, bit [7:4]).
This is the same operation as that performed by the SVR register (address 000Dh, bit [7:0] and address 000Eh, bit [7:0]). However, separate control is performed in global reset shutter drive mode (SMD = 1h), with the SVR register designating the vertical period of the exposure period (V2 period), and the GSVR register designating the vertical period of the readout period (V3 and V4 periods). This register is invalid in rolling shutter drive mode (SMD = 0h).

GSVR Setting

Register value	Function
0h to Fh	Specifies the vertical period for reading during global reset shutter drive.



Example of GSVR operation

Analog Gain

The analog gain value can be set by setting the analog gain register PGC (address 0009h, bit [7:0] and address 000Ah, bit [2:0]). Set the lower 8 bits in address 0009h and the upper 3 bits in address 000Ah, for a total of 11 bits.

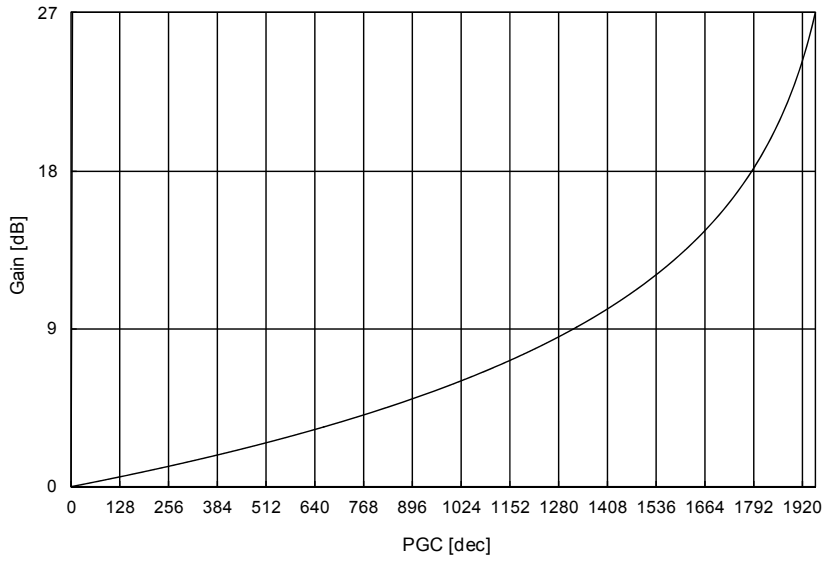
PGC Setting

Register value	Function
0h to 7A5h (0d to 1957d)	Analog gain setting

In addition, the figure below shows the relationship between the register setting value and the set gain value. When the register setting value is “0h (0d) ”, the gain value is 0 dB (minimum settable value), and when “7A5h (1957d) ”, the gain value is approximately 27 dB (maximum settable value).

Relational Formula

Gain [dB] = –20 log{(2048 – PGC [10:0])/2048}



Relationship between Register Setting Value and Set Gain Value

Digital Gain

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN (address 0011h, bit [1:0]).

DGAIN Setting

Register value	Function
0h	Digital gain setting value = 0 dB
1h	Digital gain setting value = +6 dB
2h	Digital gain setting value = +12 dB
3h	Digital gain setting value = +18 dB

Vertical Direction Readout Inversion

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV (address 001Ah, bit [0]).

MDVREV Setting

Register value	Function
0h	Vertical direction normal readout
1h	Vertical direction inversion readout

Digital Black Level Offset

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL (address 0045h, bit [7:0]).
Note that the offset unit changes according to the readout drive mode.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits.

BLKLEVEL Setting

Register value	Function
0h to FFh	Digital black level offset setting

Readout Drive Mode

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL1 to MDSEL4. When changing the mode, make the setting according to “3. Register Settings for Each Readout Drive Mode” on page 39.

Low Power Consumption Drive In Exposure of Global Reset Shutter Operation

Low power consumption drive can be used when exposing of global reset shutter operation by the register SLEEP. When using low power consumption drive in exposure of global reset shutter operation, make the setting according to “low power consumption drive in exposure of global reset shutter operation” on page 67.

Vertical Arbitrary Cropping

By setting VWIDCUT, VWINPOS, MDSEL3 and MDSEL4 the registers of vertical arbitrary cropping, arbitrary cropping in vertical direction can be performed in all-pixel scan mode (10bits). See “Vertical Arbitrary Cropping (All-pixel scan 10 bit)” on pages 59 to 62 for details.

Readout Drive Pulse Timing

The drive pulse timing is set by readout drive pulse timing registers PLSTMG.

PLSTMG Setting

Address	Bit assignment	Default value	Register name	Register Value
0058h	[7:0]	36h	PLSTMG11	Set to 37h
005Ah	[7:0]	2Ah	PLSTMG66	Set to 2Bh
0312h	[7:0]	12h	PLSTMG16	Set to 11h
0355h	[7:0]	01h	PLSTMG85	Set to 00h
0381h	[7:0]	01h	PLSTMG17	Set to 00h
052Eh	[7:0]	00h	PLSTMG67	Set to 02h
0530h	[7:0]	0Eh	PLSTMG22	Set to 0Bh
0531h	[7:0]	0Eh	PLSTMG23	Set to 0Bh
0532h	[7:0]	0Eh	PLSTMG24	Set to 0Bh
0533h	[7:0]	0Eh	PLSTMG25	Set to 0Bh
0534h	[7:0]	0Eh	PLSTMG26	Set to 0Bh
0535h	[7:0]	0Eh	PLSTMG27	Set to 0Bh
053Fh	[7:0]	1Ah	PLSTMG34	Set to 1Dh
0541h	[7:0]	1Eh	PLSTMG36	Set to 1Dh
0545h	[7:0]	01h	PLSTMG37	Set to 00h
0549h	[7:0]	04h	PLSTMG62	Set to 02h
054Bh	[7:0]	07h	PLSTMG38	Set to 00h
0555h	[7:0]	05h	PLSTMG64	Set to 02h
0563h	[7:0]	07h	PLSTMG70	Set to 05h
05A4h	[7:0]	0696h	PLSTMG45	Set to 0700h
05A5h	[7:0]			
05AAh	[7:0]	01h	PLSTMG61	Set to 00h
05D1h	[7:0]	18h	PLSTMG46	Set to 16h
05D2h	[7:0]	18h	PLSTMG47	Set to 15h
05D3h	[7:0]	16h	PLSTMG48	Set to 14h
065Ch	[7:0]	00h	PLSTMG58	Set to 01h
065Eh	[7:0]	1Ch	PLSTMG63	Set to 01h

3. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below.

3-1. When Using Type 1 Approx. 20.48 M Pixels (3:2)

Description of Register Setting for Each Readout Drive Mode

Address	Bit assign-ment	Register name	Readout mode No.[*2]								
			0	1	2	2A	3	4	5	6	7
0003h	[3:0]	STBLVDS	0h	0h	2h	2h	3h	2h	4h	1h	2h
	[6:4]	CHSEL	0h	0h	2h	2h	3h	2h	4h	1h	2h
	[7]		00h								
0004h	[7:0]	MDSEL1	00h	00h	1Dh	19h	2Eh	35h	40h	49h	20h
0005h	[7:0]	MDSEL2	03h	01h	11h	11h	18h	18h	18h	18h	21h
0006h	[7:0]	MDSEL3	10h	00h	50h	50h	10h	10h	93h	10h	00h
0007h	[7:0]	MDSEL4	00h	00h	00h	00h	00h	00h	05h	00h	09h
0008h	[0]	SMD	0h[*1]	0h[*1]	0h	0h	0h	0h	0h	0h	0h
	[3:1]		0h								
	[7:4]	GSVR	[*3]		(invalid)						
000Dh	[7:0]	SVR	According to exposure time						Multiple of 8 − 1	According to exposure time	
000Eh	[7:0]										
001Ah	[0]	MDVREV	Vertical direction 0h: normal/1h:inverted								
	[7:1]		00h								

[*1] Can be used in combination with global reset shutter (address 0008h, bit [0], when SMD = 1h)

[*2] See “1. Readout Drive Modes” on page 40 for details of readout mode No.

[*3] Specifies the vertical period for reading during global reset shutter drive. (0h to Fh)

3-2. When Using Type 1/1.4 Approx. 9.03 M Pixels (Approx. 17:9)

Description of Register Setting for Each Readout Drive Mode

Address	Bit assign-ment	Register name	Readout mode No.[*2]
			1
0003h	[3:0]	STBLVDS	0h
	[6:4]	CHSEL	0h
	[7]		00h
0004h	[7:0]	MDSEL1	54h
0005h	[7:0]	MDSEL2	41h
0006h	[7:0]	MDSEL3	00h
0007h	[7:0]	MDSEL4	00h
0008h	[0]	SMD	0h[*1]
	[3:1]		0h
	[7:4]	GSVR	[*3]
000Dh	[7:0]	SVR	According to exposure time
000Eh	[7:0]		
001Ah	[0]	MDVREV	vertical direction 0h: normal/1h:inverted
	[7:1]		00h

[*1] Can be used in combination with global reset shutter (address 0008h, bit [0], when SMD = 1h)

[*2] See “1. Readout Drive Modes” on page 40 for details of readout mode No.

[*3] Specifies the vertical period for reading during global reset shutter drive. (0h to Fh)

Readout Drive Modes

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.
All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).
Note that some readout drive modes need different (1) register settings and (2) vertical front blanking when vertical readout direction is normal and inverted.
See “3. Register Setting for Each Readout Drive Mode” on page 39 for the register setting, and “Minimum Vertical Operation Period in Each Readout Drive Mode” on pages 46 and 57, and “Image Data Output Format” on pages 48 to 56 and 58 for the vertical front blanking.

1-1. Description of Readout Drive Modes

(1) When Using Type 1 Approx. 20.48 M Pixels (3:2)

Readout mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12 bits)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (10 bits)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2	Horizontal/vertical 2/2-line binning 16:9 cropping (horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels (16:9 cropping) (See the image of binning on page 41.)
2A	Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)	Horizontal and vertical direction 2-line weighted binning readout of pixels (See the image of binning on page 41.)
3	Horizontal/vertical 3/3-line binning	Horizontal and vertical direction 3-line binning readout of pixels (See the image of binning on page 41.)
4	Vertical 2/9 subsampling binning horizontal 3 binning cropping	2 of every 9 lines in the vertical direction at the all-pixel scan area (cropping) are added. Then, 3 pixels in the horizontal direction are added and output. (See the image of binning on page 42.)
5	Vertical 2/9 subsampling binning horizontal 3 binning low power consumption drive	2 of every 9 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels in the horizontal direction are added and output. (See the image of binning on page 42.)
6	Vertical 2/19 subsampling binning horizontal 3 binning	2 of every 19 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels in the horizontal direction are added and output. (See the image of binning on page 42.)
7	Vertical 2 binning horizontal 2/4 subsampling 16:9 cropping (Vertical weighted 2 binning)	Add 2 lines with weighting in the vertical direction at the all-pixel scan area (16:9 cropping) and 2 of every 4 lines in the horizontal direction are output. (See the image of binning on page 42.)

(2) When Using Type 1/1.4 Approx. 9.03 M Pixels (Approx. 17:9)

Readout mode No.	Readout drive mode	Mode description
1	All-pixel scan mode (10 bits)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.

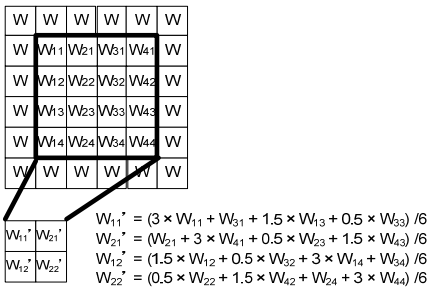
1-2. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.
Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits, so the weight of 1 digit is 4 times greater than that during 12-bit output.

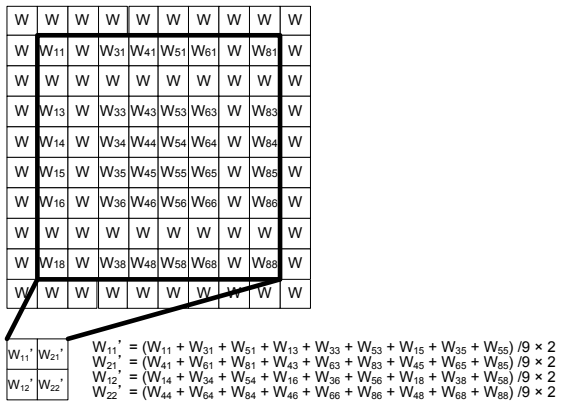
Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Horizontal pixel processing	Vertical pixel processing	Total number of binning pixels	Internal arithmetic processing	Number of output bits
0	12 bits	—	—	—	—	10 bits + 2 bits *1
1	10 bits	—	—	—	—	10 bits
2	10 bits	2 binning	2 binning	4 pixels	3/6, 1.5/6, 1/6, 0.5/6 (weighted binning*3)	10 bits + 2 bits *2
2A	10 bits	2 binning	2 binning	4 pixels	3/6, 1.5/6, 1/6, 0.5/6 (weighted binning*3)	10 bits + 2 bits *2
3	9 bits	3 binning	3 binning	9 pixels	2/9	10 bits + 2 bits *2
4	9 bits	3 binning	2/9 subsampling binning	6 pixels	1/3	10 bits + 2 bits *2
5	9 bits	3 binning	2/9 subsampling binning	6 pixels	1/3	10 bits + 2 bits *2
6	9 bits	3 binning	2/19 subsampling binning	6 pixels	1/3	10 bits + 2 bits *2
7	10 bits	2/4 subsampling	2 binning	2 pixels	3/4, 1/4 (weighted binning*3)	10 bits

*1 A/D conversion is performed with a resolution 4 times that of 10-bit A/D conversion, and the results are output in 12 bits regarded as a 10-bit integer item and a 2-bit decimal item.
*2 Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.
*3 See pages 41 to 42 “Binning Image” for details of weighted binning.

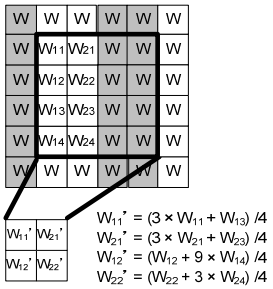


Horizontal/Vertical 2/2-line Binning (horizontal and vertical weighted binning) Binning Image

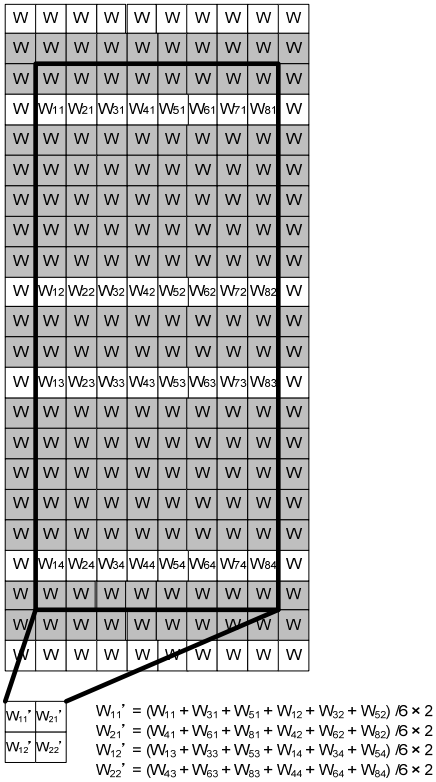


Horizontal/Vertical 3/3-line Binning Binning Image

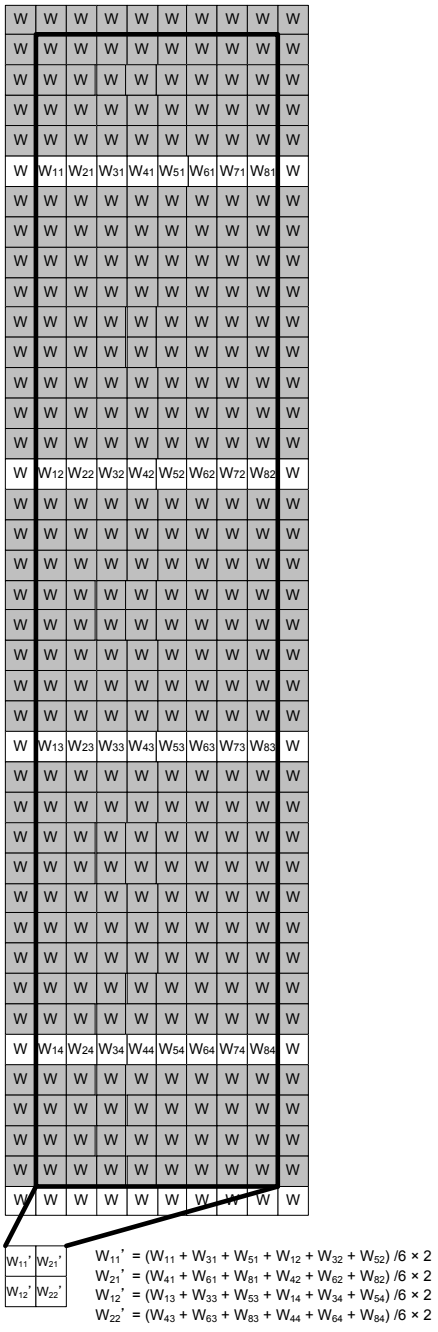
Note) Gray diagram indicate pixels which are not read out.



Vertical 2 Binning
Horizontal 2/4 Subsampling
(Vertical Weighted Binning)
Binning Image



Vertical 2/9 Subsampling Horizontal
3 Binning
Binning Image

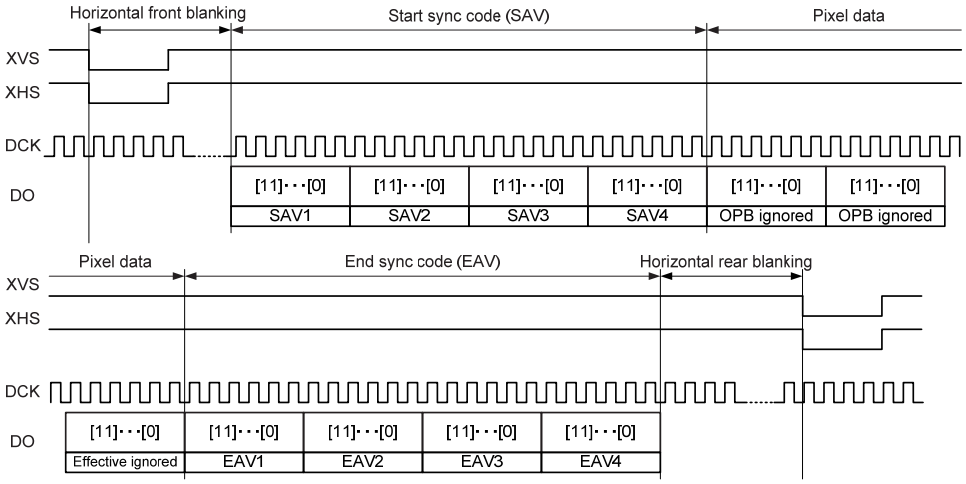


Vertical 2/19 Subsampling Horizontal
3 binning
Binning Image

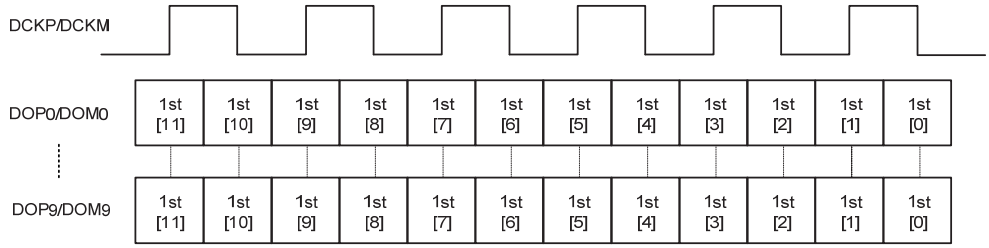
Note) Gray diagram indicate pixels which are not read out.

2. Sync Signals and Data Output Timing

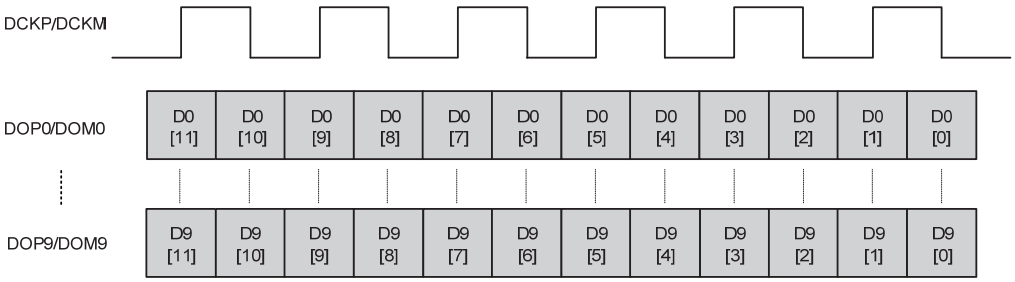
The figure below shows the sync signal and data output timing during 12-bit length serial output for this sensor.
The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals. Timing control is performed at the falling edge of both the XVS and XHS signals. The data is output in order from the start sync code (SAV) after the horizontal front blanking period after the falling edge.
See “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages 46 and 57 for the detailed blanking length and number of OPB pixels. The length of horizontal front blanking pixels varies greatly according to the mode as described in “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages 46 and 57, so using the sync code as the trigger is recommended for the recording pixel start timing.
The sync code details are shown below.
In addition, the length of horizontal rear blanking changes when the XHS period is changed.



Sync Signal and Data Output Timing



Serial Data Details (Sync Code Block)



Serial Data Details (Pixel Data Block)

Sync code details

LVDS output bit No.		Sync code (4 words)				
12-bit output	10-bit output	1st word	2nd word	3rd word	4th word	
11	9	1	0	0	1	
10	8	1	0	0	0	
9	7	1	0	0	V	1: Blanking line 0: Except blanking line
8	6	1	0	0	H	1: End sync code 0: Start sync code
7	5	1	0	0	P3	Protection bits
6	4	1	0	0	P2	
5	3	1	0	0	P1	
4	2	1	0	0	P0	
3	1	1	0	0	0	
2	0	1	0	0	0	
1	—	1	0	0	0	
0	—	1	0	0	0	

		Protection bits			
V	H	P3	P2	P1	P0
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

Sync code details (hexadecimal notation) 12-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	FFFh	000h	000h	AB0h
	End sync code (EAV)				B60h
Except blanking line	Start sync code (SAV)				800h
	End sync code (EAV)				9D0h

Sync code details (hexadecimal notation) 10-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	3FFh	000h	000h	2ACh
	End sync code (EAV)				2D8h
Except blanking line	Start sync code (SAV)				200h
	End sync code (EAV)				274h

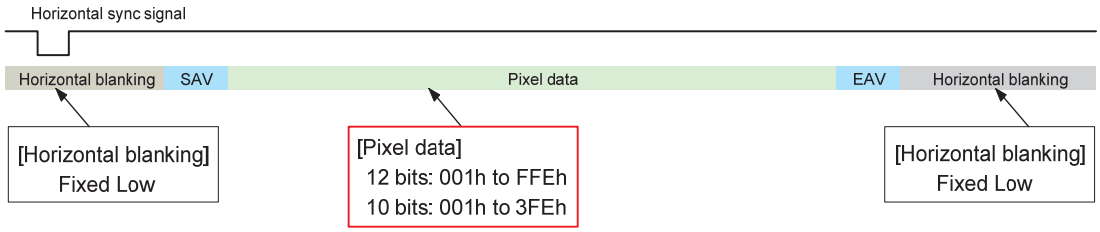
3. Output Range of LVDS Output Data

The table below shows the decimal point position, output bit length and output range of the output data in each readout mode. Note that the value of the first word of the sync code (3FFh, FFFh) and the maximum data value do not overlap in any readout mode.

Data output range in each readout mode

Readout mode No.	LVDS output		
	Decimal point position	Output bit length [bit]	Output range [hex]
0	2	12	001h to FFEh
1	0	10	001h to 3FEh
2	2	12	001h to FFEh
2A	2	12	001h to FFEh
3	2	12	001h to FFEh
4	2	12	001h to FFEh
5	2	12	001h to FFEh
6	2	12	001h to FFEh
7	0	10	001h to 3FEh

Output value during horizontal blanking period is fixed to Low (all 0).



Readout Drive Timing

4. Detailed Specification of Each Mode

4-1. When Using Type 1 Approx. 20.48 M Pixels (3:2)

(1) Horizontal/Vertical Operation Period in Each Readout Drive Mode

Minimum Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Data rate [MHz]	Horizontal front blanking [DCK] *2 *3	Horizontal operation period (Number of pixels conversion)					XHS Minimum period [INCK] *2.
			Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
0	576 (288DDR*1)	400 to 405	96	36	5472	36	0	861
1	576 (288DDR*1)	400 to 405	96	36	5472	36	0	720
2	576 (288DDR*1)	408 to 413	48	18	2736	18	0	362
2A	576 (288DDR*1)	408 to 413	48	18	2736	18	0	362
3	576 (288DDR*1)	406 to 411	32	12	1824	12	0	284
4	576 (288DDR*1)	408 to 413	32	12	1824	12	0	360
5	576 (288DDR*1)	406 to 411	32	12	1824	12	0	284
6	576 (288DDR*1)	408 to 413	32	12	1824	12	0	360
7	576 (288DDR*1)	400 to 405	48	18	2736	6	0	364

*1 DDR : Double Data Rate
*2 If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.
*3 Number of LVDS output signal DCK clock

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						XVS minimum period [XHS]
	Vertical front blanking	Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
0	17*1 16*2	16	24	3648	22	0	3728
1	17*1 16*2	16	24	3648	22	0	3728
2	9 (20XHS)	4	10	1538	8	0	3141
2A	9 (20XHS)	4	10	1824	8	0	3713
3	9 (29XHS)	4	10	1216	8	0	3744
4	7 (16XHS)	4	4	370	4	0	781
5	5 (42XHS)	4	4	404	4	0	843
6	7 (16XHS)	4	4	190	4	0	421
7	9 (19XHS)	4	10	1538	8	0	3140

*1 When vertical direction normal readout
*2 When vertical direction inverted readout

(2) NTSC/PAL Compatible Drive

This sensor can be used with a frame frequency that supports NTSC or PAL by using the recommended horizontal operating period (XHS period) and recommended vertical operating period (V period) for each readout drive mode shown in the table below. Note that the number of XHS pulses input within the horizontal operating period (H period) varies according to the drive mode.

Recommended H Period and V Periods (NTSC/PAL Compatible)

Readout mode No	NTSC compatible drive				PAL compatible drive			
	XHS period (INCK) *1	H period (number of XHS pulses) *2	V period (number of XHS pulses)	Frame frequency [frame/s]	XHS period (INCK) *1	H period (number of XHS pulses) *2	V period (number of XHS pulses)	Frame frequency [frame/s]
0	876	1	3739	21.98	900	1	4000	20.00
1	728	1	3960	24.98	720	1	4000	25.00
2	364	2	3300	59.94	375	2	3840	50.00
2A	364	2	3960	49.95	375	2	3840	50.00
3	312	3	3850	59.94	320	3	4500	50.00
4	364	2	825	239.76	375	2	960	200.00
5	308	8	7800	29.97	320	8	9000	25.00
6	364	2	440	449.55	375	2	480	400.00
7	364	2	3300	59.94	375	2	3840	50.00

*1 Number of clocks in conversion of INCK = 72 MHz
*2 Number of XHS pulses required to output the data for one sensor line

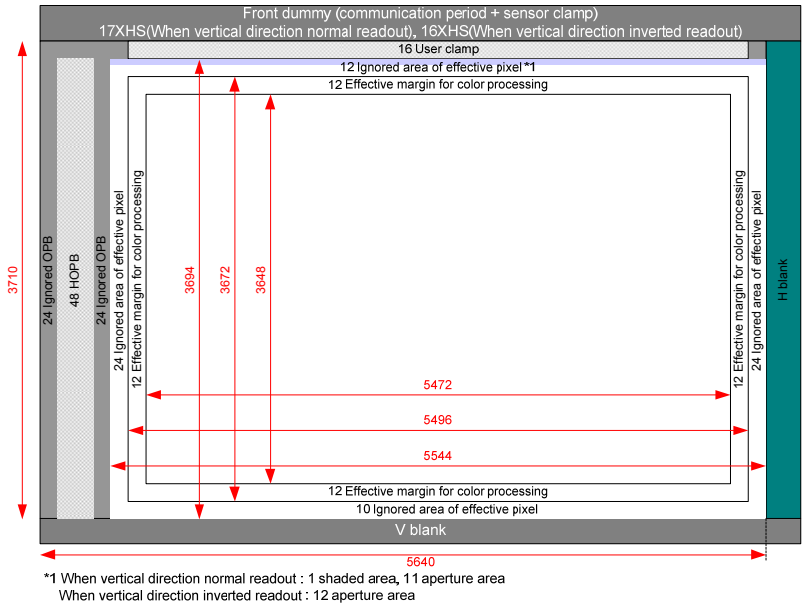
Imaging Conditions in Each Readout Drive Mode (NTSC/PAL Compatible Drive)

Readout mode No	Imaging conditions						
	Data rate [MHz]	Number of LVDS output channels [ch]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	576 (288DDR)	10	12	12	5472	3648	Approximately 19.96 M Pixels
1	576 (288DDR)	10	10	10	5472	3648	Approximately 19.96 M Pixels
2	576 (288DDR)	6	10	12	2736	1538	Approximately 4.21 M Pixels
2A	576 (288DDR)	6	10	12	2736	1824	Approximately 4.99 M Pixels
3	576 (288DDR)	4	9	12	1824	1216	Approximately 2.22 M Pixels
4	576 (288DDR)	6	9	12	1824	370	Approximately 0.67 M Pixels
5	576 (288DDR)	2	9	12	1824	404	Approximately 0.74 M Pixels
6	576 (288DDR)	8	9	12	1824	190	Approximately 0.35 M Pixels
7	576 (288DDR)	6	10	10	2736	1538	Approximately 4.21 M Pixels

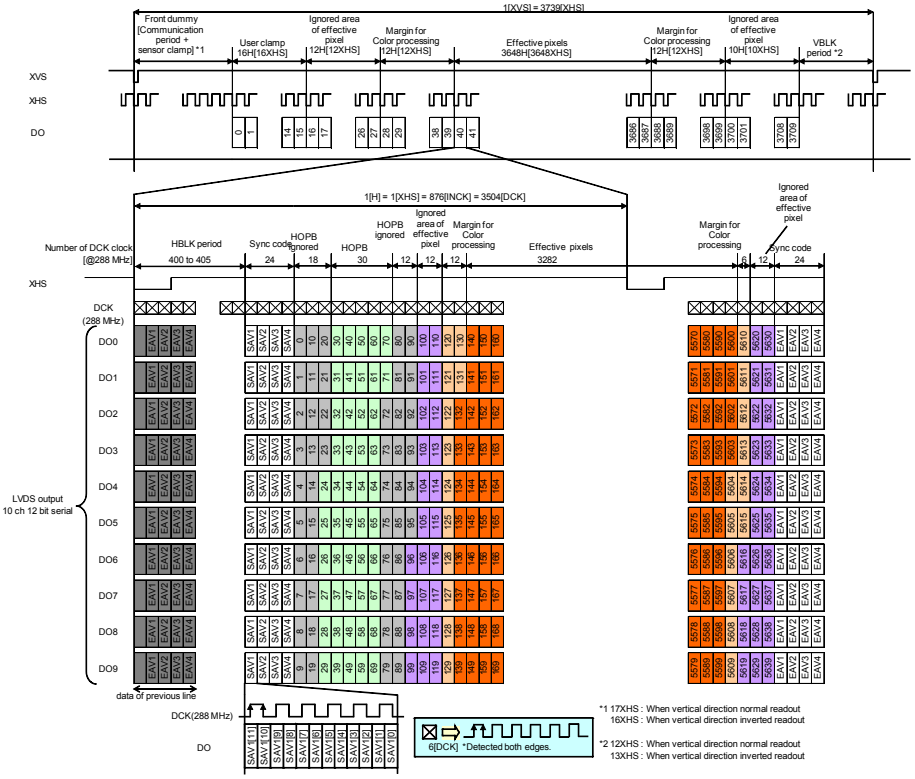
(3) Image Data Output Format

The output format in each readout drive mode is as follows.

MODE0: All-pixel scan mode (21.98 frame/s, 12-bit A/D conversion, 12-bit length output)

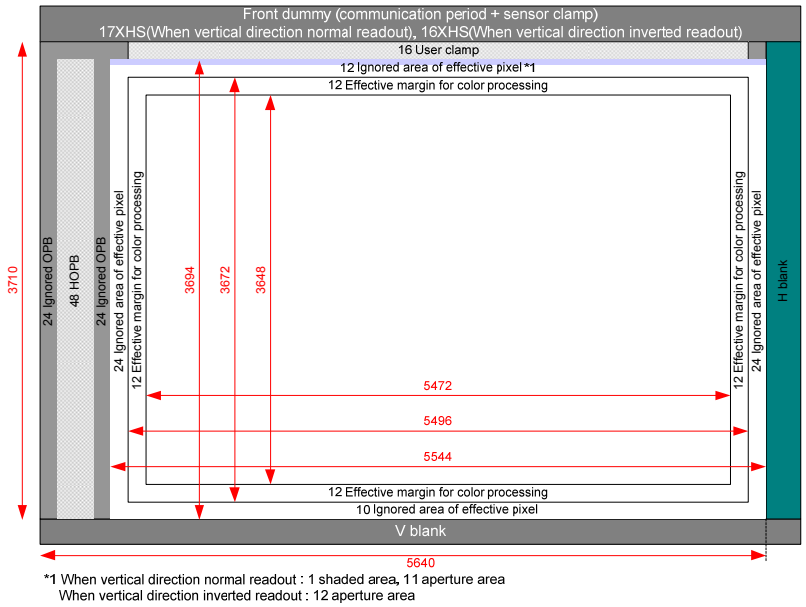


Readout Pixel Image Diagram (5472 × 3648)

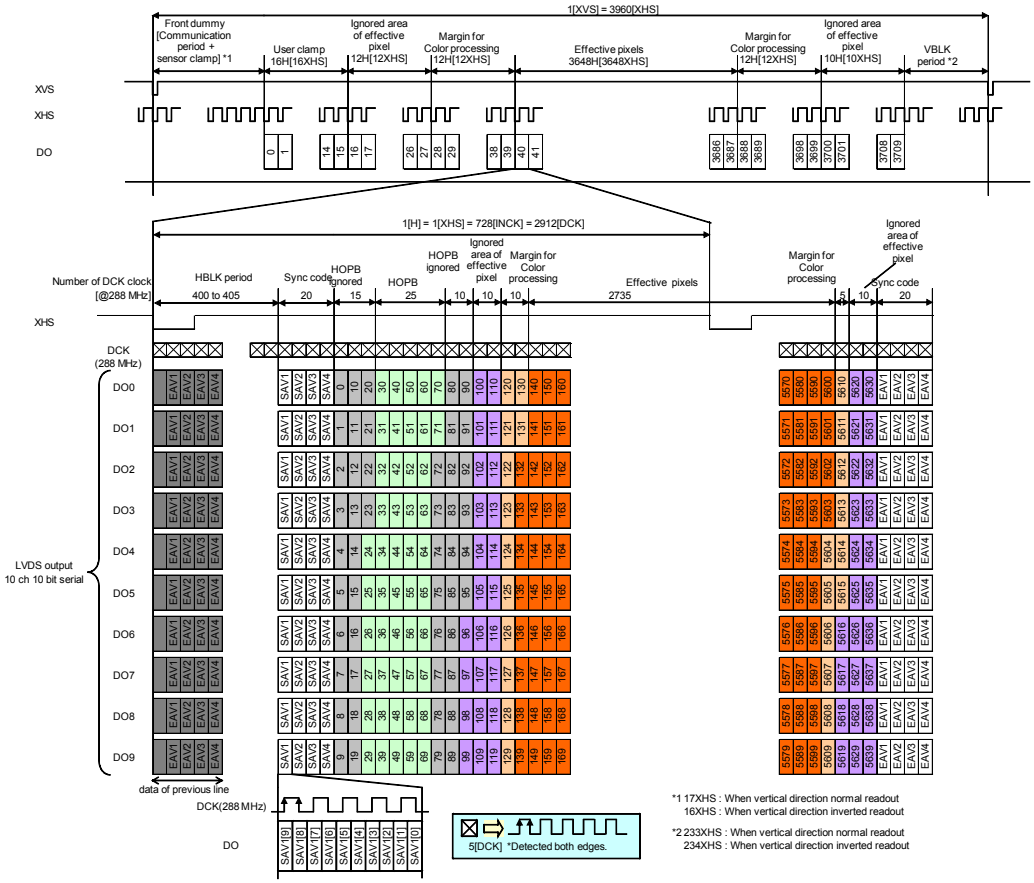


Readout Drive Timing

MODE1: All-pixel scan mode (24.98 frame/s, 10-bit A/D conversion, 10-bit length output)

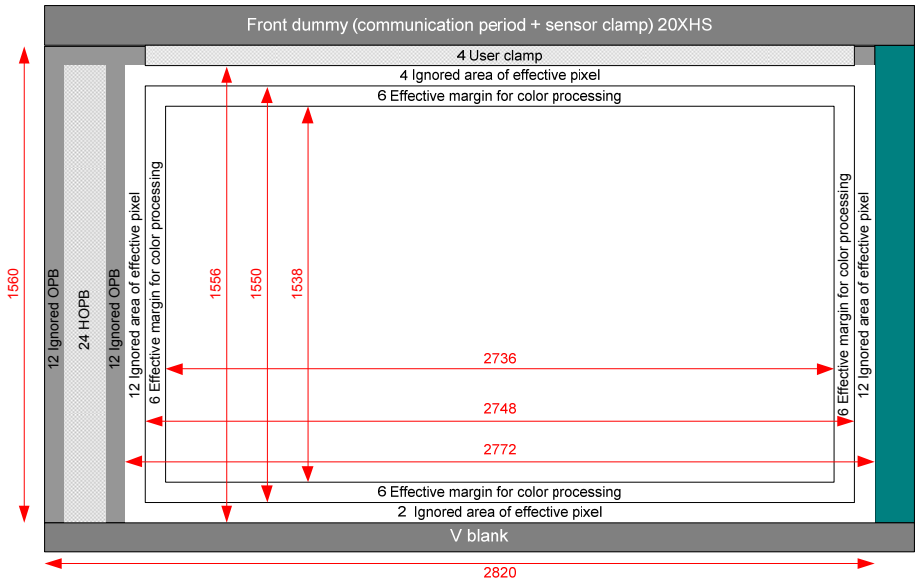


Readout Pixel Image Diagram (5472 × 3648)

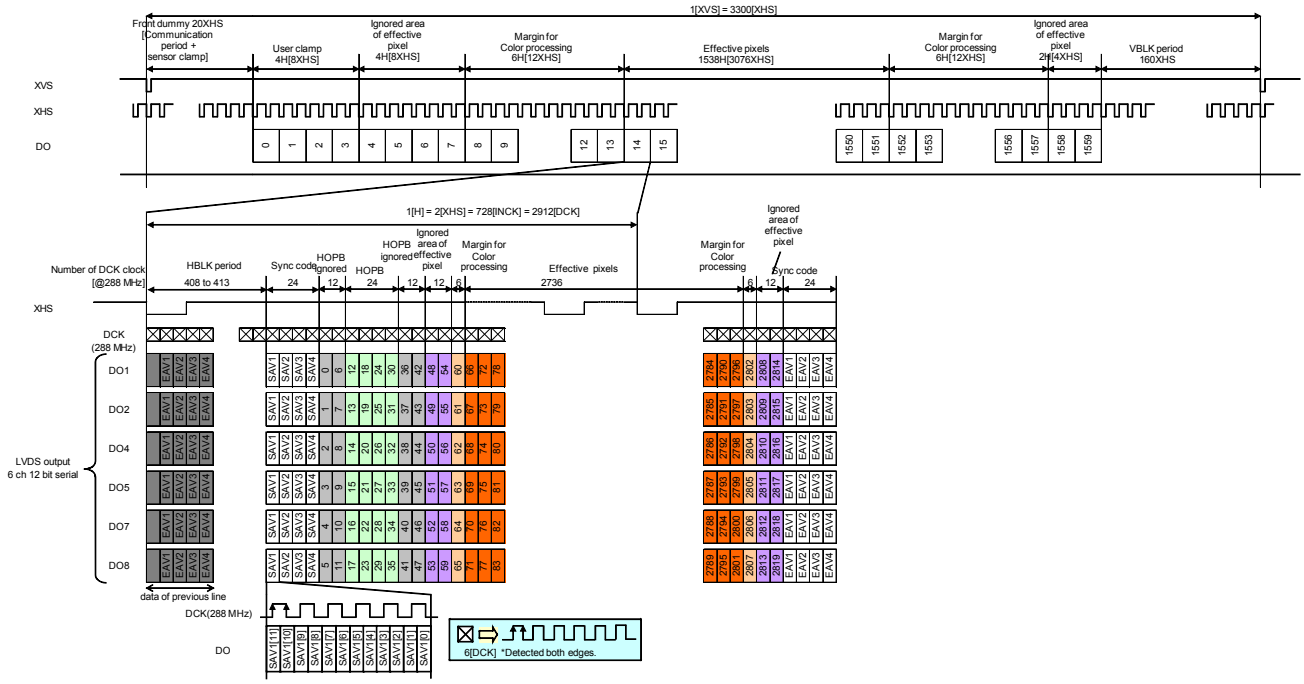


Readout Drive Timing

MODE2: Horizontal/vertical 2/2-line binning mode 16:9 cropping (horizontal and vertical weighted binning) (59.94 frame/s, 10-bit A/D conversion, 12-bit length output)

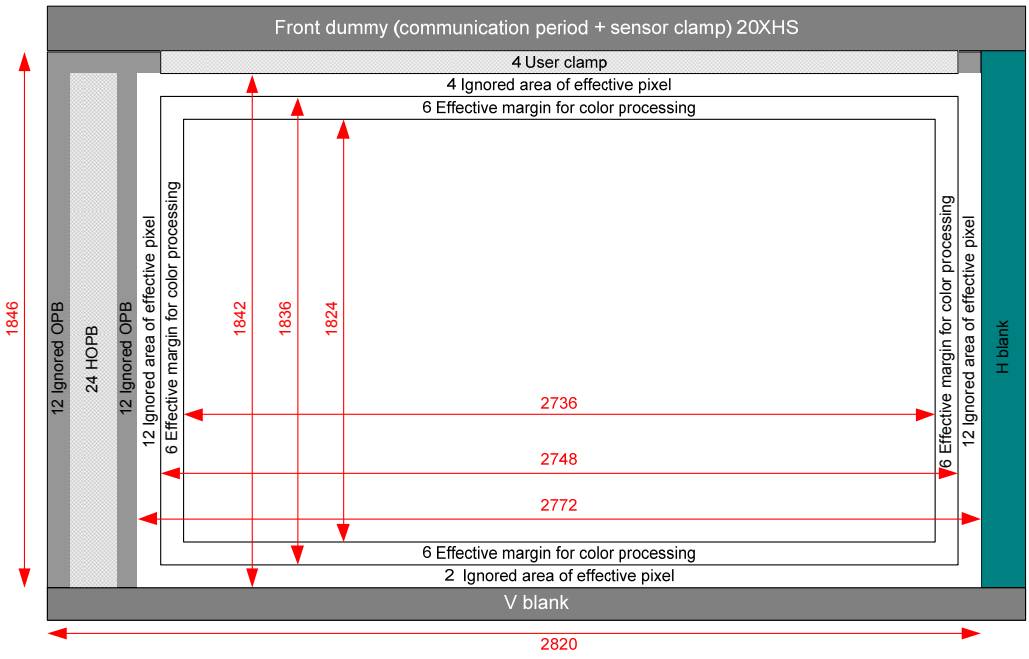


Readout Pixel Image Diagram(2736 × 1538)

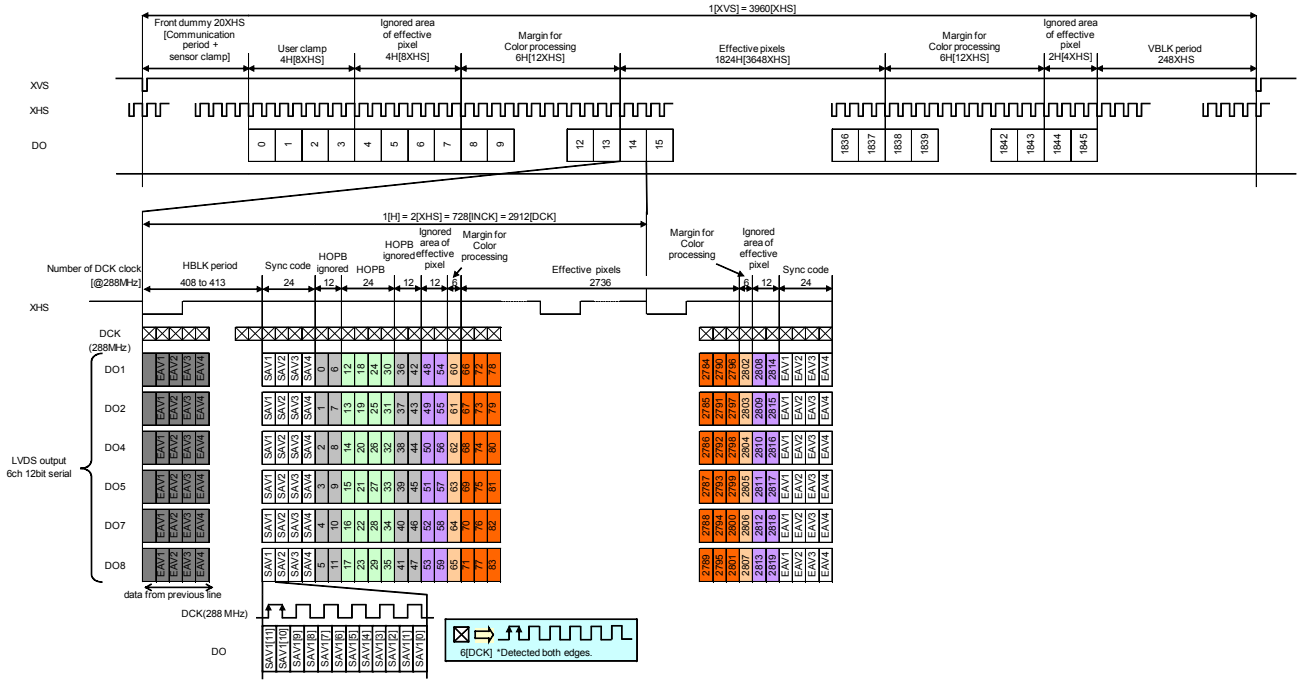


Readout Drive Timing

MODE2A: Horizontal/vertical 2/2-line binning mode (horizontal and vertical weighted binning) (49.95 frame/s, 10-bit A/D conversion, 12-bit length output)

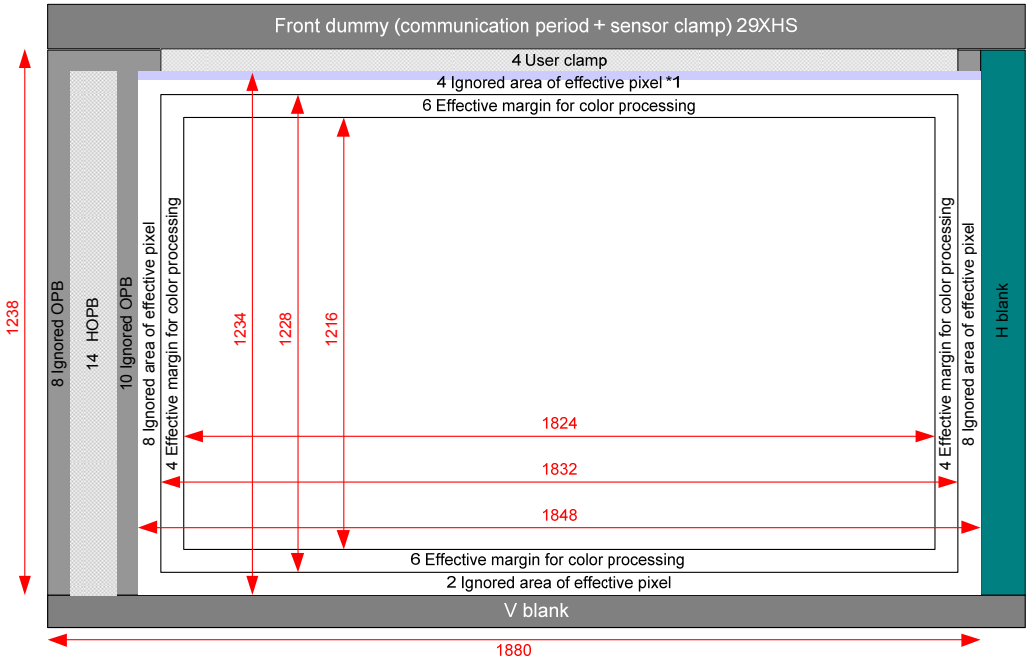


Readout Pixel Image Diagram(2736 × 1824)



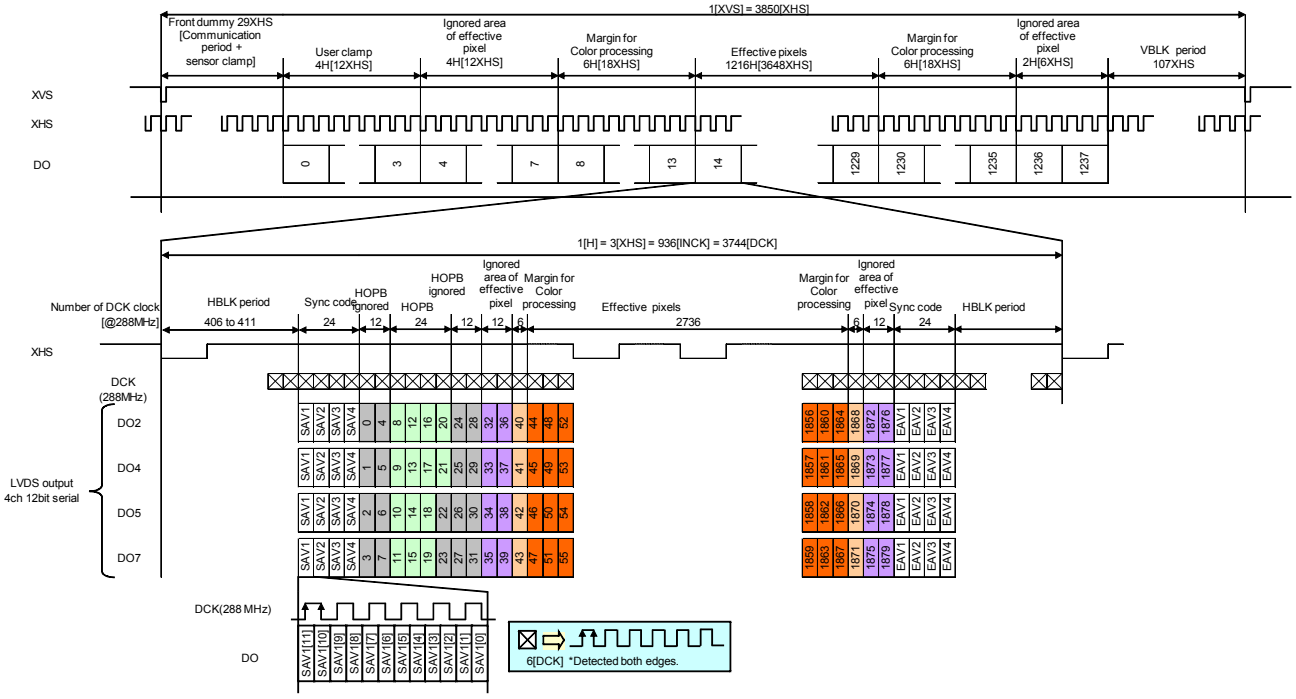
Readout Drive Timing

MODE3: Horizontal/vertical 3/3-line binning mode (59.94 frame/s, 9-bit A/D conversion, 12-bit length output)



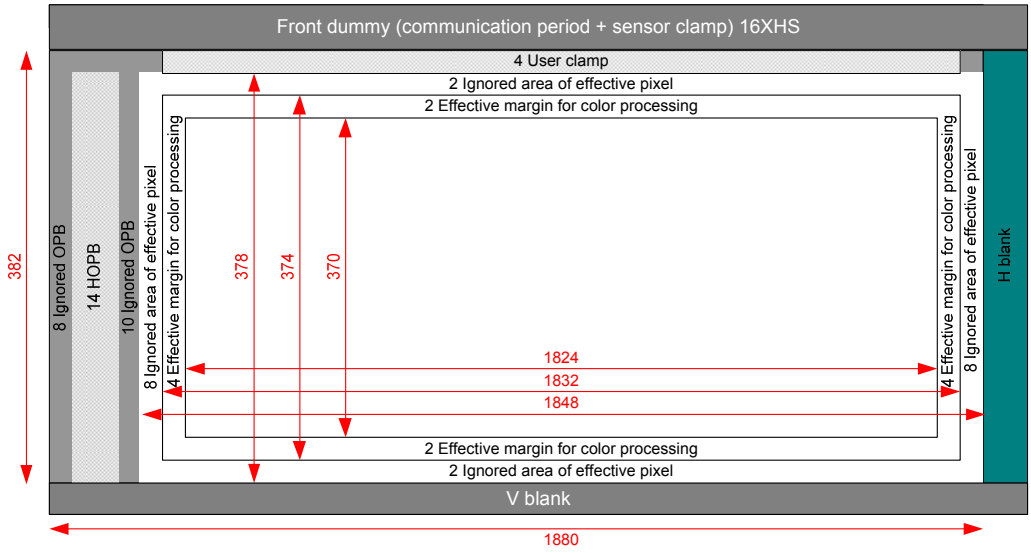
*1 When vertical direction normal readout : 4 aperture area
When vertical direction inverted readout : 1 shaded area, 3 aperture area

Readout Pixel Image Diagram (1824 × 1216)

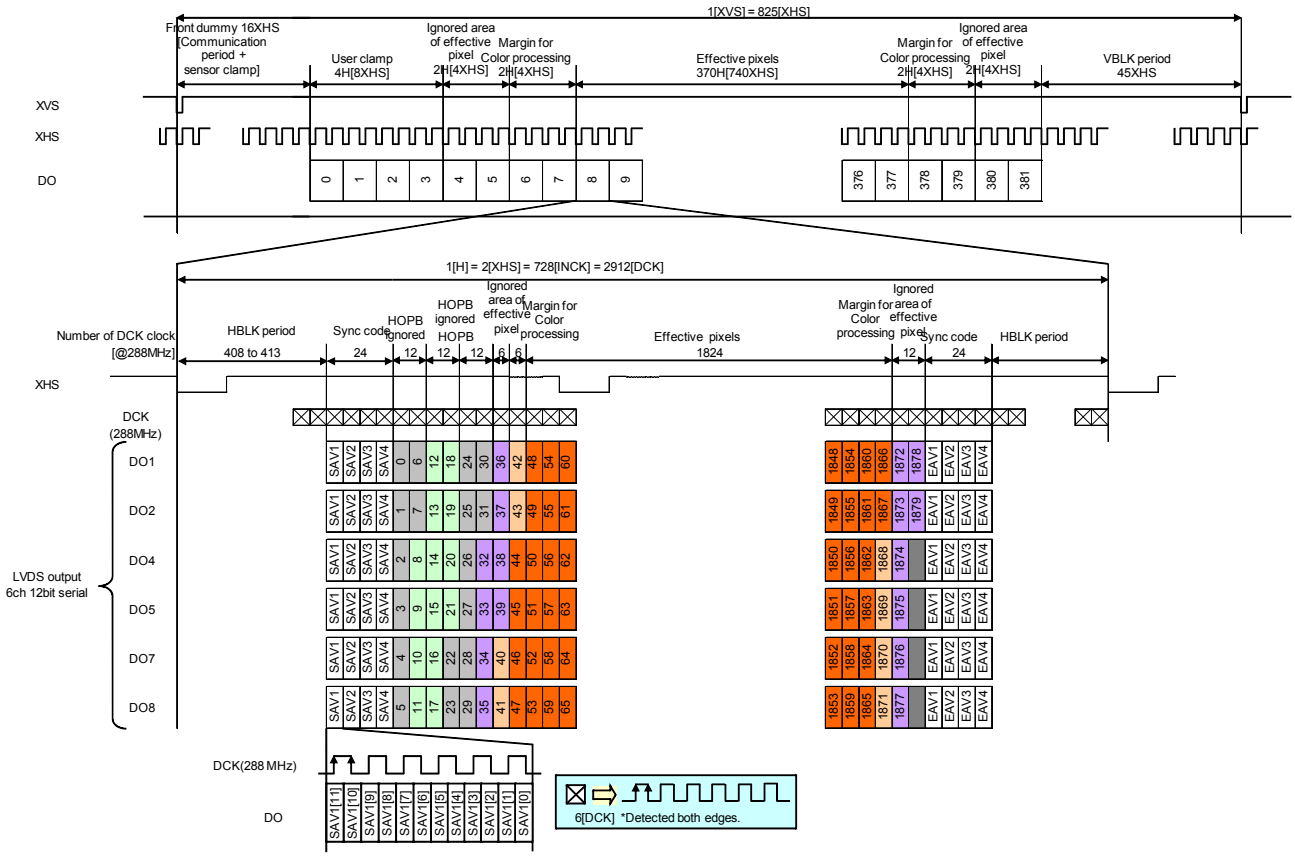


Readout Drive Timing

MODE4: Vertical 2/9 subsampling binning horizontal 3 binning mode cropping (239.76 frame/s, 9-bit A/D conversion, 12-bit length output)

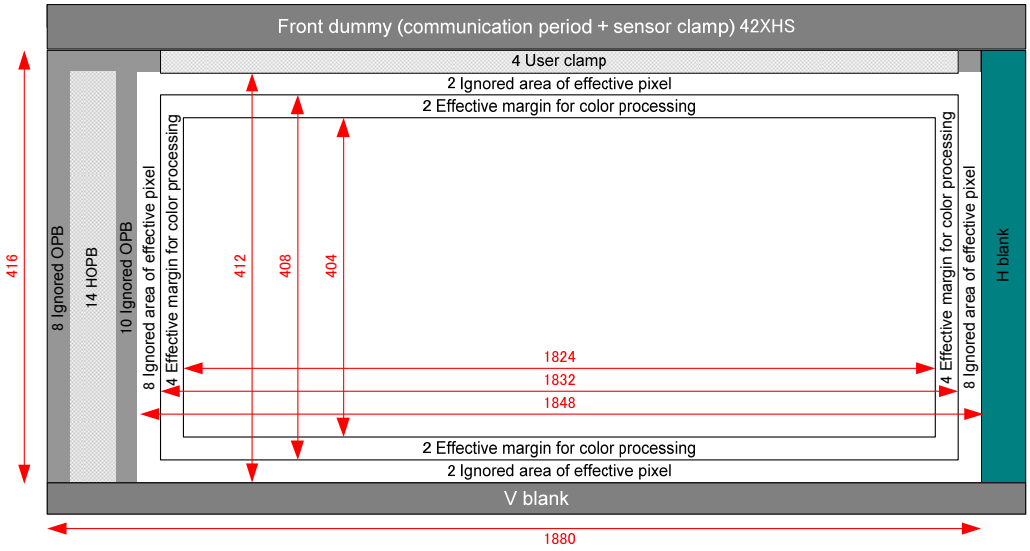


Readout Pixel Image Diagram (1824 × 370)

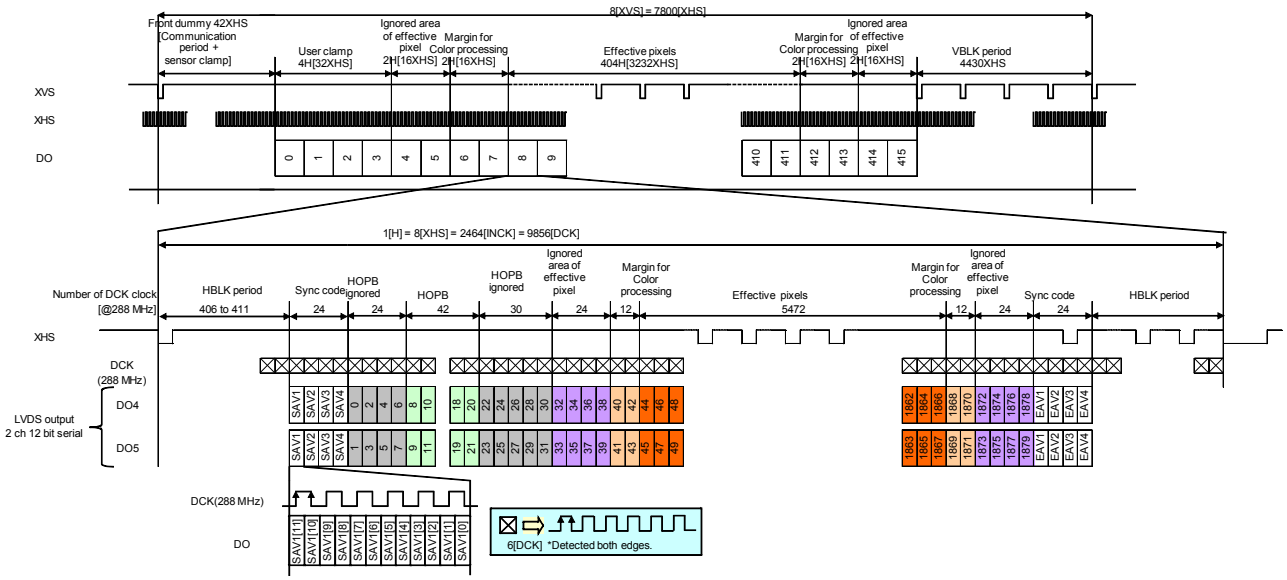


Readout Drive Timing

MODE5: Vertical 2/9 subsampling binning horizontal 3 binning mode low power consumption drive (29.97 frame/s, 9-bit A/D conversion, 12-bit length output)

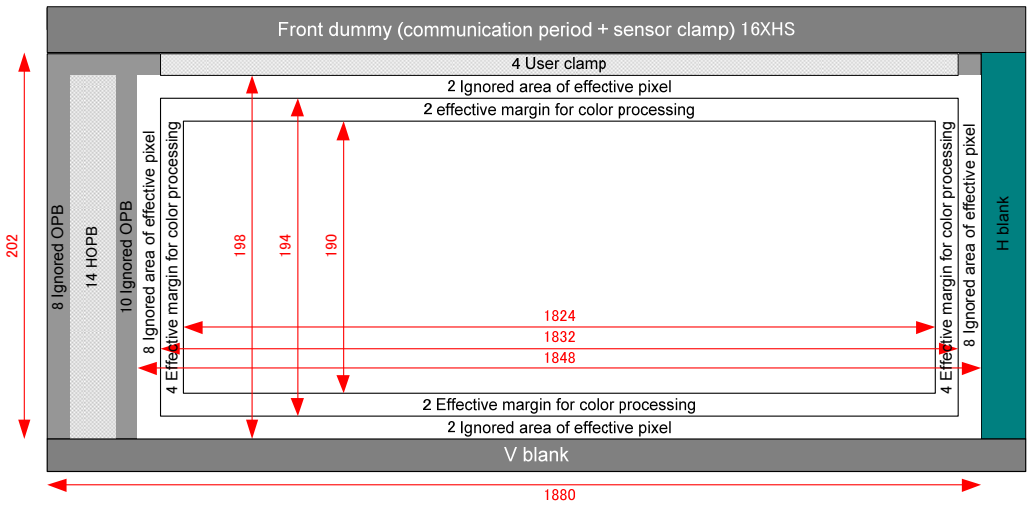


Readout Pixel Image Diagram (1824 × 404)

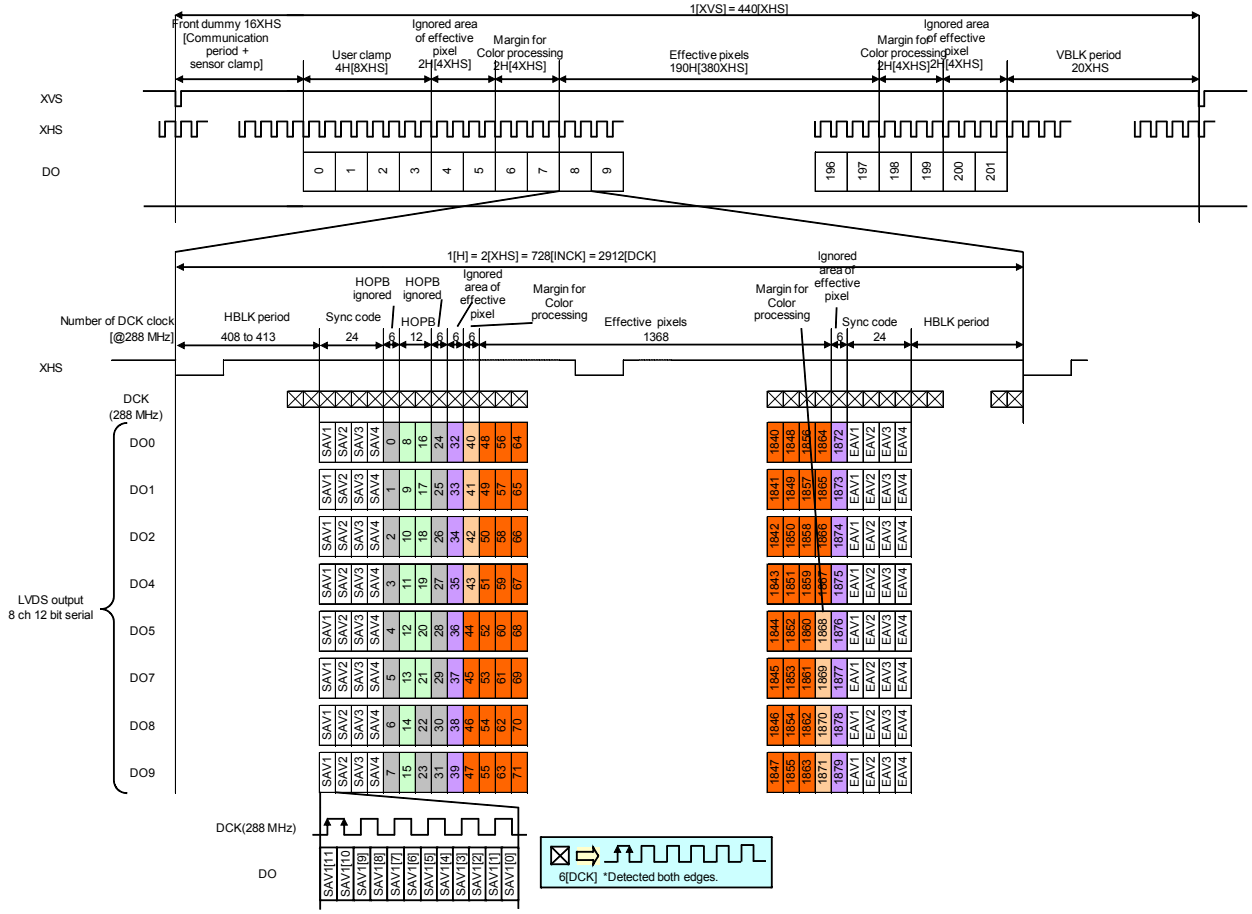


Readout Drive Timing

MODE6: Vertical 2/19 subsampling binning horizontal 3 binning mode (449.55 frame/s, 9-bit A/D conversion, 12-bit length output)

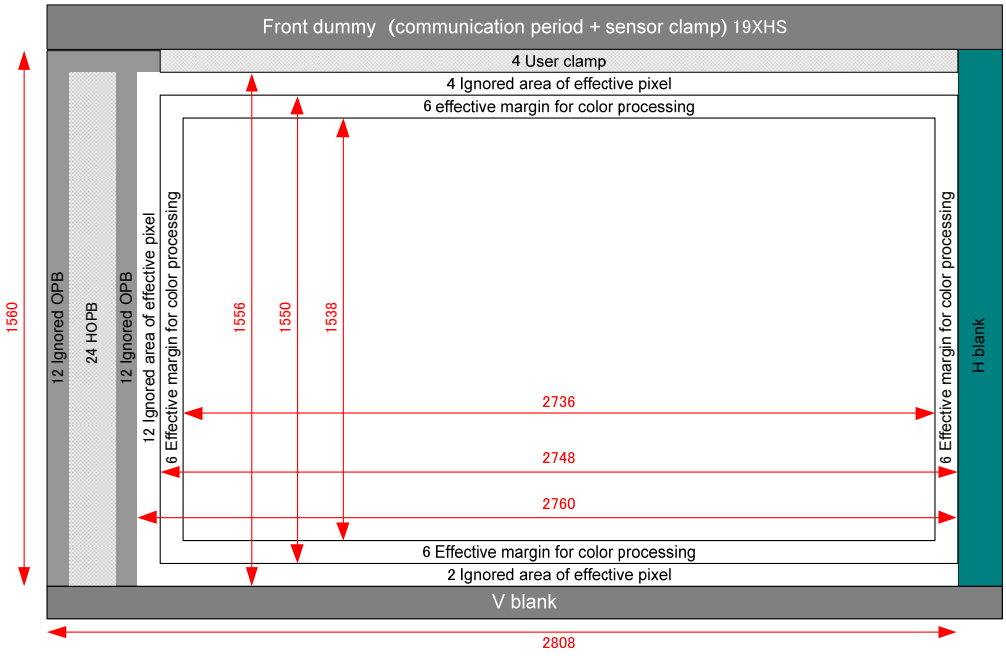


Readout Pixel Image Diagram (1824 × 190)

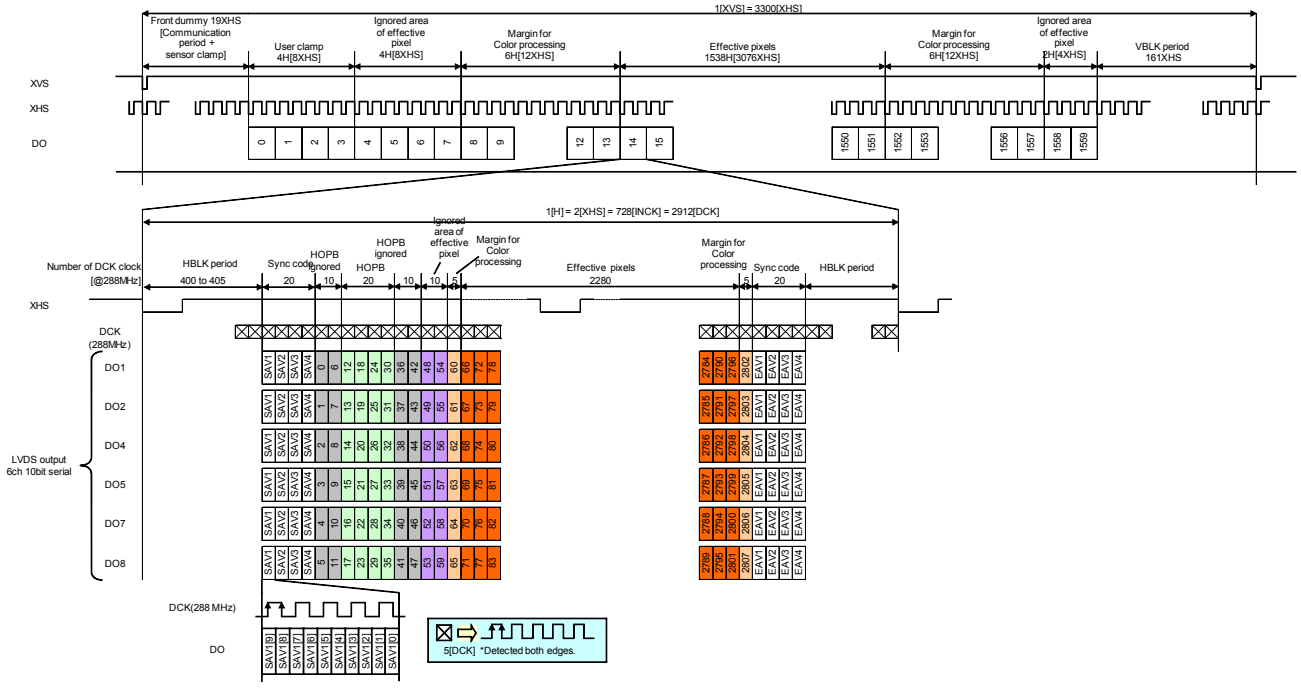


Readout Drive Timing

MODE7: Vertical 2 binning horizontal 2/4 subsampling mode 16:9 cropping (vertical weighted 2 binning) (59.94 frame/s, 10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (2736 × 1538)



Readout Drive Timing

4-2. When Using Type 1/1.4 Approx. 9.03 M Pixels (Approx. 17:9)

(1) Horizontal/Vertical Operation Period in Each Readout Drive Mode

Minimum Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Data rate [MHz]	Horizontal front blanking [DCK] *2 *3	Horizontal operation period (Number of pixels conversion)					XHS minimum period [INCK] *2
			Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
1	576 (288DDR*1)	400 to 405	96	28	4096	28	0	546

*1 DDR: Double Data Rate
*2 If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.
*3 Number of LVDS output signal DCK clock

Minimum Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						XVS minimum period [XHS]
	Vertical front blanking	Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
1	17*1 16*2	8	8	2160	6	0	2200

*1 When vertical direction normal readout
*2 When vertical direction inverted readout

(2) NTSC/PAL Compatible Drive

This sensor can be used with a frame frequency that supports NTSC or PAL by using the recommended horizontal operating period (XHS period) and recommended vertical operating period (V period) for each readout drive mode shown in the table below. Note that the number of XHS pulses input within the horizontal operating period (H period) varies according to the drive mode.

Recommended H Period and V Periods (NTSC/PAL Compatible)

Readout mode No.	NTSC compatible drive				PAL compatible drive			
	XHS period (INCK) *1	H period (number of XHS pulses) *2	V period (number of XHS pulses)	Frame frequency [frame/s]	XHS period (INCK) *1	H period (number of XHS pulses) *2	V period (number of XHS pulses)	Frame frequency [frame/s]
1	546	1	2200	59.94	576	1	2500	50.00

*1 Number of INCK conversion clocks
*2 Number of XHS pulses required to output the data for one sensor line

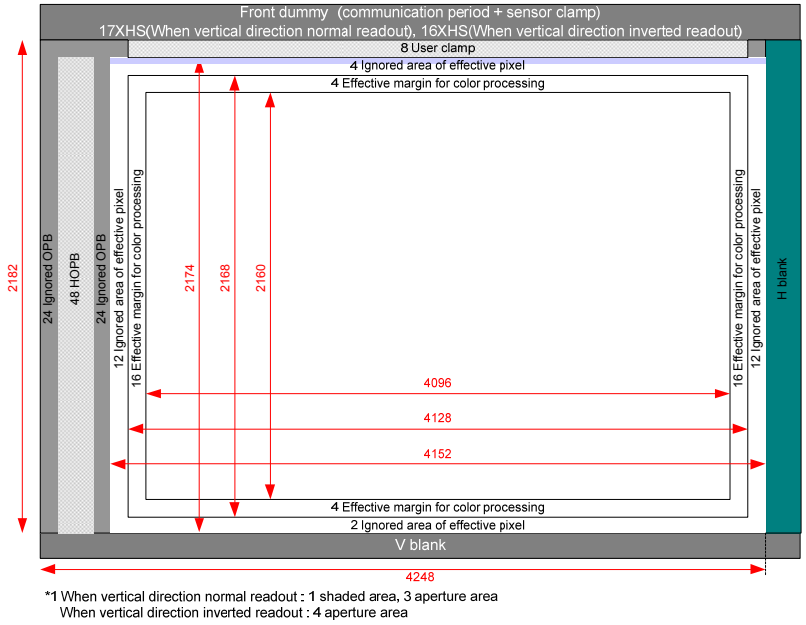
Imaging Conditions in Each Readout Drive Mode (NTSC/PAL Compatible Drive)

Readout mode No.	Imaging conditions						
	Data rate [MHz]	Number of LVDS output channels [ch]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
1	576 (288DDR)	10	10	10	4096	2160	Approximately 8.85 M Pixels

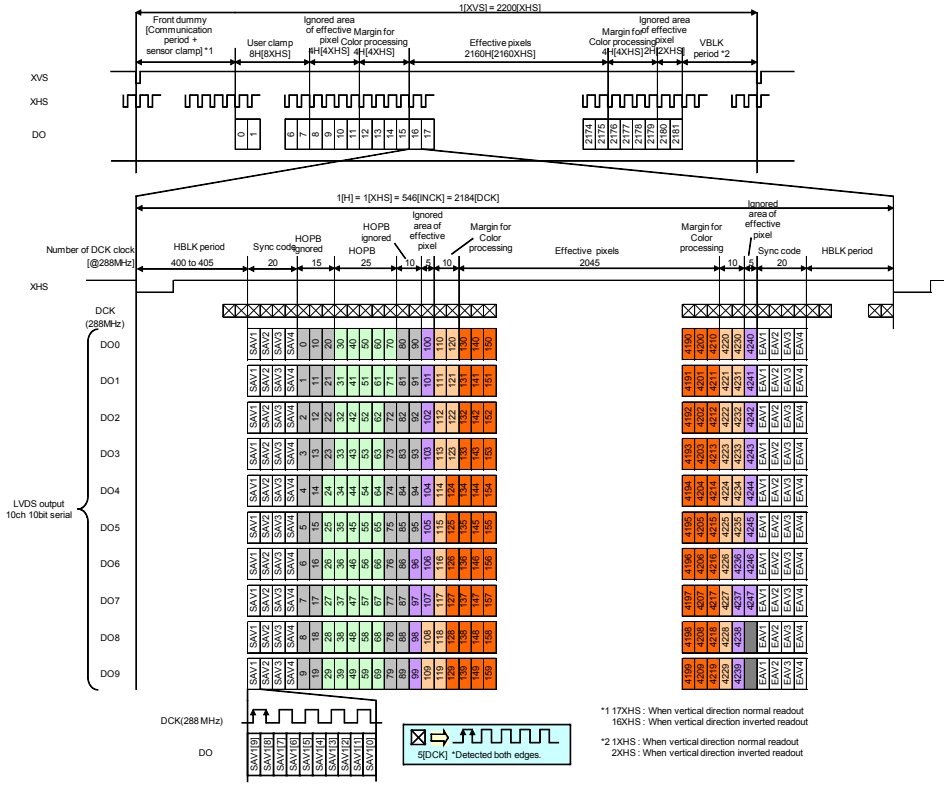
(3) Image Data Output Format

The output format in each readout drive mode is as follows.

MODE1: All-pixel scan mode (59.94 frame/s, 10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (4096 × 2160)



Readout Drive Timing

4-3. Vertical Arbitrary Cropping (All-pixel scan, 10 bits)

(1) Readout Drive Mode Outlines

Vertical cropping region can be arbitrarily changed by registers in the readout drive mode of this sensor described in the table below.

Readout mode No.	Readout drive mode	Mode description
1	All-pixel scan mode (10 bits)	In vertical arbitrary cropping area from type 1 approx. 20.48M pixels (3:2) all pixels are readout with 10-bit output.

(2) Register Settings

Set registers for readout mode No. 1, all-pixel scan mode (10 bits), when using type 1 approx. 20.48M pixels (3:2). Specify cropping width by the vertical cropping width register VWIDCUT (address 0071h, bit [7:0] and address 0072h, bit [2:0]) and MDSEL3, and cropping position by the vertical cropping start position register VWINPOS (address 006Fh, bit [7:0] and address 0070h, bit [3:0]) and MDSEL4.
Set VWINPOS negative value (two's complement) when the direction of vertical readout is inverted (address 001Ah, bit[0], MDVREV = 1h)

VWIDCUT Setting

Register value	Function
0 to 2047	Specify vertical cropping width 3694 – VWIDCUT × 2 [line]

VWINPOS Setting

Register	Function
VWINPOS	Vertical cropping start position (It is forbidden to setting value to odd number)

MDSEL3 Setting

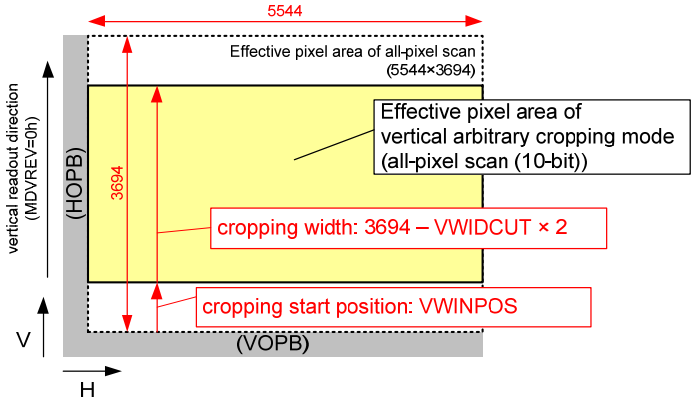
Register	Function
00h	Disable vertical cropping width
20h	Enable vertical cropping width

MDSEL4 Setting

Register	Function
00h	Disable vertical arbitrary cropping
50h	Enable vertical arbitrary cropping

Relation between register setting values of VWINPOS / VWIDCUT and cropping region on physical pixel array when vertical readout direction is normal (MDVREV=0h) is shown below.
As cropping region must not exceed all-pixel scan area, register setting values must satisfy following relations.
(Setting ranges are within those values which satisfy following.)

VWINPOS ≥ 0	(Starting position of readout must be 0 or more)
3694 – VWIDCUT × 2 ≥ 1848	(Number of readout lines must be 1848 or more)
VWINPOS + 3694 – VWIDCUT × 2 ≤ 3694	(End position of readout must be within all-pixel scan area)

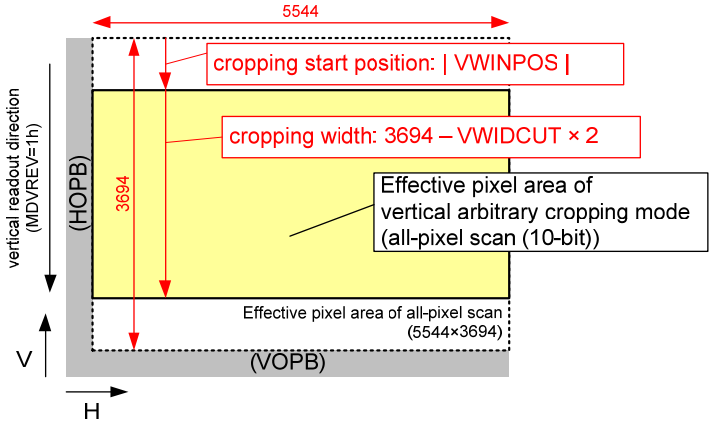


Relation Between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array
(Vertical Readout Direction Normal)

For example, when the top 400 lines of all-pixel scan area is skipped and start cropping readout from the 401st line, setting value to the register VWINPOS is 190h (400d).

Next relation between register setting values and cropping region when vertical readout direction is inverted (MDVREV=1h). Register setting values must satisfy following relations also.

| VWINPOS | ≥ 0	(Starting position of readout must be 0 or more)
3694 – VWIDCUT × 2 ≥ 1848	(Number of readout lines must be 1848 or more)
| VWINPOS | + 3694 – VWIDCUT × 2 ≤ 3694	(End position of readout must be within all-pixel scan area)



Relation Between Register Settings of VWINPOS / VWIDCUT and Cropping Region on Physical Pixel Array
(Vertical Readout Direction Inverted)

For example, when the top 400 lines of all-pixel scan area (when vertical readout direction inverted) is skipped and start cropping readout from the 401st line, setting value to the register VWINPOS is E70h (-400d)

(3) Detailed Specification of Each Mode

Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Data rate [MHz]	Horizontal front blanking [DCK] *2 *3	Horizontal operation period (Number of pixels conversion)					XHS minimum period [INCK] *2
			Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
1	576 (288DDR*1)	400 to 405	96	36	5472	36	0	720

*1 DDR: Double Data Rate

*2 If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.

*3 Number of LVDS output signal DCK clock

Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						XVS minimum period [XHS]
	Vertical front blanking	Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
1	17*1 16*2	16	24	3648 – VWIDCUT × 2	22	0	3728 – VWIDCUT × 2

*1 When vertical direction normal readout

*2 When vertical direction inverted readout

NTSC/PAL Compatible Drive

The recommended H period and V period (NTSC/PAL compatible) of vertical arbitrary cropping mode are unable to be shown because available frame rate changes depending on cropping area. Select XHS and XVS period which is more than XHS and XVS minimum period arbitrarily.

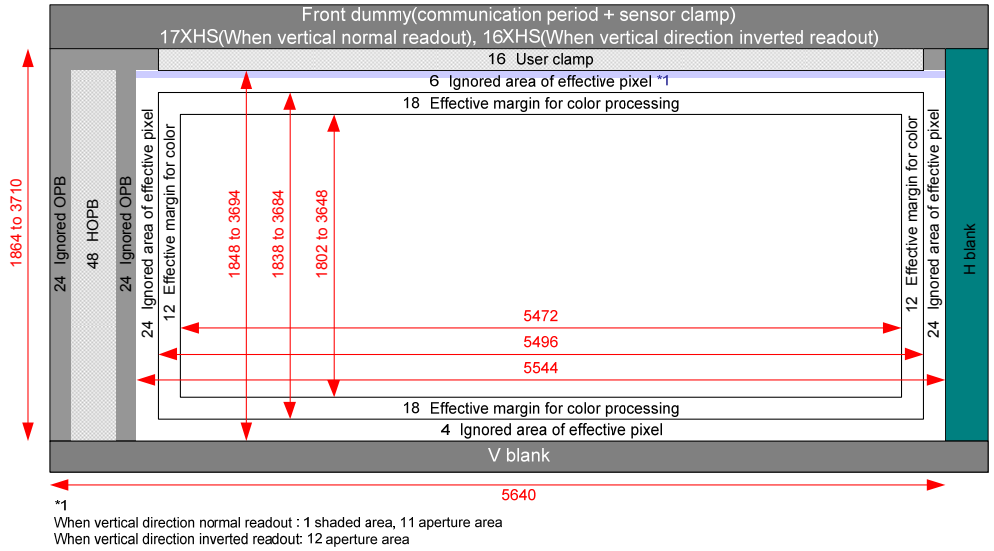
Imaging Conditions in Each Readout Drive Mode (NTSC/PAL Compatible Drive)

Readout mode No.	Imaging conditions						
	Data rate [MHz]	Number of LVDS output channels [ch]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
1	576 (288DDR)	10	10	10	5472	1802 to 3648	Approximately 9.86 to Approximately 19.96 M Pixels

(4) Image Data Output Format

The output format in each readout drive mode is as follows.

MODE1: All-pixel scan mode vertical arbitrary cropping (10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (5472 × 1802 to 5472 × 3648)

Readout Drive Timing

Integration Time in Each Readout Drive Mode and Mode Changes

1. Integration Time in Each Readout Drive Mode

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR, SVR and SPL. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

◆ Integration time of normal readout drive mode (other than mode No.5)

・When rolling operation

Integration Time [s] = [{Number of XHS per XVS period × (SVR value – SPL value + 1) – (SHR value)} × Number of clock per XHS Period + Number of clocks per internal offset period]/INCK frequency [Hz]

* See the following table for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page 32 for the SHR register setting range.

◆ Integration time of readout drive mode No.5 (low power consumption drive)

・When rolling operation

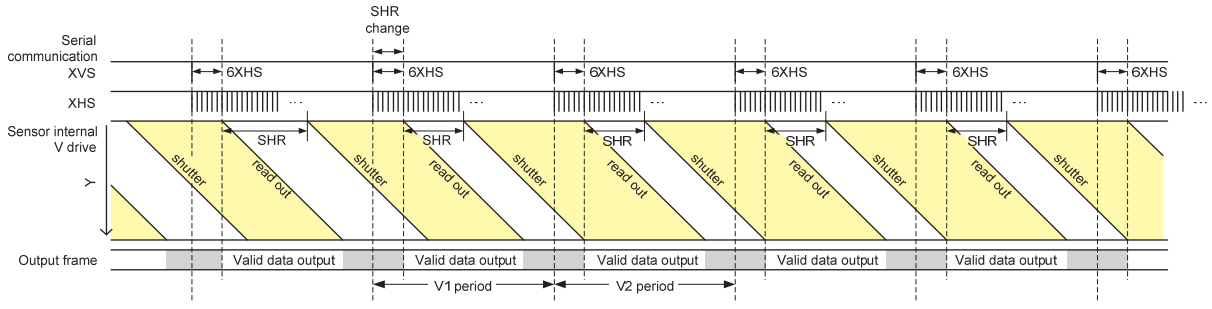
Integration Time [s] = [{Number of XHS per XVS period × (SVR value + 1) – SHR value × 4} × Number of clock per XHS period + Number of clocks per internal offset period]/INCK frequency [Hz]

* See the following table for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page 32 for the SHR register setting range.
* Only SPL = 0 can be used.

Constants Used to Calculate the Integration Time

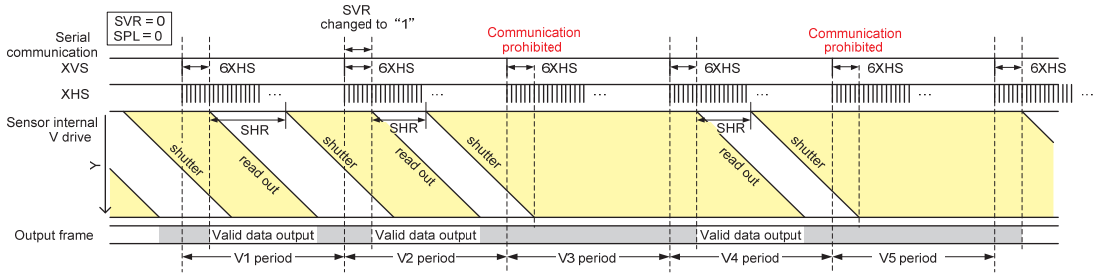
Readout mode No.	0	1	2	2A	3	4	5	6	7
Number of clocks per internal offset period	209	157	157	157	135	135	135	135	157

The figure below shows operation when changing SHR. The V1 and V2 periods in the figure below are two continuous XVS periods. The SHR value set within the first 6XHS periods (recommended serial communication period) of V1 is updated internally at the end of the 6XHS periods, and then output data which reflect the new setting is output in the V2 period. Note that the SHR setting and output are offset by 1XVS period.



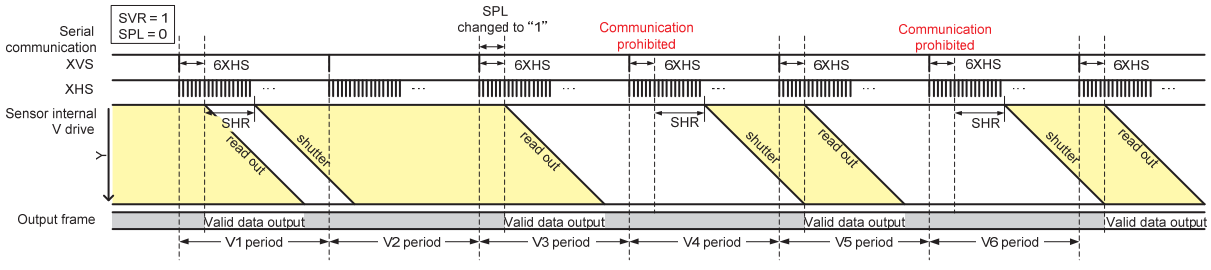
SHR Change Sequence

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal period inside the sensor is (SVR value + 1) times as long as XVS signal period. Therefore the frame rate is multiplied by 1/(SVR value + 1) according to the SVR value.
The figure below shows the operation when changing the SVR register. The example in the figure below shows the update timing when SPL = 0 and the SVR value is changed from “0” to “1”. The SVR value set within the first 6XHS periods (recommended serial communication period) of V2 is updated internally at the end of the 6XHS periods, and then applied from the shutter operation in the V2 period. Readout operation is not performed in the V3 period, and output data which reflect the changing of SVR is output in the V4 period.
The image data of the V1 period before the SVR value is changed is output as valid data in the V2 period.
In addition, note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V3 period (the frame during which readout operation is not performed)



SVR Change Sequence

When the internal vertical sync signal is subsampled by the SVR register, the SPL register can be used to set the shutter in the vertical sync signal subsampling periods (the V2, V4 and V6 periods in the figure below).
The figure below shows the operation when changing the SPL register. The example in the figure below shows the update timing when SVR = 1 and SPL is changed from “0” to “1”. SVR = 1 and SPL = 0 in the continuous frames of the V1 and V2 periods, so shutter operation is performed in the V1 period and the corresponding data is output in the V3 period. (See the aforementioned description of operation when SVR ≥ 1.)
The SPL value set within the first 6XHS periods (recommended serial communication period) of V3 is updated internally at the end of the 6XHS periods, and then applied from the shutter operation in the V3 and V4 periods. Readout operation is not performed in the V4 period, and output data which reflect the SPL change is output in the V5 period. The image data of the V1 and V2 periods before the SPL value is changed is output as valid data in the V3 period.
In addition, note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V4 period (the frame during which readout operation is not performed).
The SPL register cannot be used in readout mode No.5 (low power consumption drive), so use the SHR register when setting the shutter in the vertical sync signal subsampling period.



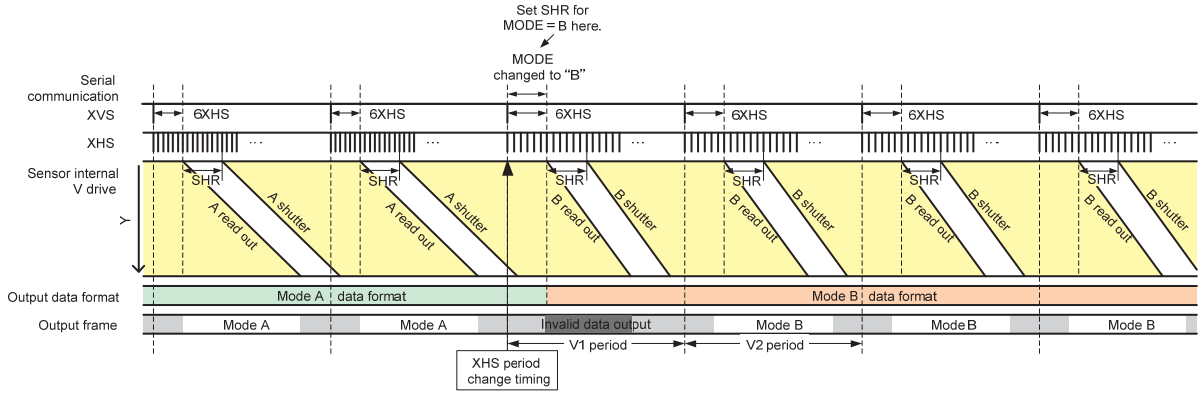
SPL Change Sequence

2. Operation when Changing the Readout Drive Mode

The following change cases are treated as mode transition on this sensor.

1. Changing the readout mode setting
2. Changing the vertical direction readout inversion setting

One frame of invalid data is always generated when changing the readout drive mode.
The figure below shows the mode transition sequence (Mode A to Mode B). The output data is invalid in the frame (V1 period in figure when SVR = 0) in which the setting is changed to Mode B. Valid data which reflect the new setting is output from the next frame (V2 period).
If the XHS period for Mode A and Mode B differs, change XHS period at the timing shown in the figure below (V1 head).
In addition, note that when the output data length or the output data rate differ in Mode A and Mode B, the new data format is output from the start of the 7th XHS of the frame (V1 period) in which the setting is changed to Mode B.



Mode Transition

3. Recommended Global Reset Shutter Operation Sequence

The recommended global reset shutter operation sequence is shown below. Operation in this mode spans multiple XVS periods. Global reset shutter is performed in the first XVS period, and the data is output in the next XVS period. The exposure time can be adjusted by varying the XVS input period. However, the minimum XVS period is 18XHS periods. In addition, the mechanical shutter must also be used to make the exposure time the same for all pixels. See “Electronic Shutter Timing” on page 32 for the SHR register setting range.

Recommended Operating Sequence for Global Reset Shutter

Operation item	Description	Explanatory diagram
Normal	When performing global reset shutter partway through rolling shutter operation	Global reset shutter normal operation
Continuous	When performing global reset shutter operation continuously	Global reset shutter continuous operation

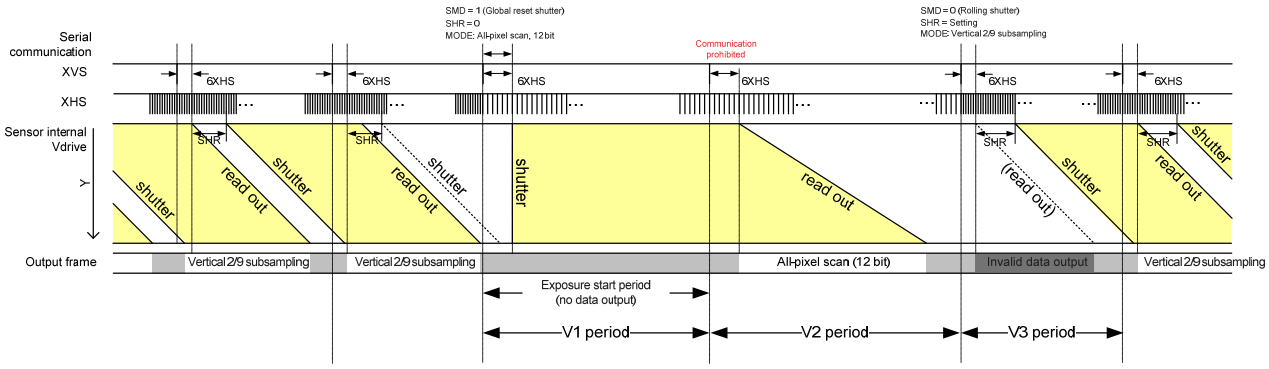
Normal Operation

Operation when performing global reset shutter + all-pixel scan (12 bits) one time partway through rolling shutter operation is shown below.
Vertical 2/9 subsampling binning horizontal 3 binning mode is described as a typical example of rolling shutter operation, but the transition operation is the same for all modes that use rolling shutter.
V1 to V3 in the figure below are three continuous XVS periods. When the global reset shutter settings (SMD = 1, register setting for all-pixel scan mode (12 bits)) are made within the first 6XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the 6XHS period. Global reset shutter readout data is output during the V2 period.
Communication to return to the original mode (SMD = 0, register setting for vertical 2/9 subsampling binning horizontal 3 binning, SHR should also be changed as necessary) is performed at the start of the V3 period.
The output data for the frame immediately after that (the V3 period in the figure) is invalid.
Note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V2 period.
The table below shows the integration start time of the exposure start period (V1 period).

Integration Start Time of the Exposure Start Period

Readout mode No.	Integration start time of the exposure start period (XVS reference)
0	Approx. 343 [INCK] after the (6 + SHR) XHS period ends *1
1	Approx. 291 [INCK] after the (6 + SHR) XHS period ends *1

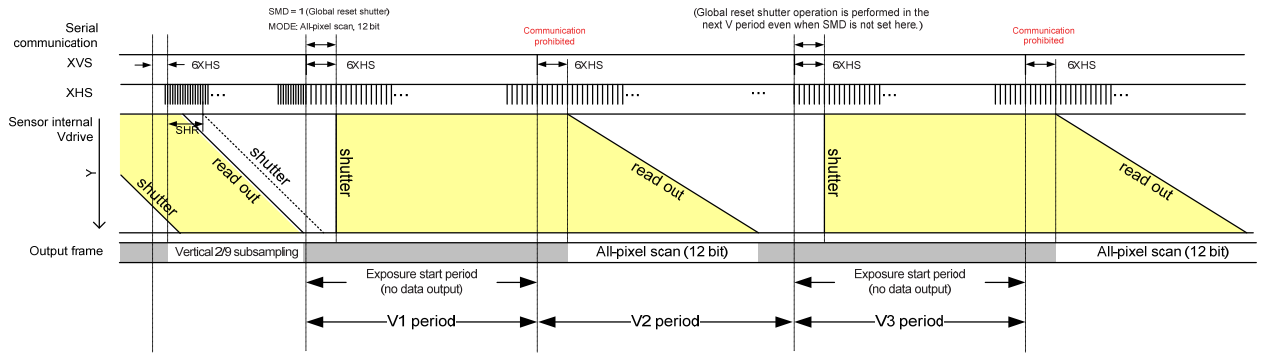
*1 Number of clocks in conversion of INCK = 72 MHz



Global Reset Shutter Normal Operation

Continuous Operation

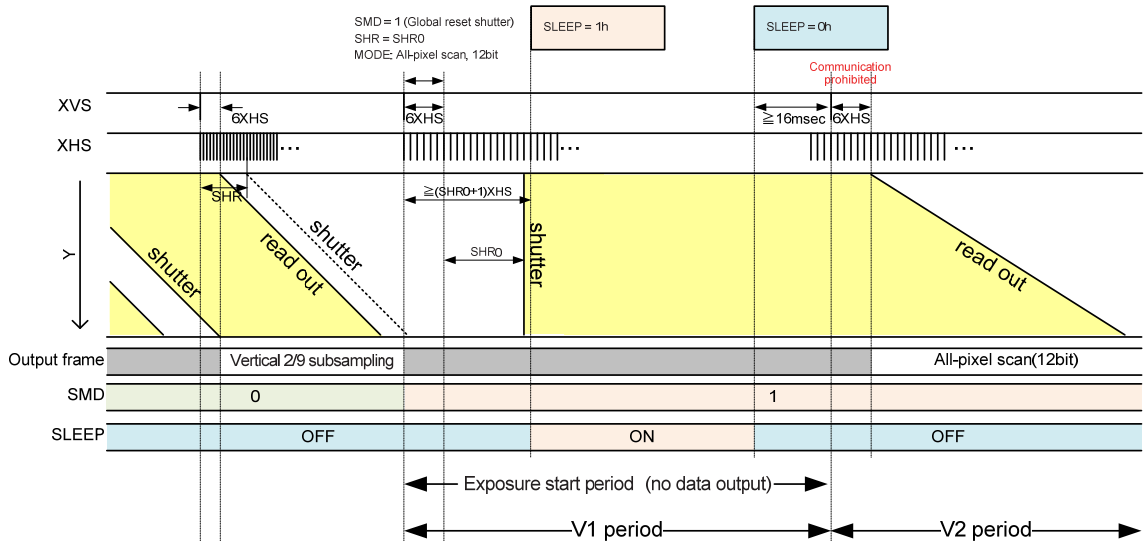
Operation when continuously performing global reset shutter + all-pixel scan (12 bits) is shown below.
V1 to V3 in the figure below are three continuous XVS periods. When the global reset shutter + all-pixel scan (12 bits) settings (SMD = 1, register setting for all-pixel scan mode (12 bits)) are made within the first 6XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the first 6XHS period of the V1 period, and the all-pixel scan (12 bits) data is output in the V2 period. The operation during V1 and V2 periods is then repeated each time XVS is input until the mode setting is changed next. Note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) in the V2 period.
See the previous section for a description of the procedure when changing from continuous operation to a different readout mode.



Global Reset Shutter Continuous Operation

Low Power Consumption Drive in Exposure of Global Reset Shutter Operation Sequence

The sequence of low power consumption drive when exposing of global reset shutter operation is shown below.
To change to low power consumption drive, set the register SLEEP (address 0000h, bit [4]) to 1h after (SHR setting value + 1) × XHS period or more in the frame of changing the register SMD from 0h to 1h.
And for readout, set SLEEP to 0h before 16 ms of readout frame in order to cancel low power consumption mode.

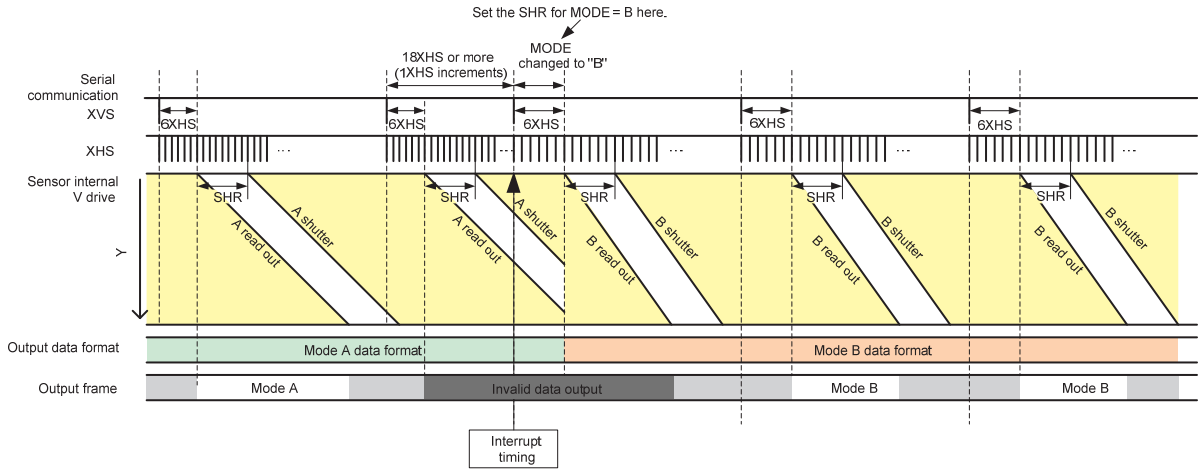


Low Power Consumption Drive in Exposure of Global Reset Shutter Operation Sequence

4. Interruptive Mode Change

The sensor mode can be changed using interrupts in all modes.
When changing the mode using an interrupt, the mode can be changed by inputting XVS in sync with XHS after 18XHS periods or more[*1] have elapsed from the start of the frame, and transmitting the mode setting register value within the communication period. In addition, the data output before the interrupt mode change is cut off at the timing of the interrupt mode change.

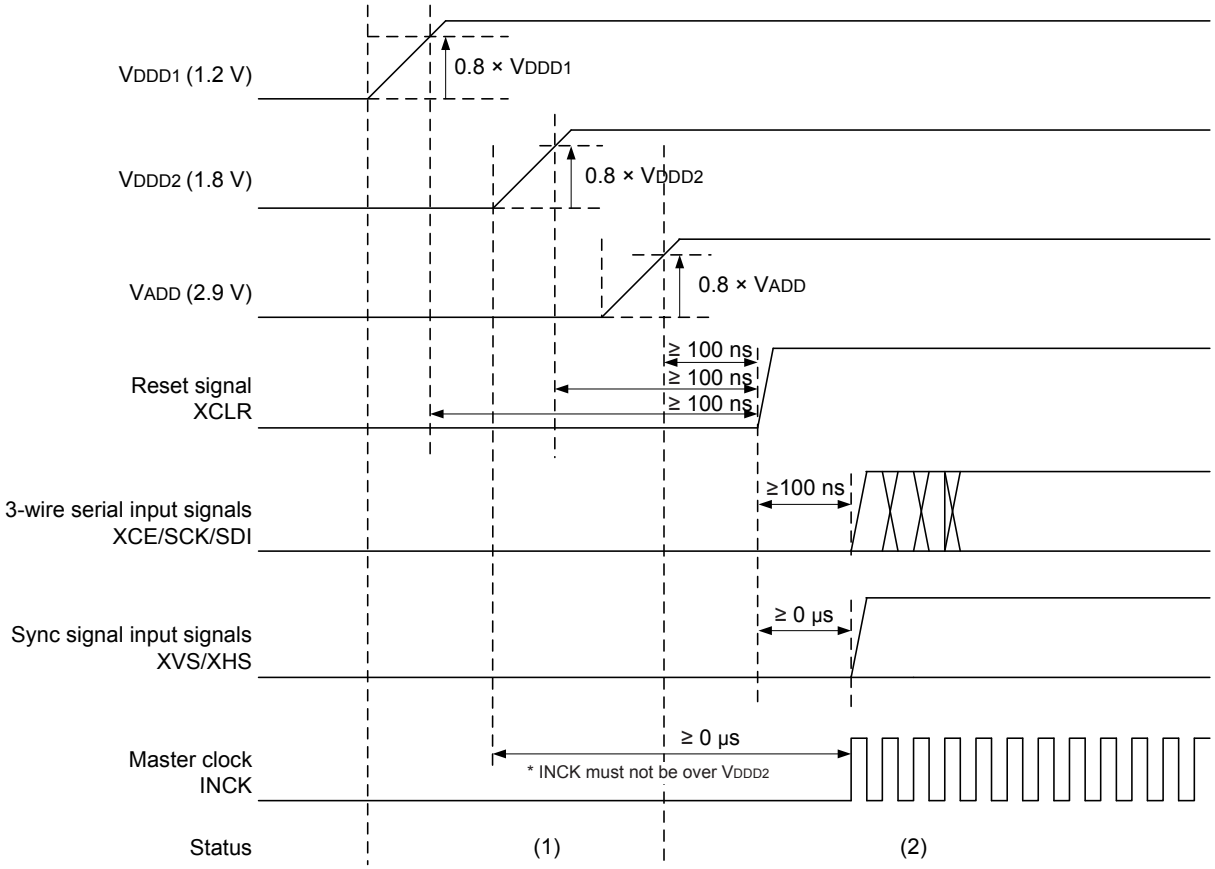
[*1] When the mode before the change (Mode A in the figure below) is readout mode No.5 (low power consumption drive), wait 54XHS periods or more from the start of the frame.



Interruptive Mode Change

Power-on/off Sequence

1. Power-on Sequence

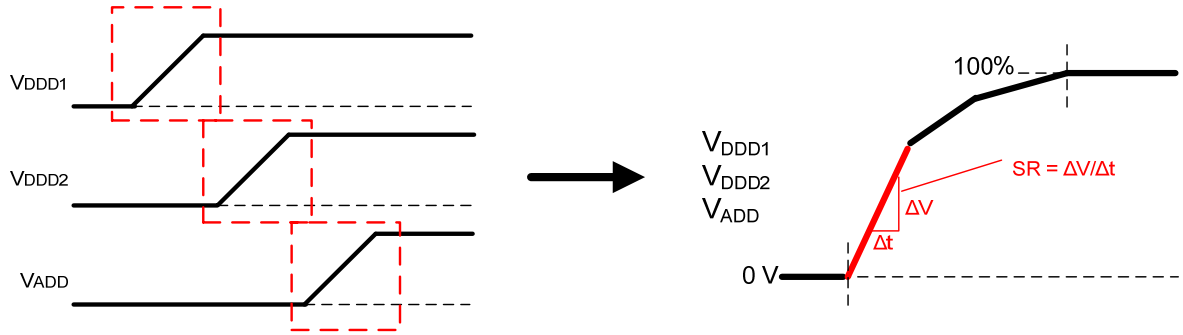


Power-on Sequence

Period name	Remarks
(1) Power stabilization time	All input signals are at Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, V_{DDD2}.
(2) Standby cancel register communication	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1}, V_{DDD2}. Then set XCLR to “H” and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence

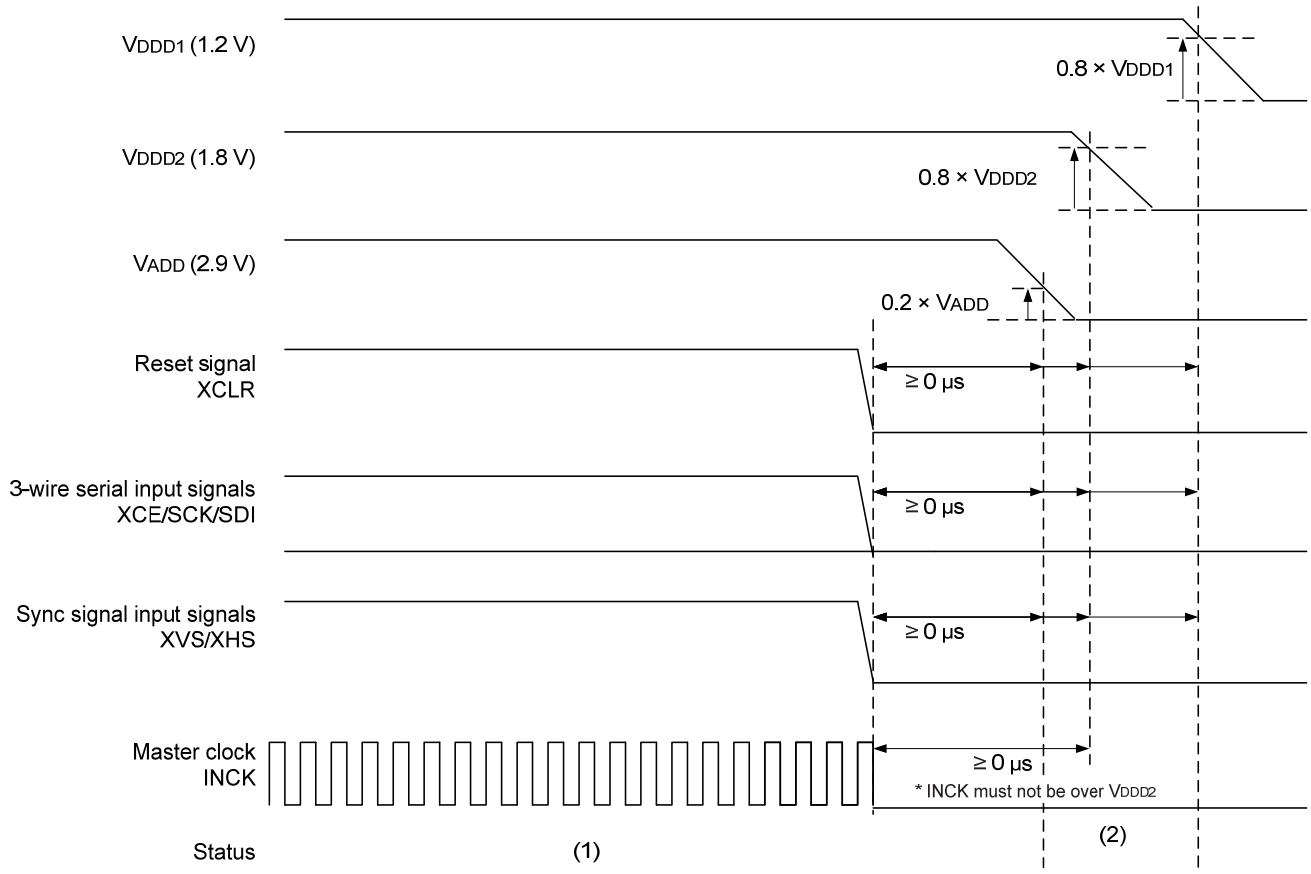
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/μs	
		V_{DDD2} (1.8 V)	—	25	mV/μs	
		V_{ADD} (2.9 V)	—	25	mV/μs	

3. Power-off Sequence

Make sure that all input signals for the 3-wire serial interface and other signals are at Low level in the area of (2).



Power-off Sequence

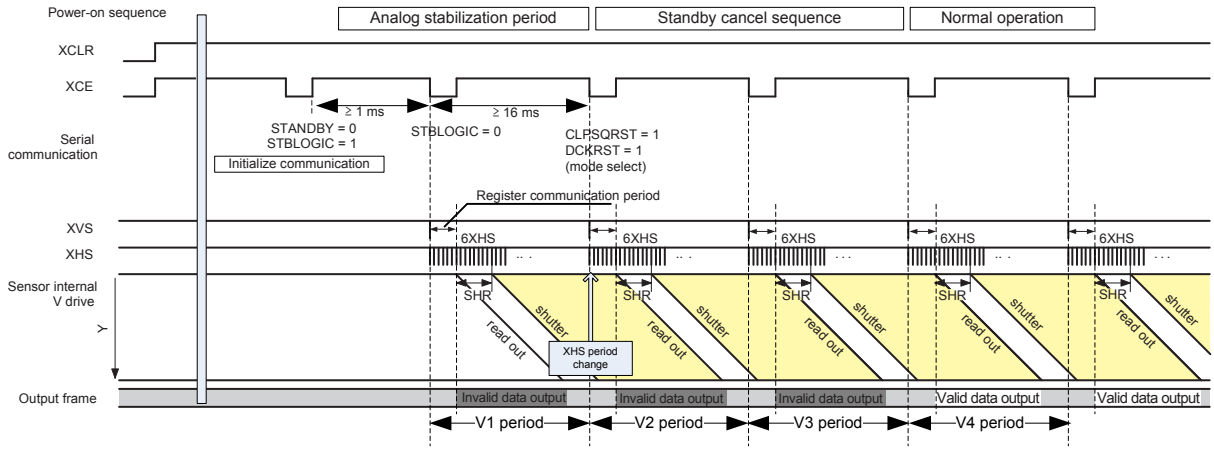
Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off time	Turn the power supplies off after "L" level is set to all input signals. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, V_{DDD2}.

Standby Cancel Sequence

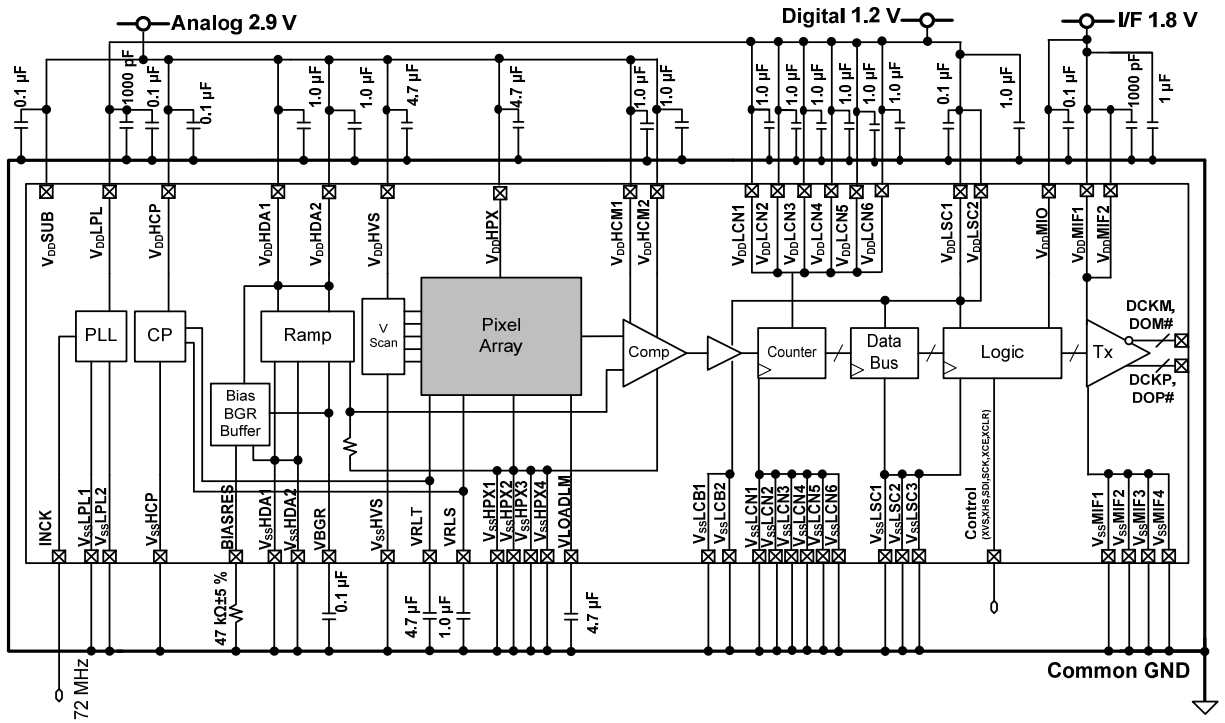
After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancel sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, set address 0000h, bit [1:0] to "2h" (STANDBY register = 0h, STBLOGIC register = 1h). When initialize communication is performed before the register communication period in the V1 period, there are no restrictions on the communication order. Register communication can be performed even when STANDBY = 1h.
2. After a stabilization period of 1 ms or more, set address 0000h, bit [1:0] to “0h” (STANDBY register = 0h, STBLOGIC register = 0h).
   In addition, when using the V4 period data after canceling standby mode, transmit the mode select register required for normal operation during the communication period of V2 period. Transmit the shutter setting and other settings during the communication period of V1 or V2 period.
3. After an analog stabilization period of 16 ms or more, set "1h" in the LVDS clock output phase locking register DCKRST (address 0001h, bit [0]) and “1h” in the clamp reset register CLPSQRST (address 0001h, bit [4]) during the register communication period of the next frame (the V2 period).

Note) 1. Vertical and horizontal sync signal can be input during initialize communication.
2. The V1 period requires a time of 16 ms or more.



Peripheral Circuit Diagram



Note) Locate a bypass capacitor for each pin. Note that even when pins have the same voltage, connecting the power supply wiring before these capacitors produces common impedance and may result in unexpected trouble.

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

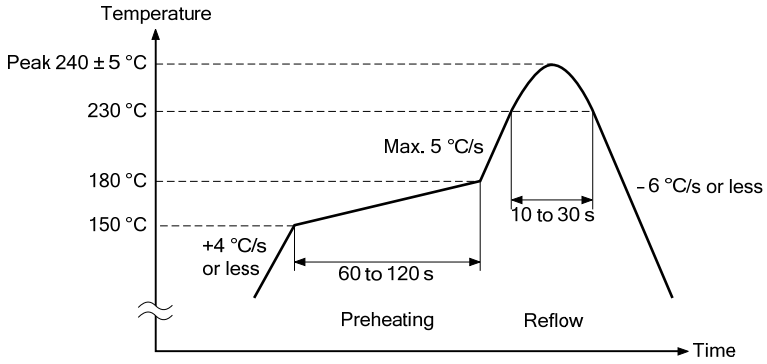
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (– 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

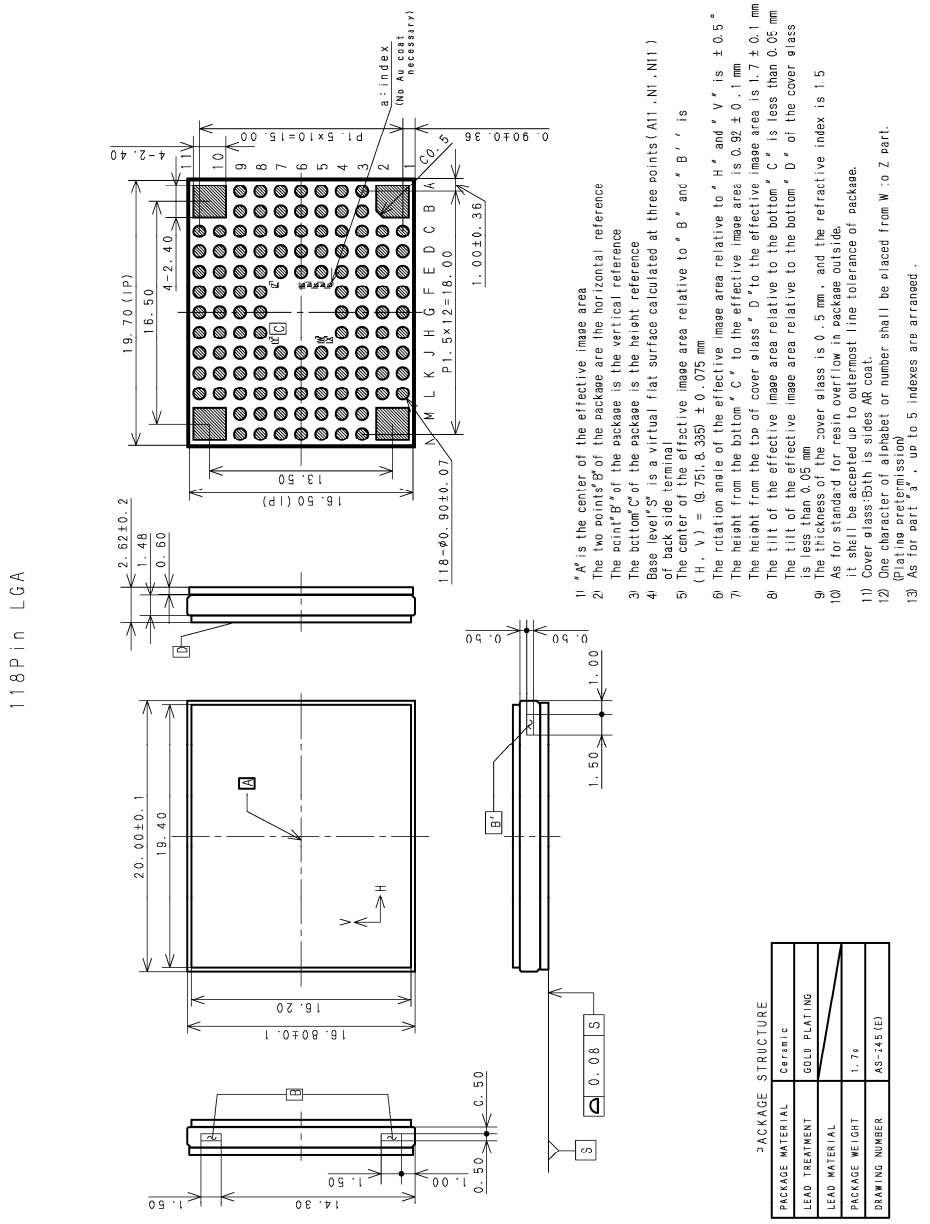
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.6

Package Outline

(Unit: mm)



1) "A" is the center of the effective image area
2) The two points"B"of the package are the horizontal reference
   The point"B'"of the package is the vertical reference
3) The bottom"C"of the package is the height reference
4) Base level"S" is a virtual flat surface calculated at three points(A11.N1.N11)
   of back side terminal
5) The center of the effective image area relative to " B " and " B ' " is
   (H, V) = (9.751,8.335) ± 0.075 mm
6) The rotation angle of the effective image area relative to " H " and " V " is ± 0.5 °
7) The height from the bottom " C " to the effective image area is 0.92 ± 0.1 mm
   The height from the top of cover glass " D "to the effective image area is 1.7 ± 0.1 mm
8) The tilt of the effective image area relative to the bottom " C " is less than 0.05 mm
   The tilt of the effective image area relative to the bottom " D " of the cover glass
   is less than 0.05 mm
9) The thickness of the cover glass is 0.5 mm, and the refractive index is 1.5
10) As for standard for resin overflow in package outside,
    it shall be accepted up to outermost line tolerance of package.
11) Cover glass:Both is sides AR coat.
12) One character of alphabet or number shall be placed from W to Z part.
    (Plating pretermission)
13) As for part "a", up to 5 indexes are arranged.

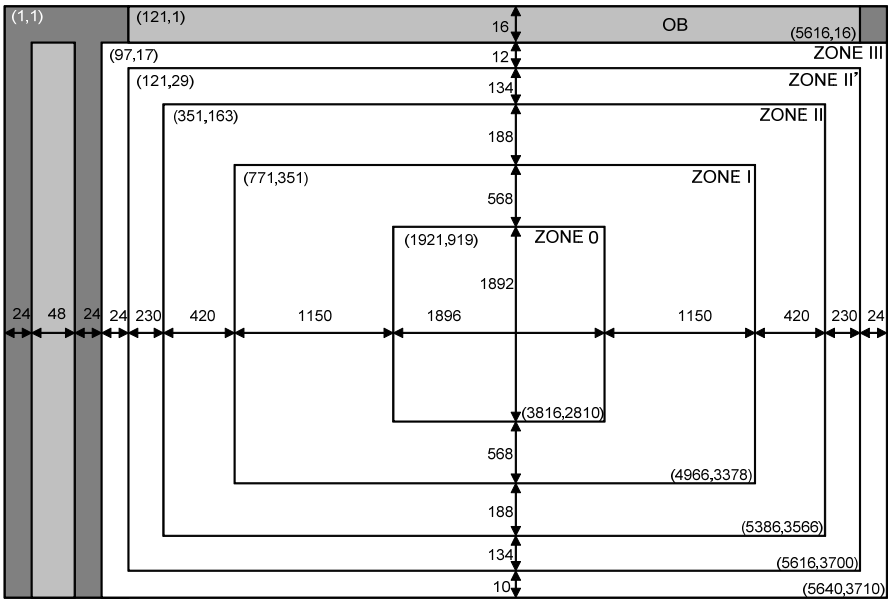
Spot Pixel Specifications

(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, 19.98 frame/s, reference gain 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone						Measure-ment method	Remarks
		0	I	II	II'	OB	III		
Black pixels at high light	30 % ≤ D	A[*1]				No evaluation criteria applied		1	
White pixels at high light	30 % ≤ D					No evaluation criteria applied		1	
White pixels in the dark	32.7 digit ≤ D	B[*1]					No evaluation criteria applied	2	1/30 s integration
Black pixels at signal saturated	D ≤ 2676 digit	C[*1]				No evaluation criteria applied		3	

Note) 1. Spec of the sum of A, B and C is 4000 pixels.
2. D...Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
3. Zone definition is illustrated in the figure below.
4. 1 digit ≈ 0.2465 mV when 12 bits output.

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
4.0 mV or higher	21.0 pcs
5.6 mV or higher	16.4 pcs
8.1 mV or higher	12.5 pcs
10.0 mV or higher	10.6 pcs
24.0 mV or higher	5.5 pcs
50.0 mV or higher	3.2 pcs
72.0 mV or higher	2.4 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

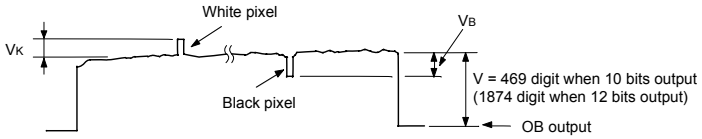
Material_No.03-0.0.9

Measurement Method for Spot Pixels

1. Black or white pixels at high light

After adjusting the luminous intensity so that the average value of signal output is 469 digit when 10 bits output (1874 digit when 12 bits output), measure the local dip point (black pixel at high light, V_B) and peak point (white pixel at high light, V_K) in each channel signal output. Substitute the values into the following formula.

Spot pixel level = (V_K (or) V_B)/V × 100 [%]



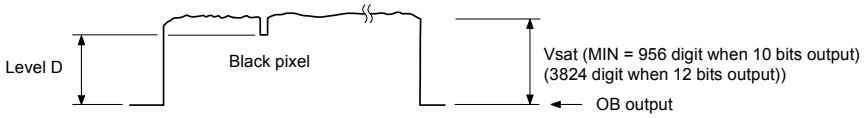
Signal output waveform

2. White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated

Set the device to operate in saturation and measure the local dip point in using the OB output with sensor as a reference.



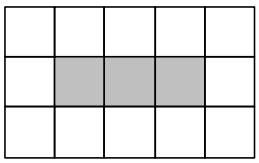
Signal output waveform

Spot Pixel Pattern Specifications

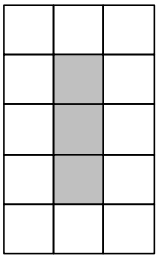
For patterns of white pixels in the dark (T.B.D digit ≤ D), Black pixels at signal saturated (D ≤ T.B.D digit), white pixels at high light (T.B.D % ≤ D) and black pixels at high light (T.B.D % ≤ D), the following table is applied.

Type of distortion	Maximum distorted pixels in each zone						Remarks
	0	I	II	II'	OB	III	
(1) Three adjacent pixels in the horizontal direction	T.B.D				No evaluation criteria applied		
(2) Three adjacent pixels in the vertical direction	T.B.D				No evaluation criteria applied		
(3) Three adjacent pixels in the diagonal direction	T.B.D				No evaluation criteria applied		

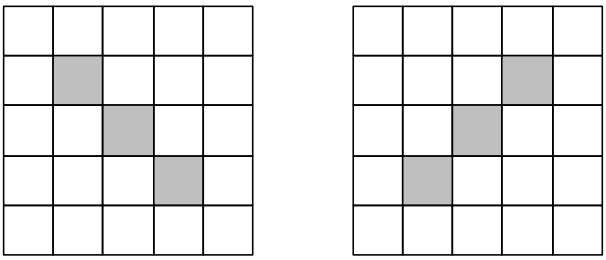
(1) Example of three adjacent pixels in the horizontal direction



(2) Example of three adjacent pixels in the vertical direction



(3) Example of three adjacent pixels in the diagonal direction

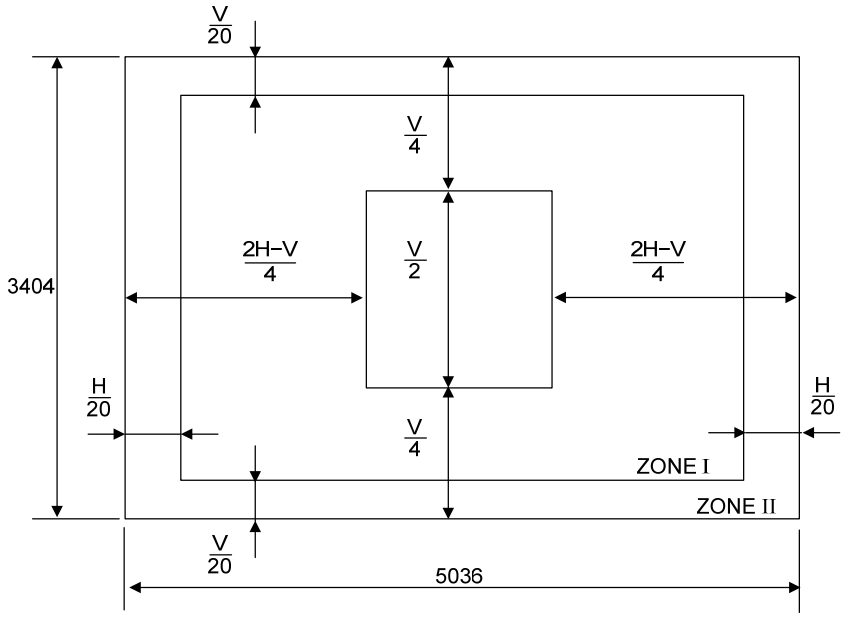


indicates spot pixels

Stain Specifications

Zone	Allowable pixels	Total allowable pixels	Size	Level	Remarks
0	1	3	3 ≤ L ≤ 10 lines	4 ≤ R ≤ 8 %	≥ 200 lines
I	2				
II	3		4 ≤ L ≤ 20 lines	4 ≤ R ≤ 8 %	Overlap permitted
For a stain extending over two or more zones, the largest zone is applied to count.					

Stain Zone Definition

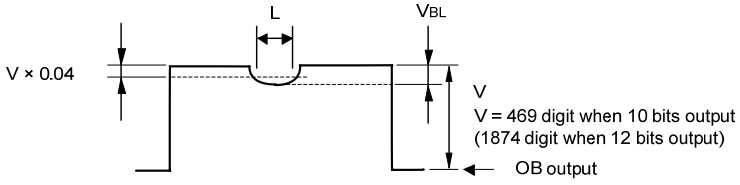


Stain Measurement Method

In the following measurements, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the signal output is 469 digit when 10 bits output (1874 digit when 12 bits output). Measure the local dip in the average value of the signal output (V_{BL}), and then calculate the stain level (R) as the ratio of V_{BL} to the average value of the signal output (V).

$$R = V_{BL}/V \times 100\ [\%]$$

At the same time, the size (L) of the area where the stain level is 4 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.



Signal output waveform

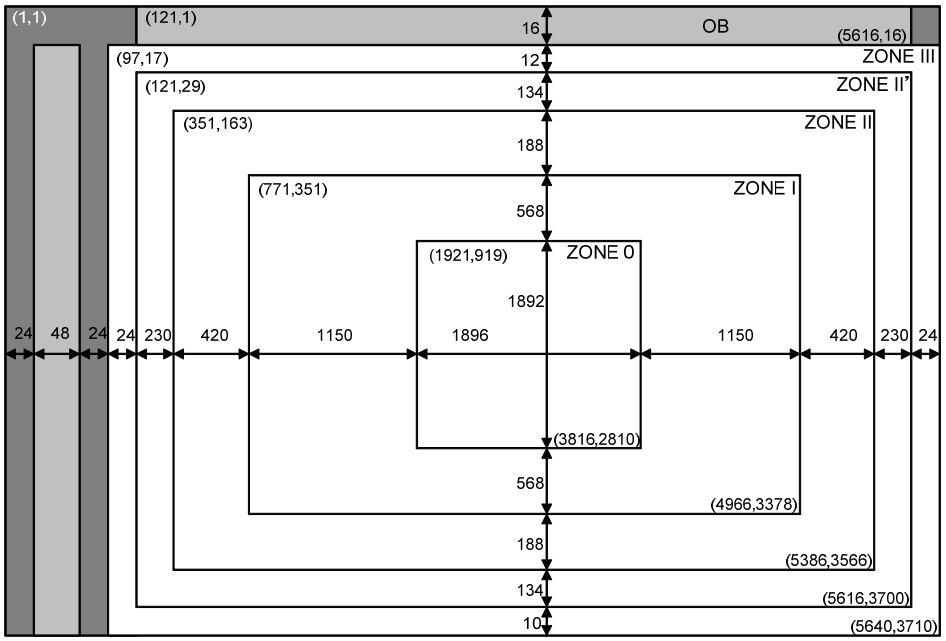
Blooming White Pixels Specifications

(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, reference gain 0 dB)

Item	Level	Maximum distorted pixels in each zone						Measurement Method	Remarks
		0	I	II	II'	OB	III		
Blooming white pixels in the dark	981 digit ≤ D	101				No evaluation criteria applied		1	2 s integration
Adjacent blooming white pixels in the dark	981 digit ≤ D	0				No evaluation criteria applied		2	
Serial Blooming white pixels in the dark	1962 digit ≤ D	0				No evaluation criteria applied		3	

Note) 1 digit ≈ 0.2465 mV when 12 bits output..

Blooming White Pixels Zone Definition



Measurement Method for Blooming White Pixels

1. Blooming white pixels in the dark

For patterns of white pixels and blooming white pixels, the following measurement method is applied.

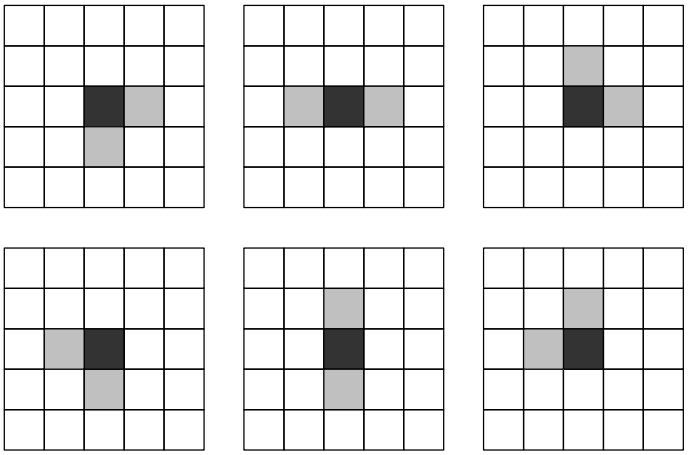
(1) Acquire dark signal output in integration time of 2 s.

(2) Define the pixels that satisfy the following conditions as blooming white pixels, and count them.

(a) The output is 3824 digit or more when 12 bits output.

(b) The number of pixels whose output is D digit or more when 12 bits output, within the adjacent 4 pixels in horizontal and vertical direction of (a) pixel, is two or more.

Example of blooming white pixels



■ indicates white pixels whose output is 3824 digits or more when 12 bits output.

□ indicates white pixels whose output is D digits or more when 12 bits output.

2. Adjacent blooming white pixels in the dark

For patterns of white pixels and blooming white pixels, the following measurement method is applied.

(1) Acquire dark signal output in integration time of 2 s.

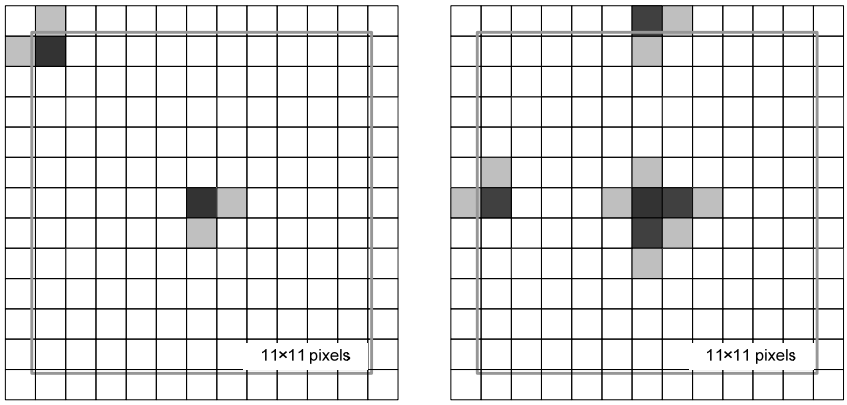
(2) Define the pixels that satisfy the following conditions as blooming white pixels, and detect them.

(a) The output is 3824 digit or more when 12 bits output.

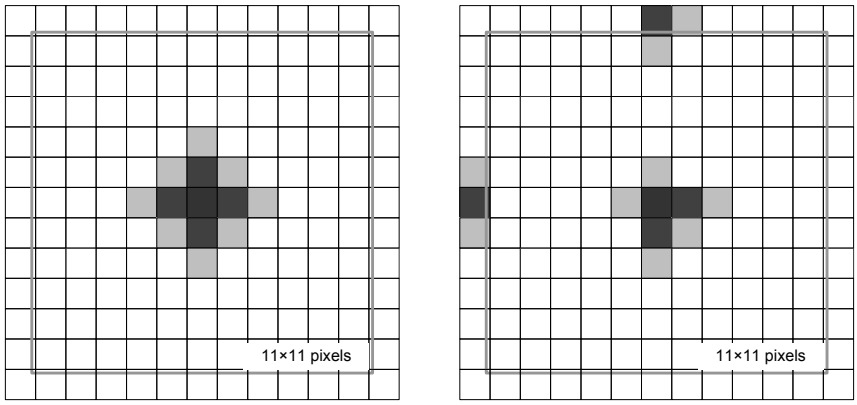
(b) The number of pixels whose output is D digit or more when 12 bits output, within the adjacent 4 pixels in horizontal and vertical direction of (a) pixel, is two or more.

(3) Define the cases as adjacent blooming white pixel, when other blooming white pixel exists in the zone of 11 × 11 pixels whose center is one of blooming white pixels defined above, and count them. However the pixels whose horizontally or vertically next pixel is other blooming white pixel are not counted, regarding as a single blooming white pixel.

Example of adjacent blooming white pixels



Example of not counted as adjacent blooming white pixels



■ indicates white pixels whose output is 3824 digits or more when 12 bits output.

■ indicates white pixels whose output is D digits or more when 12 bits output.

3. Serial blooming white pixels in the dark

For patterns of white pixels and blooming white pixels, the following measurement method is applied.

(1) Acquire dark signal output in integration time of 2 s.

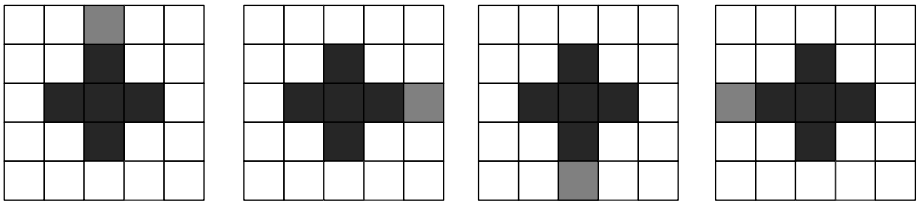
(2) Define the pixels that satisfy the following conditions as serial blooming white pixels, and count them.

(a) The output is 3824 digit or more when 12 bits output.

(b) The outputs of adjacent 4 pixels in horizontal and vertical directions are 3824 digit or more when 12 bits output.

(c) The number of pixels whose output is D digits or more when 12 bits output, at the next position in the same direction of the above (b) pixels, is one or more.

Example of serial blooming white pixels



indicates white pixels whose output is 3824 digits or more when 12 bits output.

indicates white pixels whose output is D digits or more when 12 bits output.

Marking

T.B.D

List of Trademark Logos and Definition Statements

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.

Revision History

Date of change	Revisiton.	Page	Contain of Change
2016/12/27	0.1	—	First edition