USB2.0 Video Class

WebCamera Controller

SN9C2730(XJ556JG)

Datasheet

Document No.-

Version 0.11

For the latest data sheet, please visit www.sunnywale.com

Revision	Date	Description
0.11	15-05-19	add new feature in color processing
0.10	15-04-30	Initial draft of SN9C2730(XJ556JG)

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1 General Description

SN9C2730(XJ556JG) is a USB 2.0 High-Speed compatible camera controller. The advanced power design provides low power consumption whenever device is under suspend, standby or operation mode. The low thermal design makes the module operating temperature inside platform under reasonable range. The SN9C2730(XJ556JG) is fully compliant with
USB Video Class. The supported OS includes Microsoft (Windows XP, Vista, 7 and 8/8.1.), Mac OS and Linux (Ubuntu. Android...etc.)

SN9C2730(XJ556JG) support 2 kinds of sensor interface(MIPI-CSI2 1 lane & Parallel 10bits, exclusively) for application. Resolution is up to HD@30fps. The new generation image signal processor brings better visual experience. The high performance Motion-JPEG engine provides variant compression ratio to meet bandwidth requirement. With the integrated sensor interface and color processing engine, it can supports most available CMOS sensors. It is controlled by the embedded micro-controller and the statistics for 2A (AE / AWB) are built-in. The flexible architecture is constituted by mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to fulfill customized features.

2 Features

2.1 System

- 3.3V single power supply
- Extreme low power consumption
  - standby: < 30mA (sensor is excluded)
  - suspend: <500uA (sensor is excluded)
- Built-in Clock Synthesizer for performance and power saving
- Built-in PLL for internal clock generation
- Using external serial flash to store customized code and data(default 64KBytes)
- High speed serial flash controller (60MHz) with phase detection
- External RAM is unnecessary
- 1.8V output power to supply CMOS sensor's I/O power
- 2.8V output power to supply CMOS sensor's analog power (2.7V~3.3V control by FW setting)
- 32-pins QFN 3x6mm package
- With 3 GPIO

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 compliant

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- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- Support device power state - Runtime D3 of ACPI
- 3 endpoints: CONTROL pipe, UVC Interrupt IN and Isochronous-IN (video, 24MB/s max)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- MIPI-CSI2 1-lane & Parallel(10bits), exclusively: HD(1280x800), VGA(640x480) CMOS sensor
- Support both YUY2 and Bayer RAW image data format from sensor interface
- Up to 80MHz pixel clock
- Support industrial standard 2-wire serial interface for sensor control

2.4 Color Processing

- AE histogram statistics
- AWB window statistics
- On-the fly defect-pixel cancellation
- Lens shading compensation for R/G/B channel
- Low pass filter
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Programmable gamma table for RGB channels
- Programmable color conversion matrix for R/G/B input
- Configurable noise reduction
- De-color aliasing in Edge
- Configurable edge enhancement
- Programmable gamma table for Y channel
- Configurable windowing function after processed image
- Programmable hue and saturation
- Auto Gamma for backlight preview
- Auto Frequency for MSOC
- Improved dynamic range adjustment

2.5 Scaling Engine

- Scale down on Y/Cb/Cr
- For SXGA / VGA sensors, combined scaling and windowing function provides similar view angle for SXGA / HD / SVGA / VGA / CIF / QVGA / QCIF / QQVGA output format
- With LPF to eliminate artifact

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2.6 JPEG Encoder

- JPEG format is YUV422 baseline
- Built-in JPEG encoder to support USB Video Class MJPEG payload
- Programmable 128 bytes quantization table for Y and C to adjust compression ratio

2.7 Video Image

- Support UVC1.1 - Uncompressed YUY2 payload (YUV422, 16bits/pixel)
- Support UVC1.1 - MJPG payload
- Video streaming up to 30fps@HD at USB2.0 high-speed mode

2.8 Frame rate

Mode	HD	SVGA	VGA	CIF	QVGA
MJPEG	30	60	60	60	60
YUV	12	25	30	30	30

2.9 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory
- Maximum CPU clock rate is48MHz
- Auto load extended F/W from external serial flash
- Auto load VID/PID, manufacturer, product and serial number string from external serial flash
- Auto load UVC parameter definition from external serial flash
- Firmware is upgradeable from PC
- Able to force USB at FS mode & USB disconnect
- Watch dog to auto recovery
- With interrupt when sensor image transferring is finished of each frame

2.10 Pre-Defined for USB Video Class

- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- White Balance Temperature (UVC defined)
- Backlight Compensation (UVC defined)
- Gain (UVC defined)
- Power Line Frequency (UVC defined)
- White Balance Temperature, Auto (UVC defined)

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- Auto-Exposure Mode (UVC defined)
- Auto-Exposure Priority (UVC defined)
- Wxposure Time(Absolute), (UVC defined)
- LED indicator on video streaming
- UVC Extension unit support

2.11 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit, Microsoft Window 7 32bit, Microsoft Window 7 64bit, Microsoft Window 8
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

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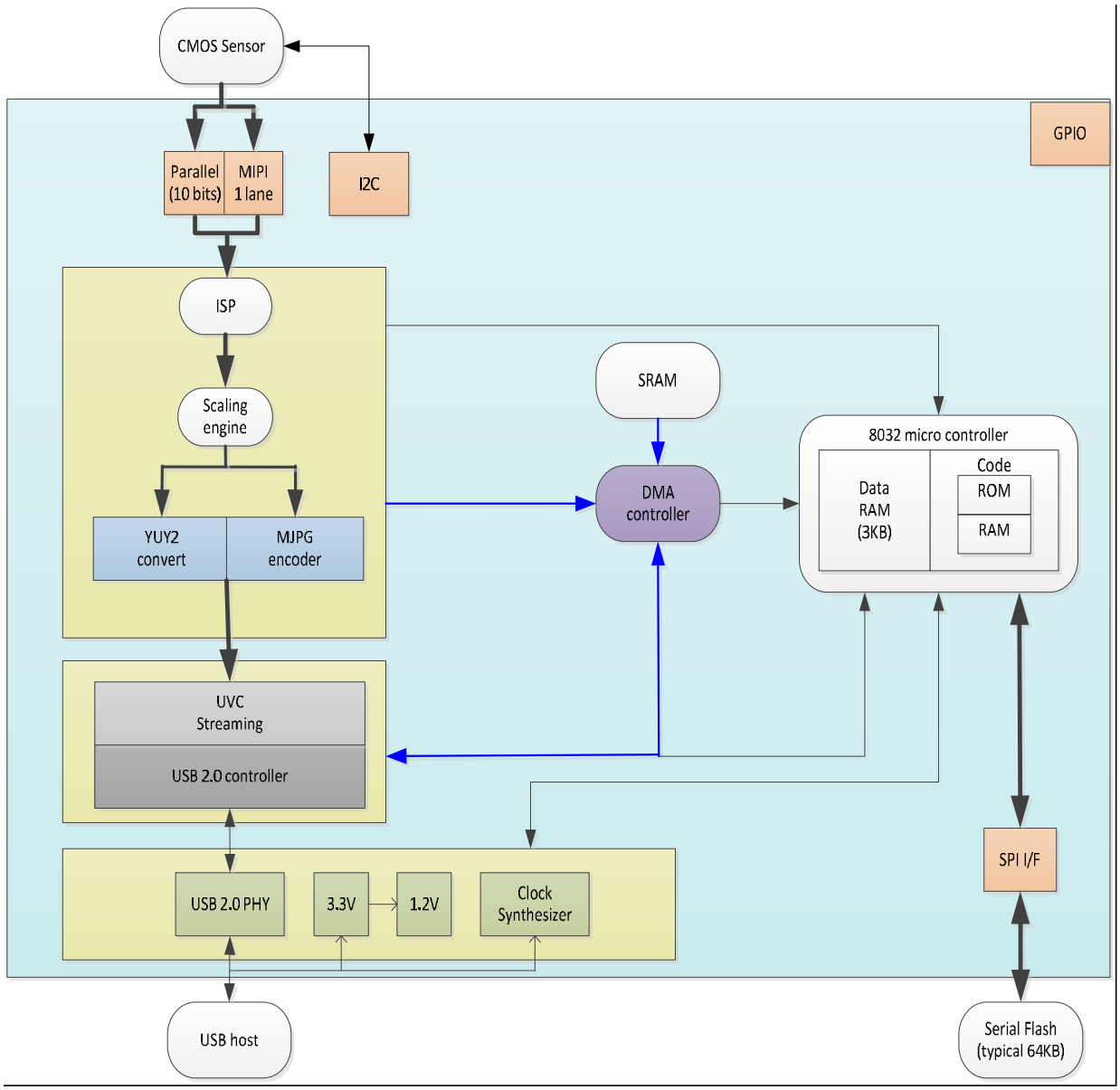
3 Function Block Diagram



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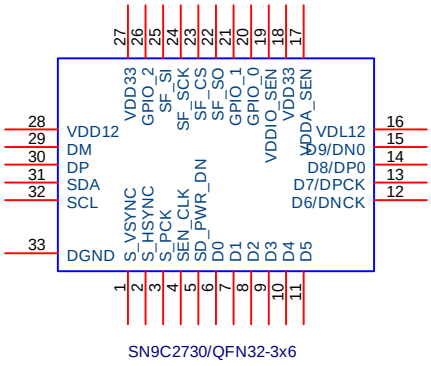
4 Pin Assignment

4.1 SN9C2730(XJ556JG) - QFN32

4.1.1 Pin-Out Diagram



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4.1.2 Pin-Out Description

Pin No.	Pin Name	Mode			Description
		Power Up	Normal	Suspend	
1	S_VSYNC	I	I	PD	Parallel sensor vsync.
2	S_HSYNC	I	I	PD	Parallel sensor hsync.
3	S_PCK	I	I	PD	Parallel sensor pixel clock.
4	SEN_CLK	O	O	O	Sensor clock.
5	SD_PWR_DN	I	O	O	General purpose I/O. Default for sensor power down control.
6	D0	I	I	PD	Parallel sensor image data.
7	D1	I	I	PD	Parallel sensor image data.
8	D2	I	I	PD	Parallel sensor image data.
9	D3	I	I	PD	Parallel sensor image data.
10	D4	I	I	PD	Parallel sensor image data.
11	D5	I	I	PD	Parallel sensor image data.
12	D6/DNCK	I/A	I/A	PD/A	Combo sensor interface.
13	D7/DPCK	I/A	I/A	PD/A	Combo sensor interface.
14	D8/DP0	I/A	I/A	PD/A	Combo sensor interface.
15	D9/DN0	I/A	I/A	PD/A	Combo sensor interface.
16	VDD12	P	P	P	DSP core power.
17	VDDA_SEN	P	P	P	Sensor analog power supply. Default 2.8V.
18	VDD33	P	P	P	DSP system power.
19	VDDIO_SEN	P	P	P	Sensor I/O power supply. Default 1.8V.
20	GPIO_0	I	B	PD	General purpose I/O. Default for LED control.
21	GPIO_1	I	B	PD	General purpose I/O. Default for SPI serial flash write protect control.
22	SF_SO	O	O	O	SPI data out to serial flash.
23	SF_CS	O	O	O	SPI chip select to serial flash.
24	SF_SCK	O	O	O	SPI clock to serial flash.
25	SF_SI	I	I	PD	SPI data in from serial flash.
26	GPIO_2	I	B	PD	General purpose I/O.
27	VDD33	P	P	P	DSP system power.
28	VDD12	P	P	P	DSP core power.
29	DM	A	A	A	USB D-.
30	DP	A	A	A	USB D+.
31	SDA	I	B	PD	I2C data for sensor.
32	SCL	I	B	PD	I2C clock for sensor.

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5 Electrical Characteristicsa

5.1 DC Operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD33_18	Power Supply	-0.3 ~ 3.6	V
DVDD	Power Supply	-0.12 ~ 1.32	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Typ	Units
VDD33	Power Supply	3.3	V
VDD33_18	Power Supply	3.3/1.8	V
DVDD	Power Supply	1.2	V
Vin	Input voltage	3.3	V

5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and
VDD33=3.0 ~ 3.6V, VDD33_18=1.62 ~ 3.6V, Ta=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil (VDD33)	Input low voltage	CMOS	-0.3		0.2*VDD33	V
Vih(VDD33)	Input high voltage	CMOS	0.8*VDD33		VDD33+0.3	V
Vil (VDD33_18)	Input low voltage	CMOS	-0.3		0.2*VDD33_18	V
Vih(VDD33_18)	Input high voltage	CMOS	0.8*VDD33_18		VDD33_18+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF

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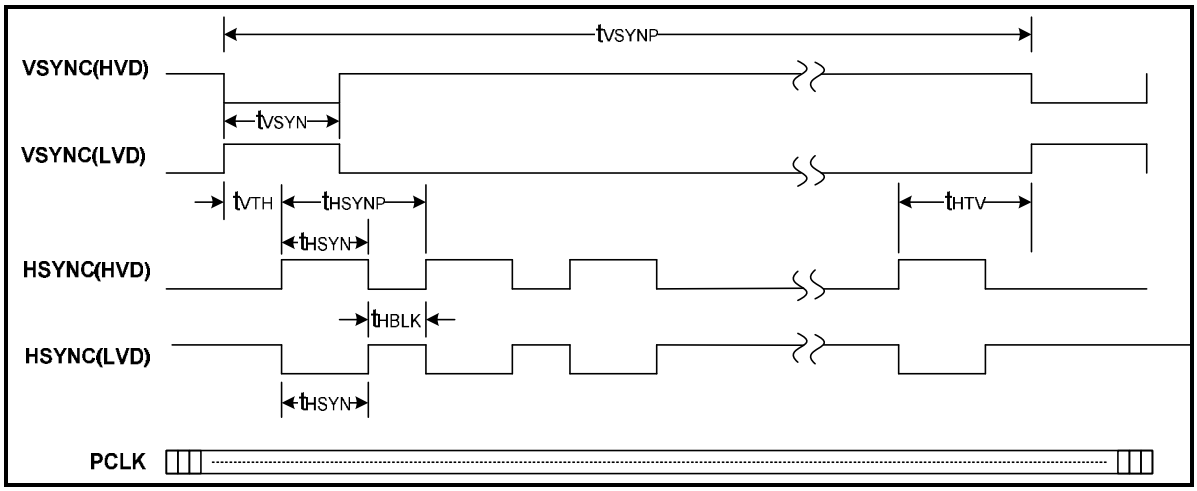
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.2 AC Operating Condition

5.2.1 Parallel Sensor Interface



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	tVSYNC	tPCLK	-	-	ns
VSYNC to HSYNC	tVTH	tPCLK	-	-	ns
HSYNC pulse width	tHSYN	tPCLK	-	-	ns
Blank time between two HSYNC	tHBLK	tPCLK	-	-	ns
HSYNC to VSYNC	tHTV	tHSYNP			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

SYNC_MODE = 1 : **(PCLK is free run)**

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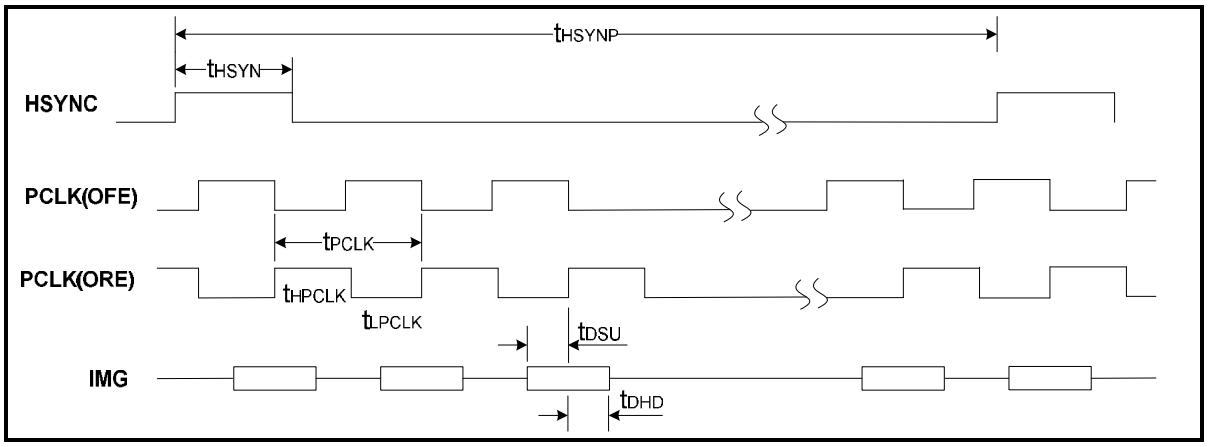
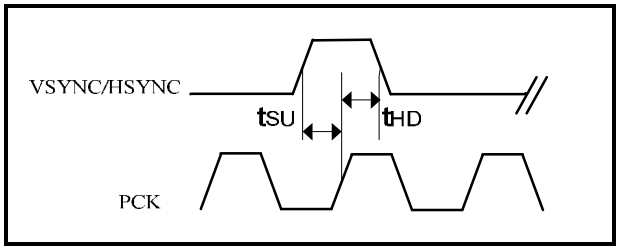


Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	tSU	2	-	-	ns
VSYNC / HSYNC hold time	tHD	2	-	-	ns

SYNC_MODE = 0 : **(PCLK is output only when hsync active)**

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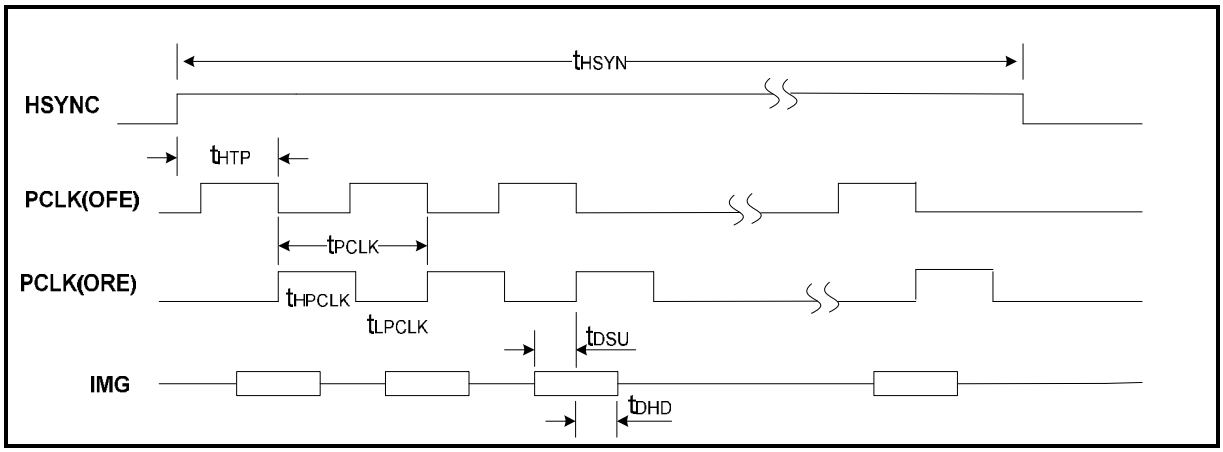


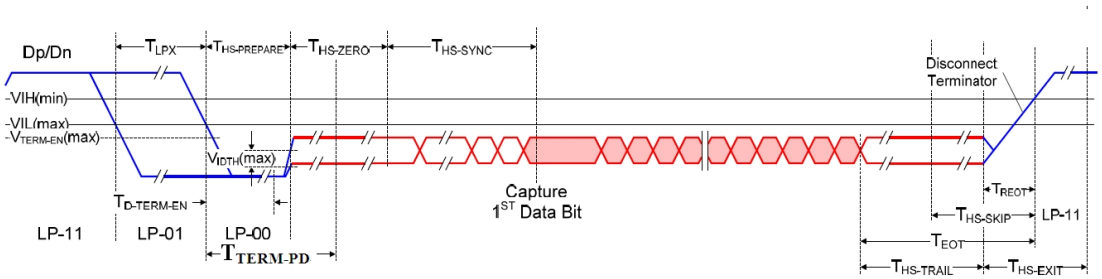
Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	HSIZE * tPCLK	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}	-	-	
PCLK Low Pulse Width	t_{LPCLK}	2.0	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2.0	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge
4. HSIZE represents total valid PCLK number per horizontal line

5.2.2 MIPI Sensor Interface

n High-speed Data Transmission



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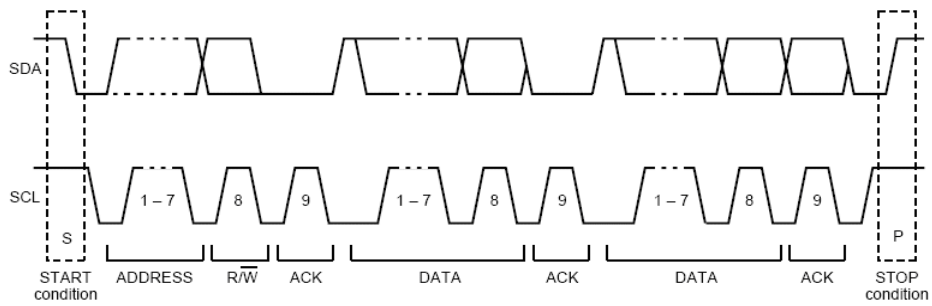
- MIPI Operation Timing Parameters

Parameter	Min	Max	Unit
$T_{LPX(1)}$	66		ns
$T_{HS\text{-}PREPARE(2)}$	66	85ns + 6*$UI_{(3)}$	ns
$T_{HS\text{-}ZERO(4)}$	120	2*[$T_{HS\text{-}EXIT}$ – (110ns+10*UI)]	ns
$T_{HS\text{-}TRAIL(5)}$	16*UI		ns
$T_{HS\text{-}EXIT(6)}$	240ns + 110*UI		ns
$T_{EOT(7)}$	16*UI	105ns + 12*UI	ns

1. T_{LPX} is the time from the end of LP-11state to the start of LP-00 state.
2. $T_{HS\text{-}PREPARE}$ is the time from the start of LP-00 to the start of the HS-0 state.
3. UI is the one data bit time.
4. $T_{HS\text{-}ZERO}$ is the time during HS-0 state.
5. $T_{HS\text{-}TRAIL}$ is the time that the transmitter drives the differential state after last data bit of HS burst.
6. $T_{HS\text{-}EXIT}$ is the time from the end of $T_{HS\text{-}TRAIL}$ to the start of the LP-01 of the next packet.
7. T_{EOT} is the time from the end of $T_{HS\text{-}TRAIL}$ to Low-Power state that mean DP = 1 and DN = 1.

- Note1: The ranges of the red marked parameters for the above table must be satisfied. The other parameters can reference the document of MIPI Alliance Specification for DPHY.
- Note2: $T_{TERM\text{-}PD}$ is the time from termination enable to the release of power down. The range of $T_{TERM\text{-}PD}$ is from ($T_{HS\text{-}PREPARE}$ + 33 ns) to ($T_{HS\text{-}ZERO}$ + $T_{HS\text{-}PREPARE}$ – 33ns) and the suggestion value is the min($T_{HS\text{-}PREPARE}$ + 0.5*$T_{HS\text{-}ZERO}$, 495ns).

5.2.3 I2C Control Interface



A complete data transfer.

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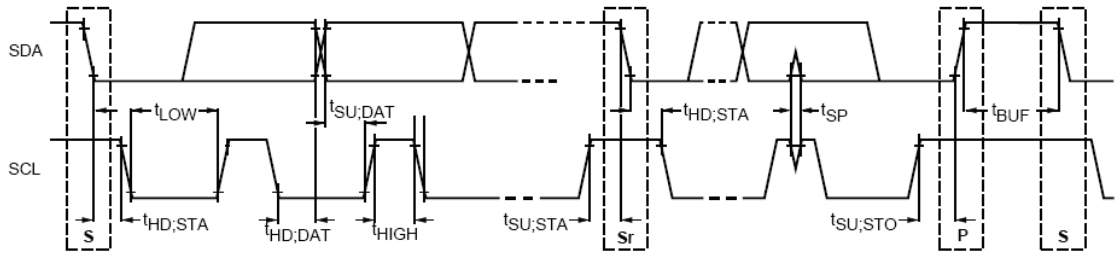
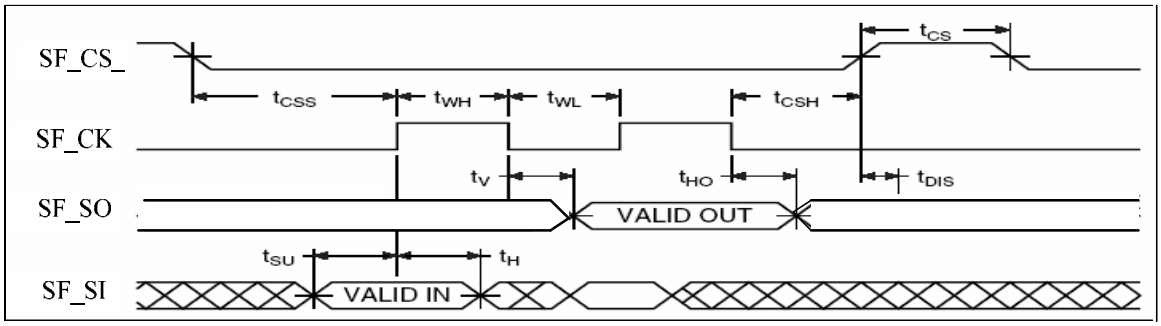


Definition of timing for F/S-mode devices on the I²C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.4 Serial Flash Interface



When fSCK = 24 Mhz (SPEED=1)

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Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

When fSCK = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

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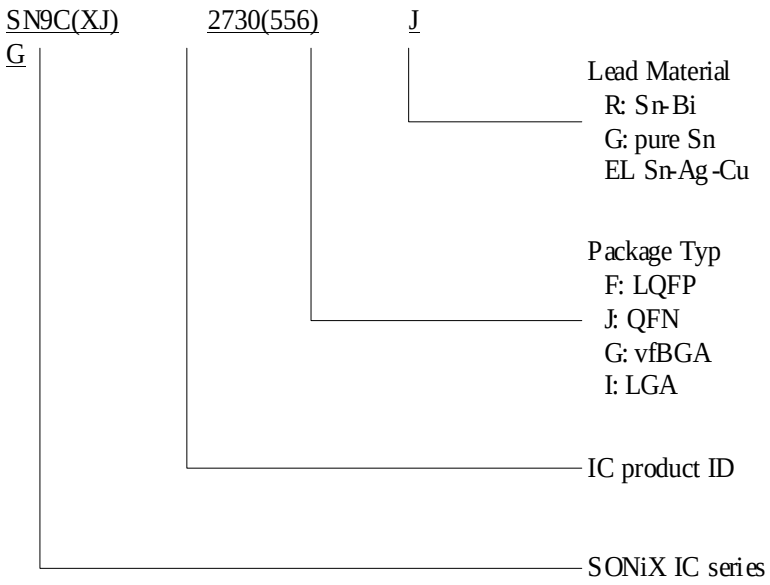
6 Package

6.1 Nomenclature



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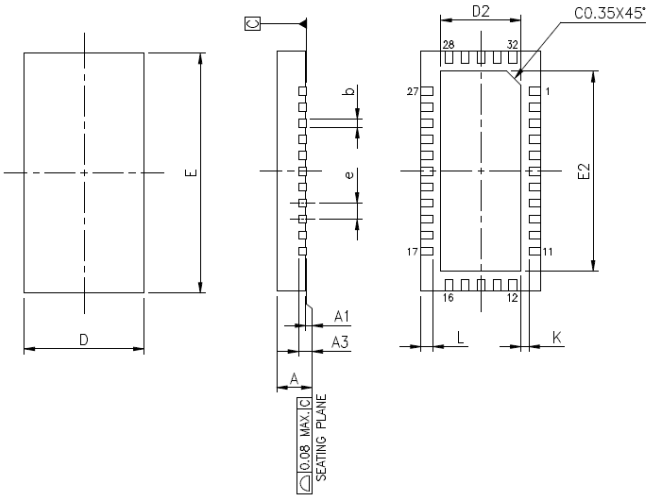
6.2 SN9C2730 - QFN32

6.2.1 Drawing



6.2.2 Dimension

SYMBOLS	MIN.	NOM.	MAX.	NOTES:
A	0.80	0.85	0.90	1. JEDEC CODE: N/A
A1	0.00	0.02	0.05	
A3	0.203 REF			
b	0.15	0.20	0.25	
D	3.00 BSC			
E	6.00 BSC			
e	0.40 BSC			
D2	1.90	2.00	2.05	
E2	4.90	5.00	5.05	
L	0.20	0.30	0.40	
K	0.20	-	-	

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