SONY

Signal Processing LSI for Single CCD Color Camera

CXD4140GG

Description

The CXD4140GG is a signal processing LSI for Ye, Cy, Mg and G single CCD color cameras.
In addition to basic camera signal processing functions, it includes 2DNR, an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.
This chip realizes basic camera control functions such as AE/AWB with an internal RISC-CPU.

Applications

- Industrial CCD cameras (Surveillance/FA/image input cameras)
- Multimedia CCD cameras (Teleconferencing/personal computer cameras)

Features

- ◆ Generates sync signals for the single CCD camera
  - Luminance signal processing
  - Chroma signal processing
- ◆ Supports NTSC/PAL systems
- ◆ Supports 510H system, 760H system and 960H system CCD image sensor
- ◆ Analog video output pin
  - Y/C composite, Y/C separate (Built-in 12-bit D/A converter)
- ◆ YCrCb digital output pin
  - Conforms to ITU-R BT.656
- ◆ Supports external sync functions
  - Line-locked function (Built-in phase comparator)
- ◆ Built-in AE/AWB/AF detector
- ◆ Block control functions with an internal RISC-CPU
  - AE/ AWB/ YC/ CLAMP/ SG/ dynamic defect detection and compensation/ static defect detection and compensation/ HLC
- ◆ Peripheral IC control function
  - CXD5148GG
  - EEPROM
- ◆ Serial communication function (2-mode selection)
  - Microcomputer communication/start-stop synchronous system communication (RS-232C)
- ◆ Mirror inversion function
- ◆ Motion detection function
- ◆ Noise reduction
- ◆ Gradation conversion
- ◆ OSD menu multi-language supported

Effio™

* “Effio” is a trademark of Sony Corporation. The “Effio” is a signal processor chip from Sony employing processing modes that deliver high resolution, high S/N ratio and excellent color reproduction.

Package

97-pin plastic LFBGA (8 mm × 8 mm, 0.65 mm pitch)

Applicable CCD Image Sensors

◆ 510H color CCDs (Type 1/3, 1/4, NTSC/PAL)
◆ 760H color CCDs (Type 1/2, 1/3, 1/4, NTSC/PAL)
◆ 960H color CCDs (Type 1/3, NTSC/PAL)

Supported Related LSI

◆ TG/AFE: CXD5148GG
◆ EEPROM: Renesas Technology Corp. R1EX25064

Absolute Maximum Ratings

◆ Supply voltage	DV_{DD}	DV_{SS} – 0.5 to +2.0	V
	VDE	DV_{SS} – 0.5 to +4.5	V
	ADVD	ADVS – 0.5 to +4.5	V
	AVD	AVS – 0.5 to +4.5	V
◆ Input voltage	V_I	DV_{SS} – 0.3 to VDE + 0.3	V
◆ Output voltage	V_O	DV_{SS} – 0.3 to VDE + 0.3	V
◆ Operating temperature	Topr	–20 to +75	˚C
◆ Storage temperature	Tstg	–55 to +125	˚C
◆ Allowable power dissipation	P_D	400	mW

Recommended Operating Conditions

◆ Supply voltage	DV_{DD}	1.1 to 1.3	V
	VDE, ADVD	3.0 to 3.6	V
	AVD	3.0 to 3.6	V
◆ Operating temperature	Topr	–20 to +75	˚C

Notes on Handling

Use Restrictions

◆ The Products are intended for incorporation into such general electronic equipment as general CCTV surveillance, image input cameras, FA cameras, teleconferencing cameras and personal computer cameras in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.

◆ You should not use the Products for critical applications, as car use products, which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. In addition, you should not use the Products in weapon or military equipment.

◆ Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

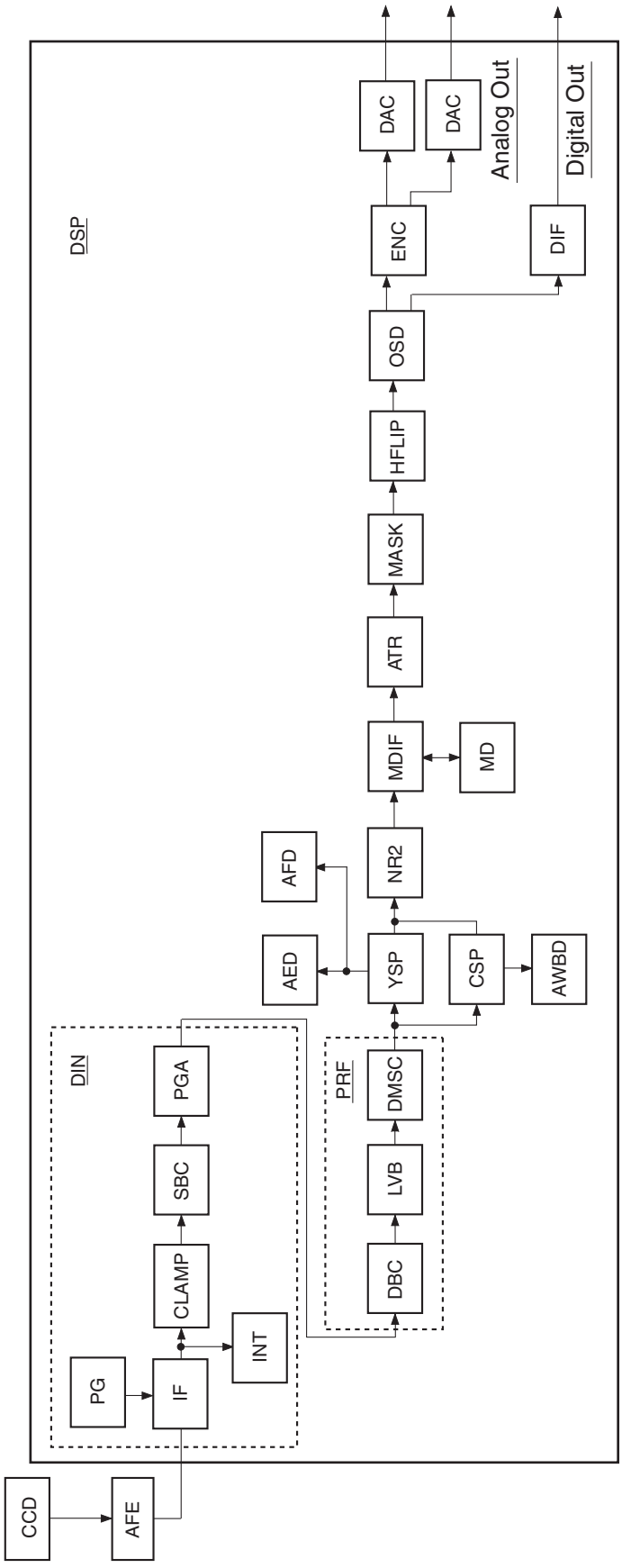
Design for Safety

◆ Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent misoperation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Other Applicable Terms and Conditions

◆ The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book.
You should review those terms and conditions when you consider purchasing and/or using the Products.

Block Diagram



IF : Digital Interface
PG : Pattern Generator
INT : Integration
CLAMP : Digital Clamp
SBC : Static Blemish Compensation
PGA : DSP AGC
DBC : Dynamic Blemish Compensation
LVB : Level Balance
DMSC : Demosaic
YSP : Luminance Signal Processing
CSP : Chroma Signal Processing
AED : AE Detector
AFD : Auto Focus Detector
AWBD : AWB Detector

NR2 : 2D Noise reduction
MDIF : Motion Detector Interface
MD : Motion Detector
ATR : Adaptive Tone Reproduction
MASK : Privacy Masking
HFLIP : Horizontal Flip
OSD : On Screen Display
ENC : Analog Out processing
DIF : Digital Out processing
DAC : Digital Analog Convertor

Pin Configuration

(Top View)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	CAMSO	CAMCS AFE	CAMSI	EXCS	EXSI	EXSCK	PB0	PB2	PB4	NC	A
B	AFECK	AD0	CAMSCK	CAMCS EEPROM	EXBUSY	EXSO	DVss	PB1	PB3	PB5	PB6	B
C	AD1	AD2								PB7	DCKO	C
D	AD3	AD4		DVDD	DVDD	DVSS	DVSS	ADVS		ADVS	SIFSEL	D
E	AD5	AD6		DVDD	VDE	DVSS	DVSS	ADVD		EVR0	EVR1	E
F	AD7	AD8		DVDD	VDE	DVSS	AVD	ADVD		VGC	IOC	F
G	AD9	AD10		DVDD	VDE	DVSS	AVD	AVS		AVS	IREFC	G
H	TGCK	AD11		DVDD	DVDD	DVSS	DVSS	DVss		IOY	VREFY	H
J	TGVD	TGHD								IREFY	VGY	J
K	NC	PA0	PA1	PA2	PA5	PA7	XRST	ECKO SCO	ECKSEL	PCOMP1	PCOMP2	K
L	NC	DVss	PLLCK	PA3	PA4	PA6	ECKO SCI	DVss	DCKI	VRI	NC	L
	1	2	3	4	5	6	7	8	9	10	11	

Pin Description

Symbol	Pin No.	I/O	Description	I/O type
AD0	B2	I	External A/D signal input	[Input] cmos
AD1	C1	I	External A/D signal input	[Input] cmos
AD2	C2	I	External A/D signal input	[Input] cmos
AD3	D1	I	External A/D signal input	[Input] cmos
AD4	D2	I	External A/D signal input	[Input] cmos
AD5	E1	I	External A/D signal input	[Input] cmos
AD6	E2	I	External A/D signal input	[Input] cmos
AD7	F1	I	External A/D signal input	[Input] cmos
AD8	F2	I	External A/D signal input	[Input] cmos
AD9	G1	I	External A/D signal input	[Input] cmos
AD10	G2	I	External A/D signal input	[Input] cmos
AD11	H2	I	External A/D signal input	[Input] cmos
CAMSCK	B3	O	Serial clock for peripheral IC communication	[Output] 4 mA
CAMSI	A4	I	Serial data input for peripheral IC communication	[Input] schmitt
CAMSO	A2	O	Serial data output for peripheral IC communication	[3-state] 4 mA
CAMCSAFE	A3	O	AFE chip select	[Output] 2 mA, 4 mA selectable *1
CAMCSEEPROM	B4	O	EEPROM chip select	[Output] 2 mA, 4 mA selectable *1
EXSCK	A7	I	Serial clock for external microcomputer communication	[Input] schmitt, built-in pull-up resistor
EXSI	A6	I	Serial data input/UART receive data input for external microcomputer communication	[Input] schmitt, built-in pull-up resistor
EXSO	B6	O	Serial data output/UART receive data output for external microcomputer communication	[3-state] 4 mA
EXCS	A5	I	Chip select for external microcomputer communication	[Input] schmitt, built-in pull-up resistor
EXBUSY	B5	O	BUSY signal for external microcomputer communication	[Output] 4 mA
SIFSEL	D11	I	External microcomputer communication, UART communication selectable (0: External microcomputer, 1: UART)	[Input] cmos, built-in pull-down resistor
TGCK	H1	I	Sensor drive clock input	[Input] schmitt
TGHD	J2	O	Horizontal sync signal output for timing generator	[Output] 2 mA, 4 mA selectable *1
TGVD	J1	O	Vertical sync signal output for timing generator	[Output] 2 mA, 4 mA selectable *1
AFECK	B1	O	Output clock to external AFE	[3-state] 2 mA, 4 mA selectable *1
XRST	K7	I	System reset	[Input] schmitt

Symbol	Pin No.	I/O	Description	I/O type
PA0	K2	I/O	Port A/Vertical sync signal output (HD for external AFD, VD for external sync) *2	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA1	K3	I/O	Port A/Horizontal sync signal output (HD for external AFD) *2	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA2	K4	I/O	Port A /SYNC signal output (SYNC for video servo)*2	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA3	L4	I/O	Port A, VALIDFLD	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA4	L5	I/O	Port A	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA5	K5	I/O	Port A	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA6	L6	I/O	Port A	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PA7	K6	I/O	Port A	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB0	A8	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB1	B8	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB2	A9	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB3	B9	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB4	A10	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB5	B10	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB6	B11	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in pull-up resistor*1
PB7	C10	I/O	Port B/Digital out/External AFD data output	[I/O] 2 mA, 4 mA selectable, cmos, built-in built-in pull-up resistor resistor*1
PCOMP1	K10	O	Phase comparison output for VPLL (analog side)	Charge Pump (2 mA)

Symbol	Pin No.	I/O	Description	I/O type
PCOMP2	K11	O	No connection	
VRI	L10	I	External sync signal input	[Input] cmos, built-in pull-up resistor
IREFY	J10	O	Reference current setting (for YDAC)	[Output] Analog
VREFY	H11	I	Reference voltage setting	[Input] Analog
IOY	H10	O	Luminance signal (current) output/ Composite output (for YDAC)	[Output] Analog
VGY	J11	O	Capacitor connection for luminance (for YDAC)	[Output] Analog
IREFC	G11	O	Reference current setting (for CDAC)	[Output] Analog
IOC	F11	O	Chroma signal (current) output (for CDAC)	[Output] Analog
VGC	F10	O	Capacitor connection for chroma (for CDAC)	[Output] Analog
EVR0	E10	O	Mechanical iris EVR0 output	[Output] Analog
EVR1	E11	O	Mechanical iris EVR1 output	[Output] Analog
DCKO	C11	O	Digital out clock/External AFD clock output	[Output] Analog
DCKI	L9	I	DCK oscillator input	[Input] cmos
ECKOSCI	L7	I	ECK oscillator input	Oscillator
ECKOSCO	K8	O	ECK oscillator output	
ECKSEL	K9	I	ECK connection destination selection (0: Oscillator connection, 1: Clock direct input)	[Input] cmos, built-in pull-down resistor
PLLCK	L3	I	PLL clock input	[Input] cmos
DV_{DD}	D4	PWR	Digital power supply (1.2 V)	Core power supply
	D5			
	E4			
	F4			
	G4			
	H4			
	H5			
VDE	E5	PWR	Digital I/O power supply (3.3 V)	I/O power supply
	F5			
	G5			
AVD	F7	PWR	DAC analog power supply (3.3 V)	I/O power supply
	G7			
ADVD	E8	PWR	DAC digital power supply (3.3 V)	I/O power supply
	F8			

Symbol	Pin No.	I/O	Description	I/O type
DVSS	B7	GND	Digital GND	Digital GND
	D6			
	D7			
	E6			
	E7			
	F6			
	G6			
	H6			
	H7			
	H8			
	L2			
	L8			
AVS	G8	GND	DAC analog GND	Analog GND
	G10			
ADVS	D8	GND	DAC digital GND	Digital GND
	D10			

*1 Output drive capability can be selected by parameter setting. For details, see the application note.

*2 Arbitrary function can be selected by register setting. For details, see the application note.

Electrical Characteristics

DC Characteristics (within the recommended operating range)

Item		Symbol	Pin	Measurement conditions	Min.	Typ.	Max.	Unit
Digital I/O supply voltage		VDE	VDE, ADVD	—	3	3.3	3.6	V
Analog supply voltage		AVD	AVD	—	3	3.3	3.6	V
Digital supply voltage		DV_{DD}	DV_{DD}	—	1.1	1.2	1.3	V
Input voltage	3.3 V CMOS input	V_{IH}	CMOS input*1	—	VDE × 0.7	—	VDE + 0.3	V
		V_{IL}		—	–0.3	—	VDE × 0.3	V
	3.3 V Schmitt input	Vt+	Schmitt input*1	—	VDE × 0.7	—	VDE + 0.3	V
		Vt–		—	–0.3	—	VDE × 0.3	V
		Vt+ – Vt–		—	—	0.35	—	V
Output voltage	3.3 V CMOS output	V_{OH}	CMOS output (2 mA)*1	I_{OH} = –2mA	VDE – 0.4	—	—	V
		V_{OL}		I_{OL} = 2mA	—	—	0.4	V
	3.3 V CMOS output	V_{OH}	CMOS output (4 mA)*1	I_{OH} = –4mA	VDE – 0.4	—	—	V
		V_{OL}		I_{OL} = 4mA	—	—	0.4	V
Input leakage current	Normal input pin	I_I	CMOS input*1 Schmitt input*1	VIN = DV_{SS} or VDE	–10	—	10	µA
	With pull-up resistor	I_{IL}		VIN = DV_{SS}	–240	—	—	µA
	With pull-down resistor	I_{IH}		VIN = VDE	—	—	240	µA
Output leakage current	Tri-state output pin (when high impedance)	I_{OZ}	CMOS output*1	VIN = DV_{SS} or VDE	–10	—	10	µA
	With pull-up resistor (when high impedance)	I_{OZL}		VIN = DV_{SS}	–240	—	—	µA

*1 For the applicable pins, see the “I/O type” in Pin Description.

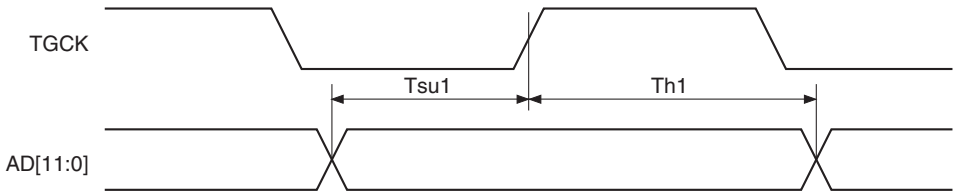
I/O Capacitance

Item	Symbol	Pin	Min.	Typ.	Max.	Unit
Input pin capacitance Output pin capacitance I/O pin capacitance	CIO	CMOS input*1 Schmitt input*1 CMOS output*1	—	—	6	pF
Output pin capacitance	CCAM	CAMSCK, CAMSO	—	—	11	pF

*1 For the applicable pins, see the “I/O type” in Pin Description. However, CAMSCK and CAMSO are excluded.

AC Characteristics

◆ AD pin

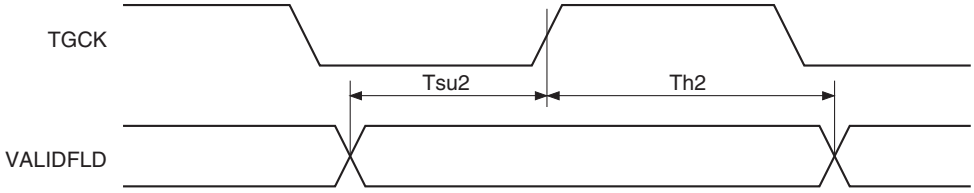


(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Input setup time	Tsu1	AD[11:0]	12.6	—	—	ns
Input hold time	Th1		0	—	—	ns

◆ VALIDFLD pin

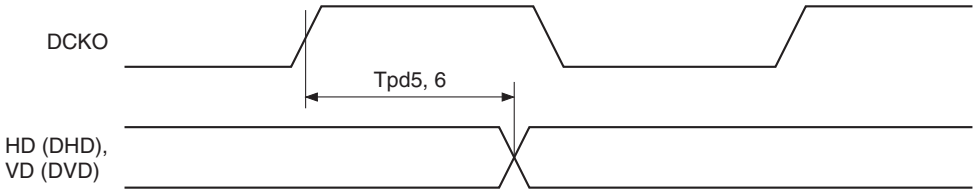
Shared with PA[3] pin, this is defined as PA[3] pin specification.



(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Input setup time	Tsu2	VALIDFLD (PA[3])	12.6	—	—	ns
Input hold time	Th2		0	—	—	ns

◆ TGHD, TGVD pins

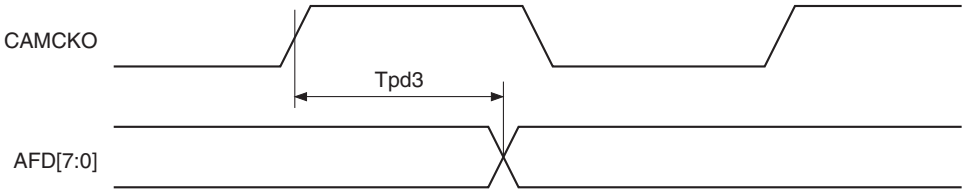


(within the recommended operating range, TGHD, TGVD load capacitance = 15.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd1	TGHD	1	—	17.6	ns
	Tpd2	TGVD	1	—	17.6	ns

◆ AFD pin

Shared with PB pin, this is defined as PB pin specification.
In addition, shared with DCKO pin, CAMCKO is defined as DCKO pin specification.

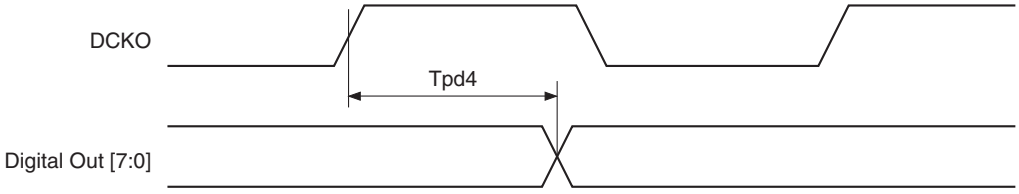


(within the recommended operating range, DCKO, PB[7:0] load capacitance = 14.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd3	AFD[7:0] (PB[7:0])	5	—	35.6	ns

◆ Digital Out pin

Shared with PB pin, this is defined as PB pin specification.

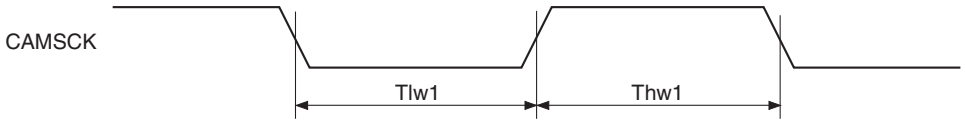


(within the recommended operating range, DCKO, PB[7:0] load capacitance = 15.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd4	Digital Out (PB[7:0])	10.9	—	16.9	ns

◆ CAMSCK pin

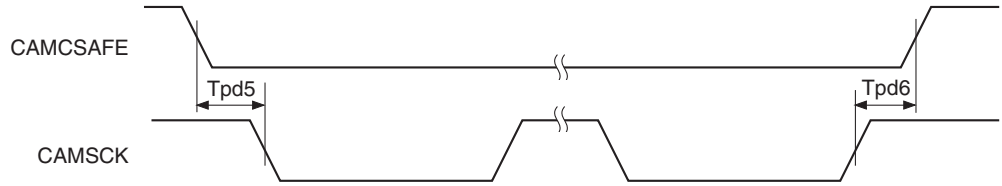
CAMSCK, CAMCSAFE, CAMCSEEPROM, CAMSI and CAMSO pins are signals for performing serial communication with the peripheral ICs.



(within the recommended operating range, CAMSCK load capacitance = 29 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output pulse width (High period)	Thw1	CAMSCK	131	—	260	ns
Output pulse width (Low period)	Tlw1		131	—	260	ns
Frequency	Fsck		1.929	—	3.814	MHz

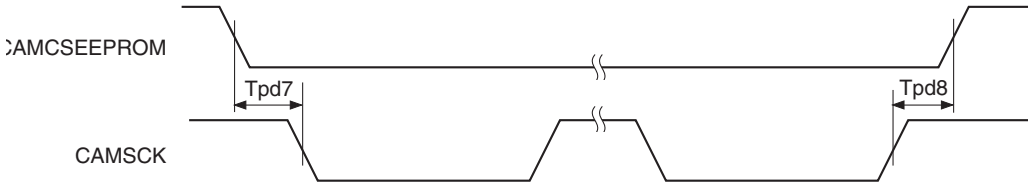
◆ **CAMCSAFE pin**



(within the recommended operating range, CAMSCK load capacitance = 29 pF, CAMCSAFE load capacitance = 15.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Falling edge of CAMCSAFE to falling edge of CAMSCK	Tpd5	CAMCSAFE	252.59	—	—	ns
Rising edge of CAMSCK to rising edge of CAMCSAFE	Tpd6		119.94	—	—	ns

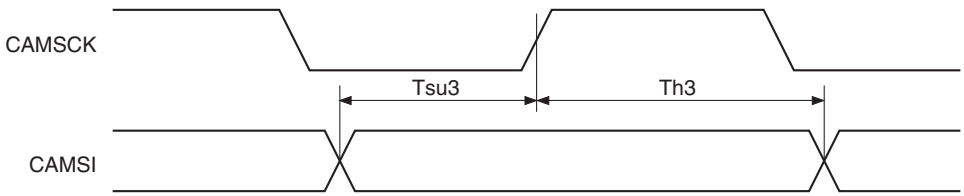
◆ **CAMCSEEPROM pin**



(within the recommended operating range, CAMSCK load capacitance = 29 pF, CAMCSEEPROM load capacitance = 15.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Falling edge of CAMCSEEPROM to falling edge of CAMSCK	Tpd7	CAMCSEEPROM	252.59	—	—	ns
Rising edge of CAMSCK to rising edge of CAMCSEEPROM	Tpd8		119.94	—	—	ns

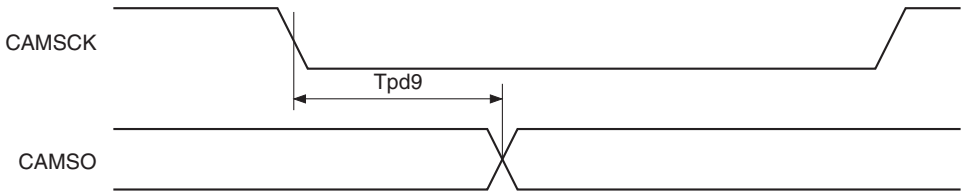
◆ **CAMSI pin**



(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Input setup time	Tsu3	CAMSI	26.2	—	—	ns
Input hold time	Th3		0	—	—	ns

◆ **CAMSO pin**

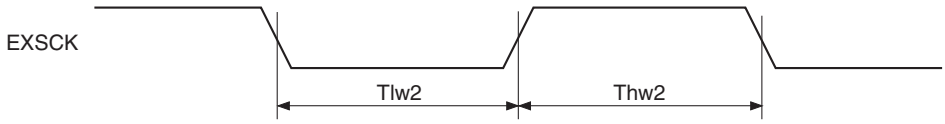


(within the recommended operating range, CAMSCK, CAMSO load capacitance = 29 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd9	CAMSO	–11.01	—	10.61	ns

◆ **EXSCK pin**

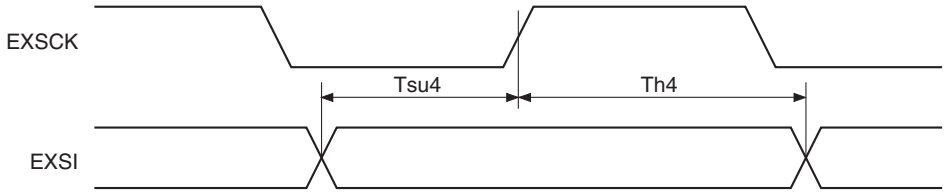
EXSCK, EXSI, EXCS, EXSO and EXBUSY pins are input signals to communicate with external microcomputer.



(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output pulse width (High period)	Thw2	EXSCK	78.6	—	—	ns
Output pulse width (Low period)	Tlw2		78.6	—	—	ns

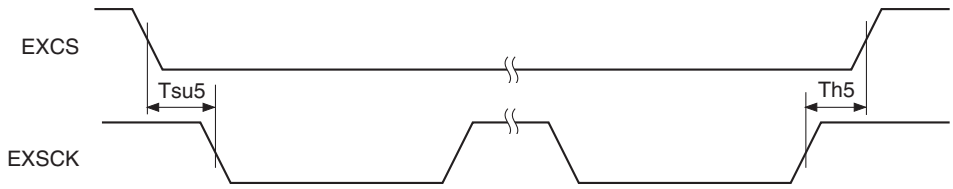
◆ **EXSI pin**



(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Input setup time	Tsu4	EXSI	0	—	—	ns
Input hold time	Th4		85.03	—	—	ns

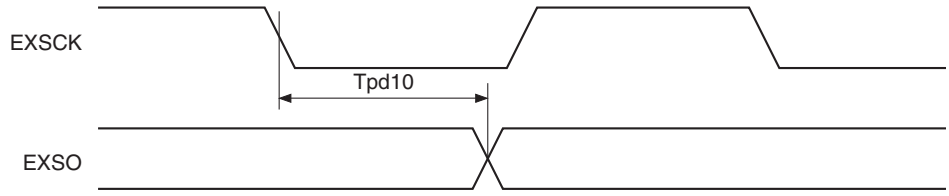
◆ **EXCS pin**



(within the recommended operating range)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Falling edge of EXCS to falling edge of EXSCK	Tsu5	EXCS	78.6	—	—	ns
Rising edge of EXSCK to rising edge of EXCS	Th5		78.6	—	—	ns

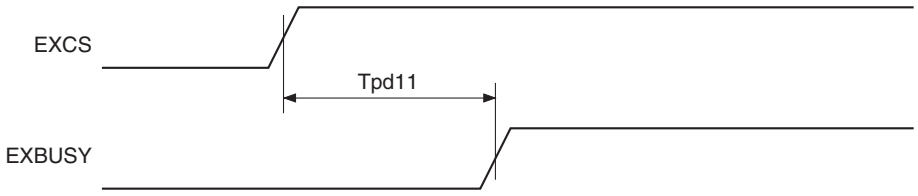
◆ **EXSO pin**



(within the recommended operating range, EXSO load capacitance = 20.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd10	EXSO	57.85	—	132.15	ns

◆ **EXBUSY pin**

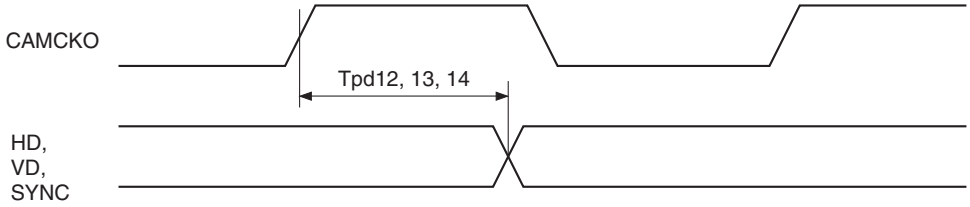


(within the recommended operating range, EXBUSY load capacitance = 20.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd11	EXBUSY	54.44	—	141.22	ns

◆ **HD, VD and SYNC pins**
(HD, VD signals for external AFD and external sync/SYNC signal for video servo)

HD and VD signals for external AFD and external sync, and SYNC signal for video servo can be output from the HD, VD and SYNC pins by changing parameter setting.
Shared with PA[2:0] pin, this is defined as PA[2:0] pin specification.
In addition, shared with DCKO pin, CAMCKO is defined as DCKO pin specification.

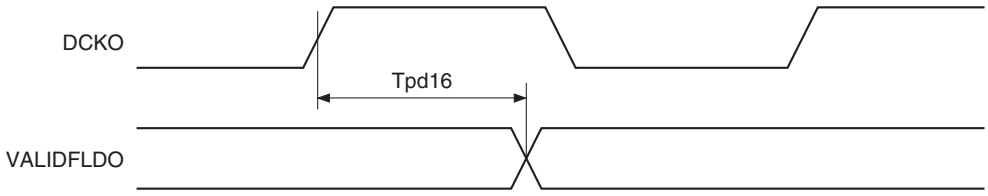


(within the recommended operating range, DCKO and PA[2:0] load capacitance = 14.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd12	HD (PA[2:0])	10	—	45.6	ns
	Tpd13	VD (PA[2:0])	10	—	45.6	ns
	Tpd14	SYNC (PA[2:0])	10	—	45.6	ns

◆ **AFVALID pin**

Shared with PA[2:0] pin, this is defined as PA[2:0] pin specification.
In addition, shared with DCKO pin, CAMCKO is defined as DCKO pin specification.



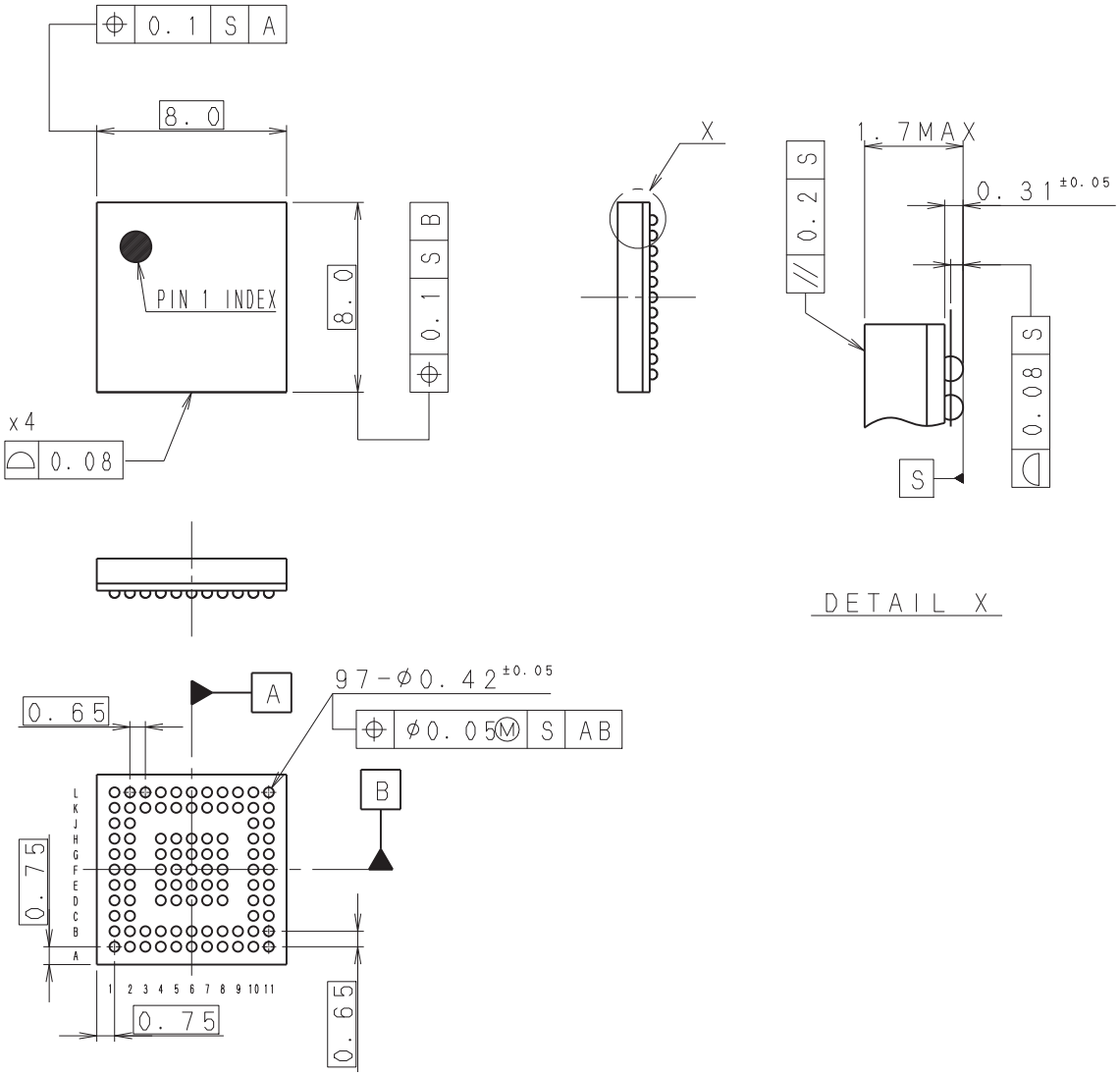
(within the recommended operating range, DCKO load capacitance = 14.5 pF,
PA[2:0] load capacitance = 20.5 pF)

Item	Symbol	Pin name	Min.	Typ.	Max.	Unit
Output delay time	Tpd15	AFVALID (PA[2:0])	3	—	50.5	ns

Package Outline

(Unit: mm)

97PIN LFBGA



SONY CODE	LFBGA-97P-01
JEITA CODE	P-LFBGA97-8X8-0.65
JEDEC CODE	————

P-9576-A4001BS Rev. 0

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	*.*g